TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD × 16-BIT EDO (HYPER PAGE) DYNAMIC RAM

DESCRIPTION

The TC5118165CJ/CFT is an EDO (hyper page) dynamic RAM organized as 1,048,576 words by 16 bits. The TC5118165CJ/CFT utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC5118165CJ/CFT to be packaged in a 42-pin plastic SOJ or a 50-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of 5 V ± 10% tolerance and direct interfacing with high performance logic families such as Schottky TTL.

FEATURES

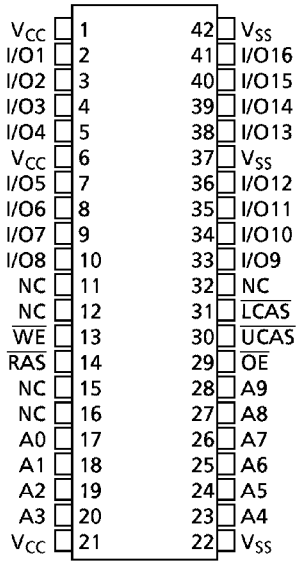
- 1,048,576-word by 16-bit organization
- Fast access time and cycle time

		TC5118165CJ/CFT	
		-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	50 ns	60 ns
t_{AA}	Column Address Access Time	25 ns	30 ns
t_{CAC}	$\overline{CAS}$ Access Time	14 ns	17 ns
t_{RC}	Cycle Time	84 ns	104 ns
t_{HPC}	Hyper Page Mode Cycle Time	20 ns	25 ns

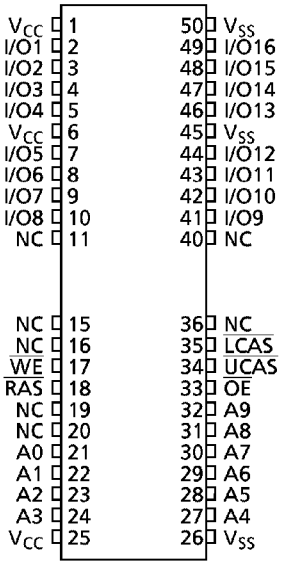
- Single power supply of 5 V ± 10% with a built-in V_{BB} generator
- Low-power dissipation (max)
  - Operating: 1237 mW (50 ns type)
  - : 1018 mW (60 ns type)
  - Stand by : 5.5 mW (both devices)
- Unlatched outputs at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-Only refresh, Hidden refresh and EDO (Hyper Page mode) capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles per 16 ms
- Package
  - CJ : SOJ42-P-400-1.27, 1.66 grams
  - CFT: TSOP II 50/44-P-400-0.80, 0.53 grams

PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ



Plastic TSOP

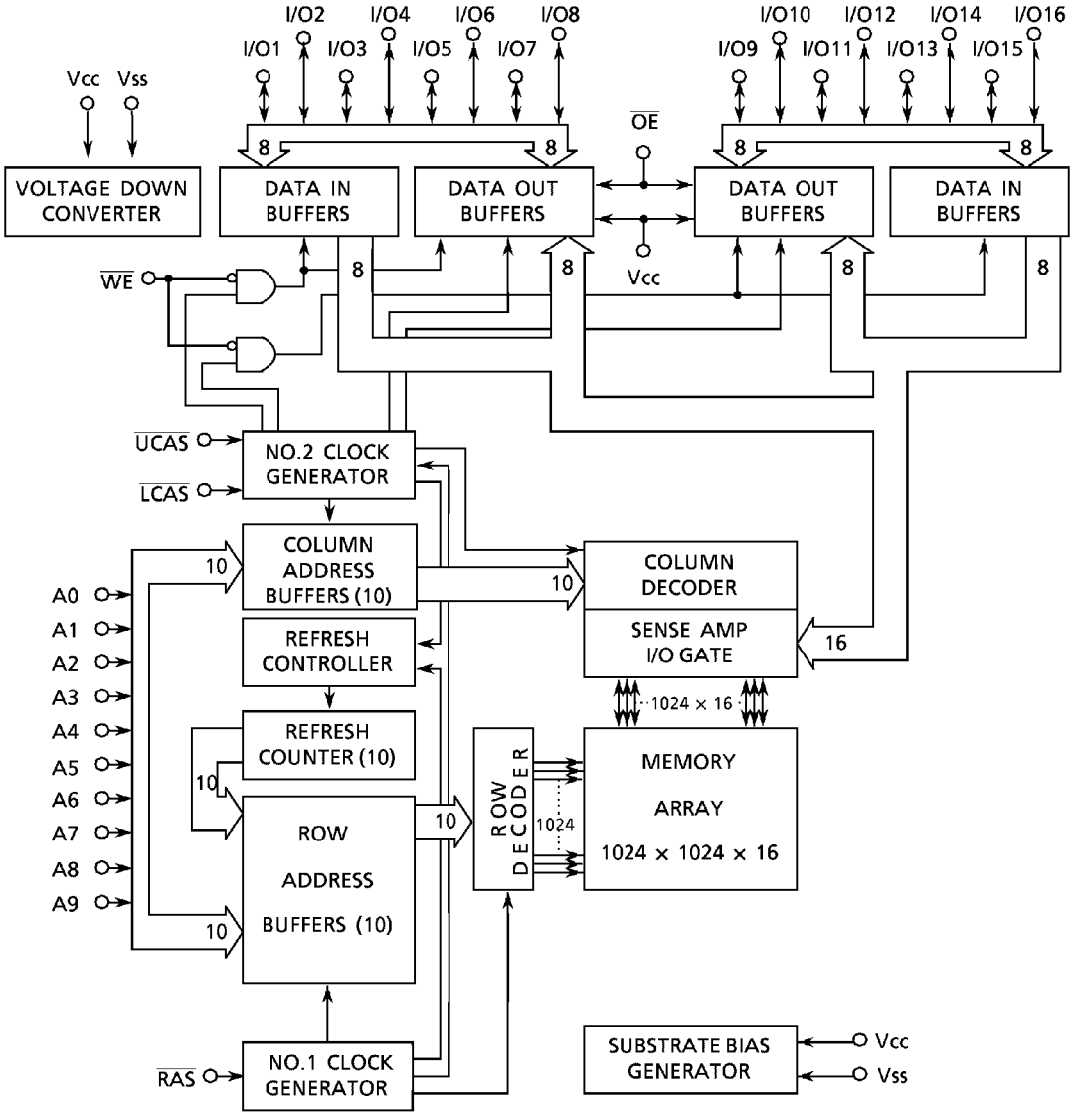


PIN NAMES

A0 to A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe /Upper Byte Control
$\overline{LCAS}$	Column Address Strobe /Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 to I/O16	Data I/O
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
N.C.	No Connection

961001EBA2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	– 0.5 to V_{CC} + 0.5	V	1
Output Voltage	V_{OUT}	– 0.5 to V_{CC} + 0.5	V	1
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V	1
Operating Temperature	T_{OPR}	0 to 70	°C	1
Storage Temperature	T_{STG}	– 55 to 150	°C	1
Soldering Temperature (10 s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	V_{CC} + 0.5*	V	2
V_{IL}	Input Low Voltage	– 0.5**	–	0.8	V	2

* V_{CC} + 2.0 V at pulse width ≦ 20 ns (pulse width is measured at V_{CC})

** – 2.0 V at pulse width ≦ 20 ns (pulse width is measured at V_{SS})

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{RC} = t_{RC} min)	TC5118165CJ/CFT-50	–	225	mA	3, 4, 5
		TC5118165CJ/CFT-60	–	185		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}: t_{RC} = t_{RC} min)	TC5118165CJ/CFT-50	–	225	mA	3, 5
		TC5118165CJ/CFT-60	–	185		
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	TC5118165CJ/CFT-50	–	145	mA	3, 4, 5
		TC5118165CJ/CFT-60	–	105		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{CC} – 0.2 V)		–	1	mA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, CAS-before-RAS Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Cycling: t_{RC} = t_{RC} min)	TC5118165CJ/CFT-50	–	225	mA	3, 4, 5
		TC5118165CJ/CFT-60	–	185		
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0 V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not under Test = 0 V)		– 10	10	μA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is disabled, 0 V ≦ V_{OUT} ≦ V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage (I_{OUT} = – 5 mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage (I_{OUT} = 4.2 mA)		–	0.4	V	