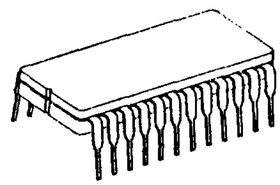
NMOS ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

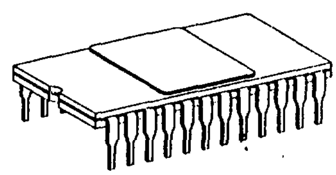
DESCRIPTION

The EF 6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the EF 6800 Microprocessing Unit.

The bus interface of the EF 6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional and data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided.



J suffix
DIL 24
Ceramic Cerdip package



C suffix
DIL 24
Ceramic Side Brazed package

E suffix
LCCC 28
Leadless Ceramic Chip Carrier package

See the ordering information § 11.

Pin connection : see § 10.

MAIN FEATURES

- 8- and 9-bit transmission.
- Optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional + 1, + 16 and + 64 clock modes.
- Up to 1.0 Mbps transmission.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered.
- One- or two-stop bit operation.
- Three available versions :
  - EF 6850 (1.0 MHz),
  - EF 68A50 (1.5 MHz),
  - EF 68B50 (2 MHz) - 0°C to 70°C only.

SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 class B.
- NFC 96863 class G.
- or according to TMS standards.

SUMMARY

A - GENERAL DESCRIPTION

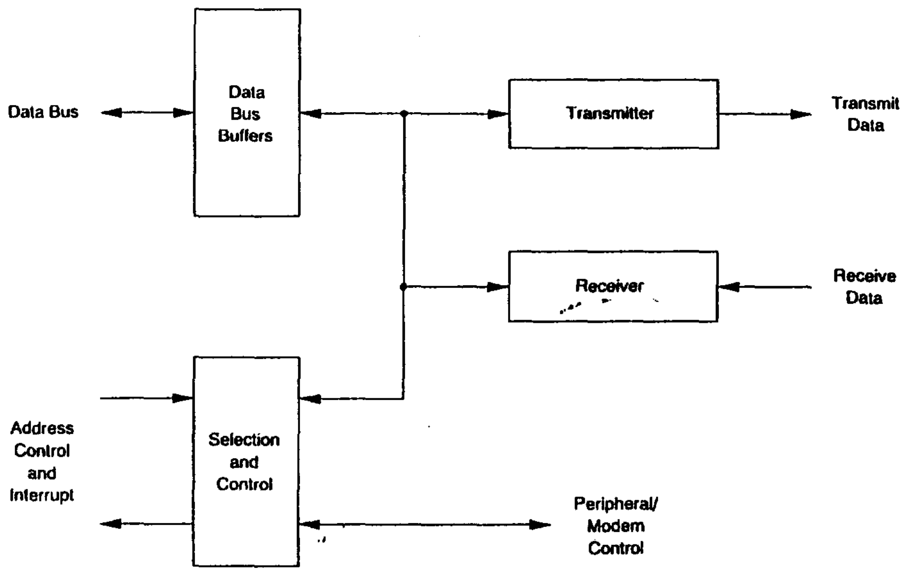


Figure 1 : EF 6850 asynchronous communications interface adapter block diagram.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the peripherals EF 6850, 1, 1.5 and 2 MHz, in compliance with MIL-STD-883 class B and TMS standards.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38510 : general specifications for microcircuits.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in § 10.1 and § 10.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-M-38510 appendix C (when defined):

- 24 leads - DIL Ceramic Side Brazed
- 24 leads - DIL Ceramic Cerdip
- 28 leads - LCCC Leadless Ceramic Chip Carrier

The precise case outlines are described on § 9.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter		Test conditions	Min	Max	Unit
V_{CC}	Supply voltage			−0.3	+7.0	V
V_I	Input voltage			−0.3	+7.0	V
P_{dmax}	Max Power dissipation		T_{case} = −55°C		0.7	W
			T_{case} = +125°C		0.4	W
T_{case}	Operating temperature	M suffix : EF 6850/EF 68A50	f = 1 and 1.5 MHz	−55	+125	°C
		V suffix : EF 6850/EF 68A50	f = 1 and 1.5 MHz	−40	+85	°C
		No suffix : EF 6850/EF 68A50/EF 68B50	f = 1, 1.5 and 2 MHz	0	+70	°C
T_{stg}	Storage temperature			−55	+150	°C
T_j	Junction temperature				+160	°C
T_{leads}	Lead temperature		Max 5 sec. soldering		+270	°C

Note : This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

3.4 - Thermal characteristics (at 25°C)

Table 2

Package	Symbol	Parameter	Value	Unit
DIL 28	θ JA	Thermal resistance - Ceramic junction to ambient	65	°C/W
	θ JC	Thermal resistance - Ceramic junction to case	15	°C/W
LCCC 28	θ JA	Thermal resistance - Ceramic junction to ambient	86	°C/W
	θ JC	Thermal resistance - Ceramic junction to case	15	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics are specified, for inspection purpose, refer to relevant specification:
Table 3: Static electrical characteristics for all electrical variants. See § 5.2.
Tables 4 and 5: Dynamic electrical characteristics. See § 5.3.

For static characteristics, test methods refer to clause 5.4 hereafter of this specification.

For dynamic characteristics, test methods refer to IEC 748-2 method number, where existing.

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature.

5.2 · Static characteristics

Table 3

V_{CC} = 5.0 V_{dc} ±5 % ; V_{SS} = 0 V_{dc} ; T_c = −55°C / +125°C or −40°C / +85°C or 0°C / +70°C

Symbol	Characteristic	Min	Typ	Max	Unit
V_{IH}	Input high voltage	V_{SS} +2.0		V_{CC}	V
V_{IL}	Input low voltage	V_{SS} −0.3		V_{SS} +0.8	V
I_{in}	Input leakage current R/$\overline{W}$, CS0, CS1, $\overline{CS2}$, Enable (V_{in} = 0 to 5.25 V) RS, Rx D, Rx C, $\overline{CTS}$, $\overline{DCD}$		1.0	2.5	µA
I_{TSI}	Hi-Z (off state) input current (V_{in} = 0.4 to 2.4 V) D0-D7		2.0	10	µA
V_{OH}	Output high voltage (I_{load} = −205 µA, Enabled pulse width < 25 µs) D0-D7 (I_{load} = −100 µA, Enabled pulse width < 25 µs) Tx Data, $\overline{RTS}$	 V_{SS} +2.4 V_{SS} +2.4			 V V
V_{OL}	Output low voltage (I_{load} = 1.6 mA, Enabled pulse width < 25 µs)			V_{SS} +0.4	V
I_{LOH}	Output leakage current (off state) (V_{OH} = 2.4 V) $\overline{IRQ}$		1.0	10	µA
P_{INT}	Internal power dissipation (measured at T_A = 0°C)		400	700	mW
C_{in}	Internal Input capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7 E, Tx CLK, Rx CLK, R/$\overline{W}$, RS, Rx, Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$		 10 7.0	 12.5 7.5	 pF pF
C_{out}	Output capacitance RTS, Rx Data (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) $\overline{IRQ}$			10 5.0	pF pF

5.3 · Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C or −40°C to +85°C or 0°C to +70°C and V_{CC} in the range 4.75 V to 5.25 V V_{IL} = 0.8 V and V_{IH} = 2.0 V.

Table 4 · Serial data timing characteristics

Symbol	Characteristic	EF 6850		EF 68A50		EF 68B50		Unit
		Min	Max	Min	Max	Min	Max	
PW_{CL}	Data clock pulse width, low (see Figure 2) +16, +64 Modes +1 Mode	600 900		450 650		280 500		ns ns
PW_{CH}	Data clock pulse width, high (see Figure 3) +16, +64 Modes +1 Mode	600 900		450 650		280 500		ns ns
f_C	Data clock frequency +16, +64 Modes +1 Mode		0.8 500		1.0 750		1.5 1000	MHz kHz
t_{TDD}	Data clock-to-data delay for transmitter (see Figure 4)		600		540		460	ns
t_{RDS}	Receive data setup time (see Figure 5) +1 Modes	250		100		30		ns
t_{RDH}	Receive data hold time (see Figure 6) +1 Modes	250		100		30		ns
t_{IR}	Interrupt request release time (see Figure 7)		1.2		0.9		0.7	µs
t_{RST}	Request-to-send delay time (see Figue 7)		560		480		400	ns
t_r, t_f	Input rise and fall times (or 10 % of the pulse width if smaller)		1.0		0.5		0.25	µs

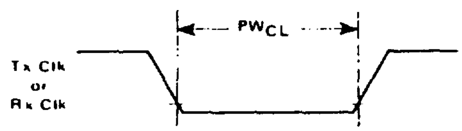


Figure 2 : Clock pulse width, low-state.

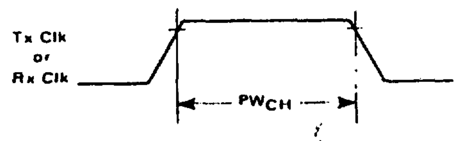


Figure 3 : Clock pulse width, high-state.

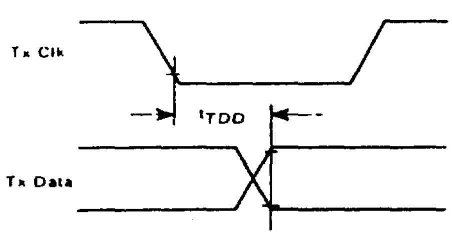


Figure 4 : Transmit data output delay.

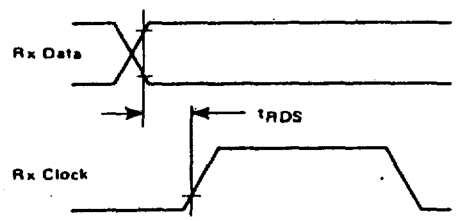


Figure 5 : Receive data setup time (+1 Mode).

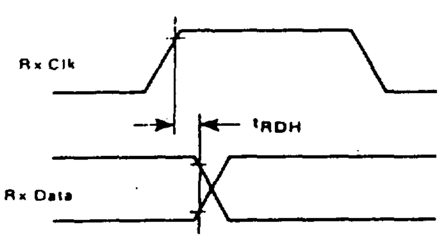


Figure 6 : Receive data hold time (+1 Mode).

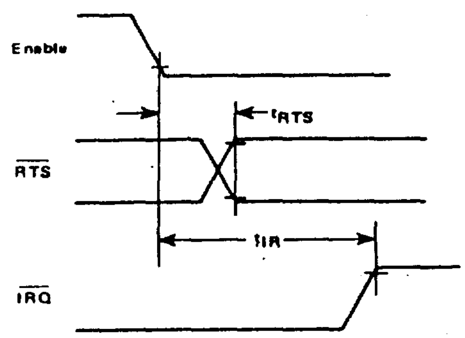


Figure 7 : Request-to-send delay and interrupt-request release times.

Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

Table 5 · Bus timing characteristics · see Notes 1, 2 and Figure 8

Ident. Number	Symbol	Characteristic	EF 6850		EF 68A50		EF 68B50		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{cyc}	Cycle time	1.0	10	0.67	10	0.5	10	μs
2	PW_{EL}	Pulse width, E low	430	9500	280	9500	210	9500	ns
3	PW_{EH}	Pulse width, E high	450	9500	280	9500	220	9500	ns
4	t_r, t_f	Clock rise and fall time		25		25		20	ns
9	t_{AH}	Address hold time	10		10		10		ns
13	t_{AS}	Address setuo time before E	80		60		40		ns
14	t_{CS}	Chip select setup time before E	80		60		40		ns
15	t_{CH}	Chip select hold time	10		10		10		ns
18	t_{DHR}	Read data hold time	20	50*	20	50*	20	50*	ns
21	t_{DHW}	Write data hold time	10		10		10		ns
30	t_{DDR}	Output data delay time		290		180		150	ns
31	t_{DSW}	Input data setput time	165		80		60		ns

* The data bus output buffers are not longer sourcing or sinking current by t_{DHR} max (high impedance).
Note 1 : Voltage levels shown are $V_L \leqslant 0.4$ V, $V_H \geqslant 2.4$ V, unless otherwise specified.
Note 2 : Measurements points shown are 0.8 V and 2.0 V, unless otherwise specified.

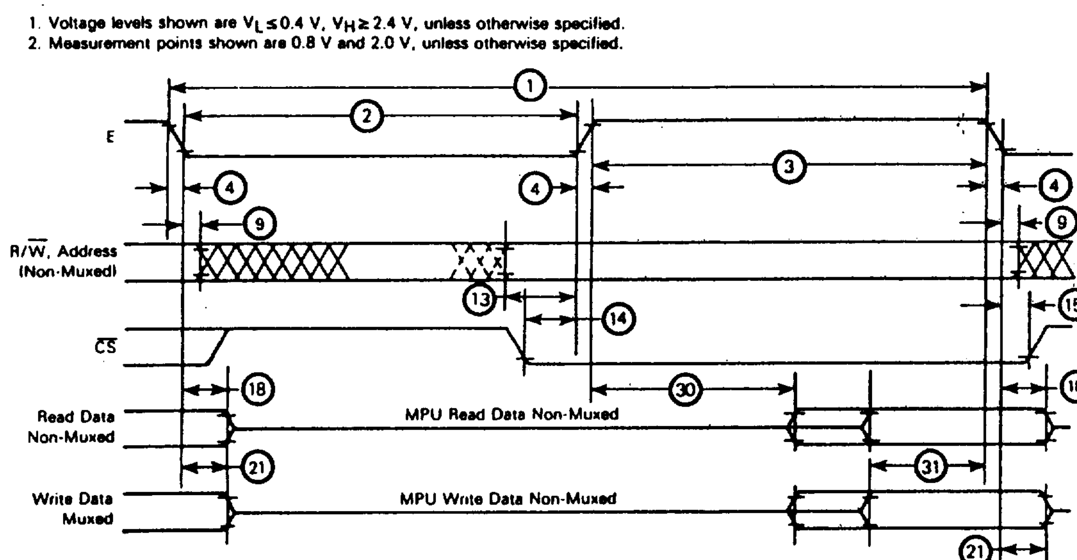


Figure 8 : Bus timing characteristics.

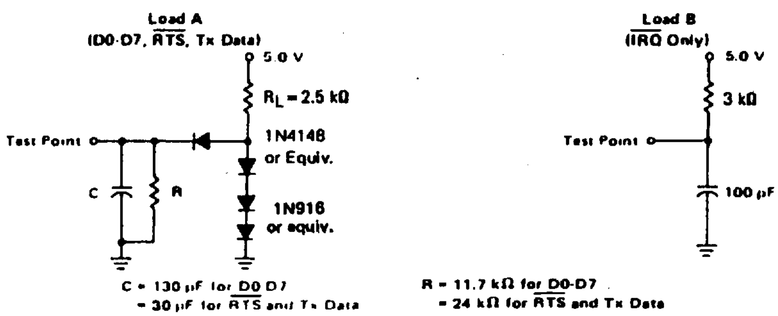


Figure 9 : Bus timing test loads.

6 - FUNCTIONAL DESCRIPTION

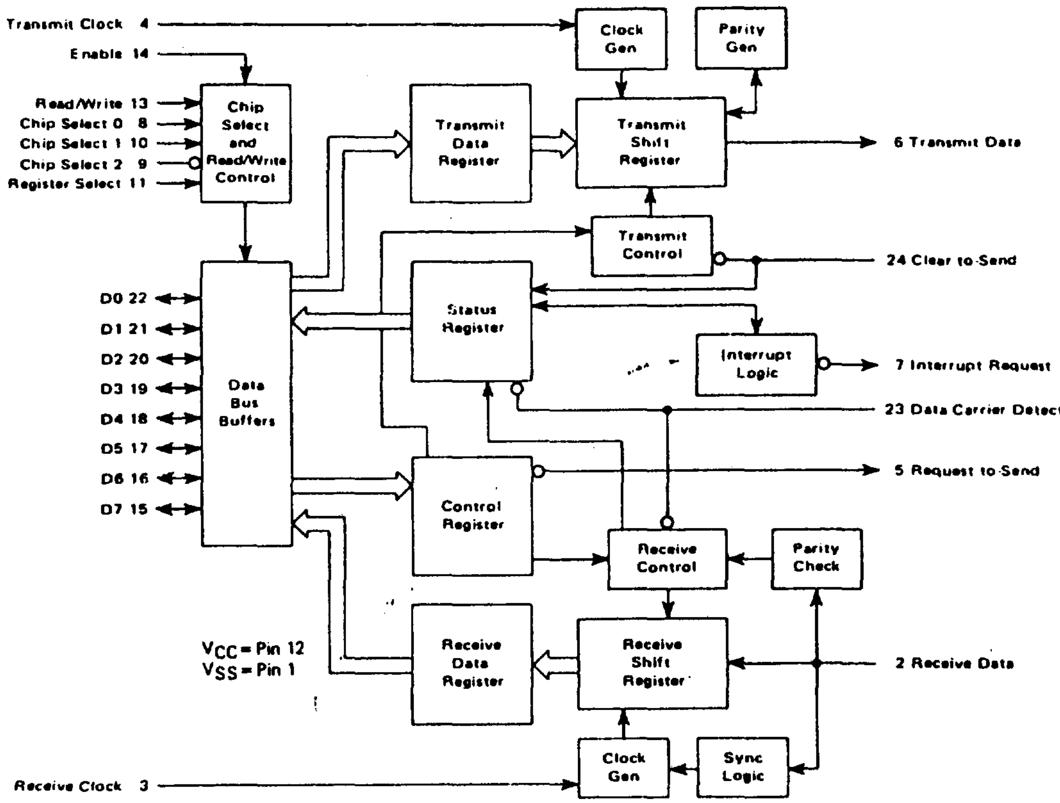


Figure 10 : Expanded block diagram.

6.1 - Device operation

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers : two read-only and two write-only registers. The read-only registers are Status and Receive Data ; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

6.1.1 - Power on/master reset

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACAI functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuity depends on clean power turn on transitions. The power-on reset released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider rations, variable word-length, one or two stop bits, parity (even, odd, or none), etc.

6.1.2 - Transmit

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even through the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

6.1.3 - Receive

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

6.2 - Input/output functions

6.2.1 - ACIA interface signals for MPU

The ACIA interfaces to the 6800 MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the ACIA.

ACIA Bidirectional Data (D0-D7) - The bidirectional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) - The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the EF 6800 Φ_2 Clock or EF 6809E clock.

Read/Write (R/$\overline{W}$) - The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) - These three high-impedance TTL-compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable Signal, Read Write, and Register Select.

Register Select (RS) - The Register Select is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjuction with Register Select to select the read-only or write-only register in each register pair.

Interupt Request ($\overline{IRQ}$) - Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ outputs is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writting data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bits. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occured, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can bi cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred an then reading the Receive Data Register or reseting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

6.2.2 - Clock inputs

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (Tx CLK) - The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx CLK) - The Receive Clock input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally). The receiver samples the data on the positive transition of the clock.

6.2.3 - Serial input/output lines

Receive Data (RX Data) - The Receive Data is a high-impedance TTL-compatible input through which data is received a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (Tx Data) - The Transmit Data ouptut line transfers serial to a modem or other peripheral.

6.2.4 - Peripheral/modem control

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) - This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) - The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the RTS output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) - This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

6.3 - ACIA registers

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 6.

6.3.1 - Transmit data register (TDR)

Data is written in the Transmit Data Register during the negative transition of enable (E) when the ACIA has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

6.3.2 - Receive data register (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

Table 6 - Definition of ACIA register contents

Data bus line number	Buffer address			
	RS • R/$\overline{W}$ Transmit data register	RS • R/W Receive data register	$\overline{RS}$ • R/$\overline{W}$ Control register	$\overline{RS}$ • R/W Status register
	(Write only)	(Read only)	(Write only)	(Read only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7**	Data Bit 7***	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit = LSB = Bit 0.
** Data bit is «don't care» in 7-bit plus parity modes.
*** Data bit will be zero in 7-bit plus parity modes.

6.3.3 - Control register

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and $R/\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) - The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	+1
0	1	+16
1	0	+64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) - The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

Word lenth , Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Transmitter Control Bits (CR5 and CR6) - Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled

Receive Interrupt Enable Bit (CR7) - The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

6.3.4 - Status register

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and $R/\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 - Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 - The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 - The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 - Framing error indicates that the received character in improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty tranmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throught the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 - Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occured. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 - The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data characteris in the RDR. If no parity selected, then both the transmitter parity generator outupt and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 - The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 - Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

8 - HANDLING

MOS device must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

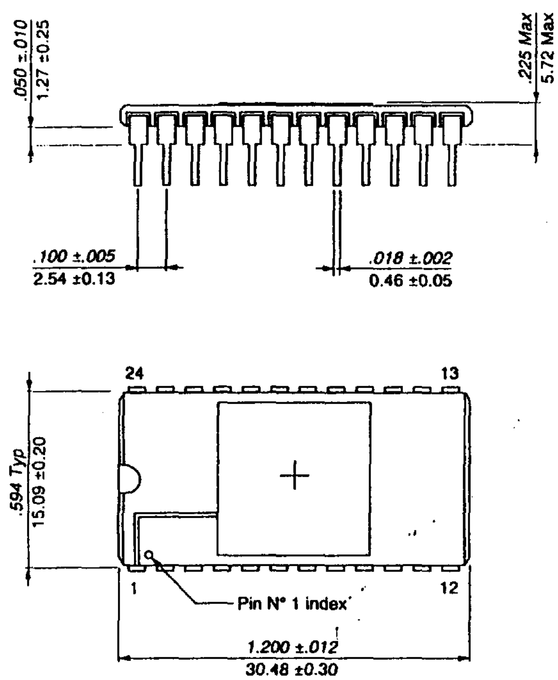
d) Store devices in conductive foam or carriers.

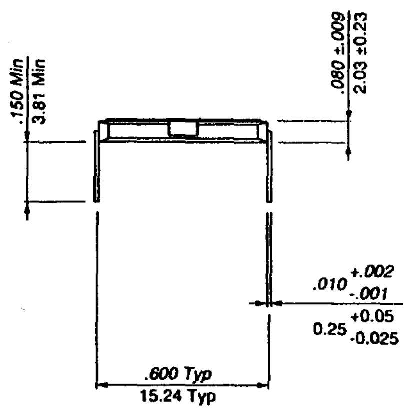
e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 %, if pratical.

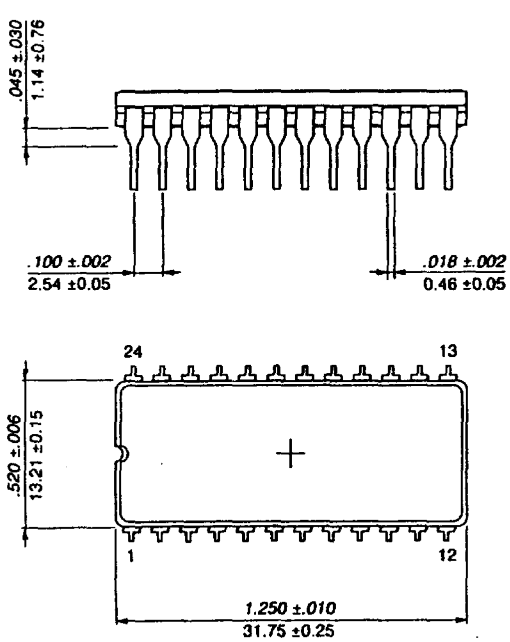
9 - PACKAGE MECHANICAL DATA

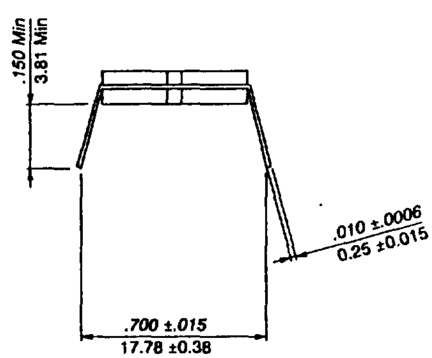
9.1 - 24 pins - DIL Ceramic Side Brazed package



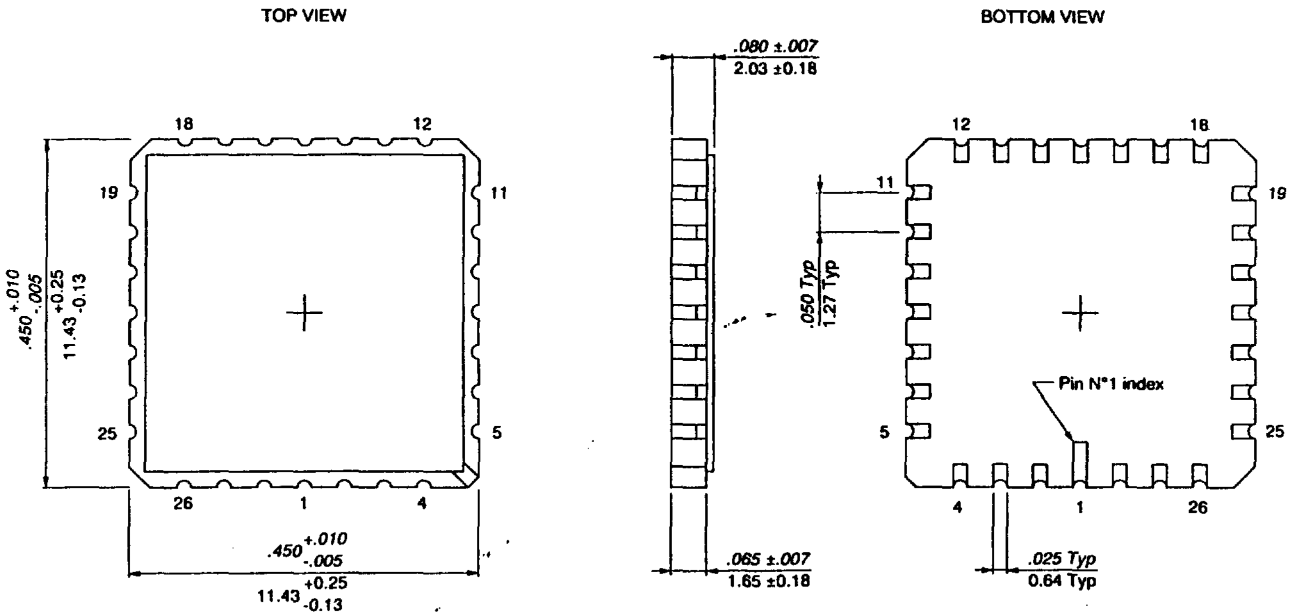


9.2 - 24 pins - DIL Cerdip package



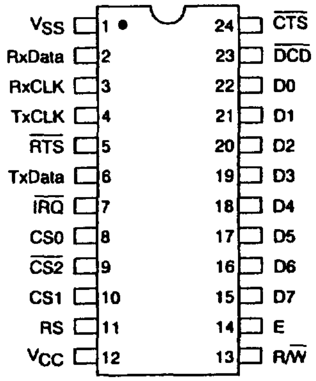


9.3 - 28 pins - Leadless Ceramic Chip Carrier package

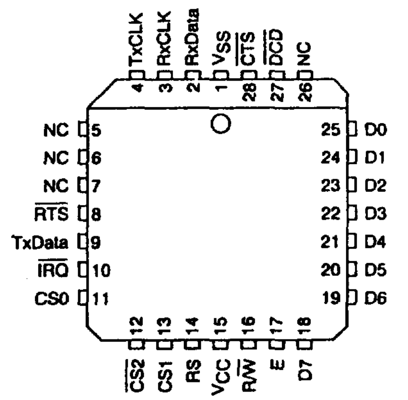


10 - TERMINAL CONNECTIONS

10.1 - 24 pins - Pin assignment (DIL)



10.2 - 28 pins - Pin assignment (LCCC)



11 - ORDERING INFORMATION

11.1 - Hi-REL product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6850JMG/B	NFC 96863 class G	DIL Cerdip	– 55 / + 125	1	Data sheet
EF6850CMG/B*	NFC 96863 class G	DIL Side Brazed	– 55 / + 125	1	Data sheet
EF6850EMG/B	NFC 96863 class G	LCCC	– 55 / + 125	1	Data sheet
EF68A50JMG/B	NFC 96863 class G	DIL Cerdip	– 55 / + 125	1.5	Data sheet
EF68A50CMG/B*	NFC 96863 class G	DIL Side Brazed	– 55 / + 125	1.5	Data sheet
EF68A50EMG/B	NFC 96863 class G	LCCC	– 55 / + 125	1.5	Data sheet
EF6850JMB/C	MIL-STD-883 class B	DIL Cerdip	– 55 / + 125	1	Data sheet
EF6850C1MB/C*	MIL-STD-883 class B	DIL Side Brazed	– 55 / + 125	1	Data sheet
EF6850E1MB/C	MIL-STD-883 class B	LCCC	– 55 / + 125	1	Data sheet
EF68A50JMB/C	MIL-STD-883 class B	DIL Cerdip	– 55 / + 125	1.5	Data sheet
EF68A50C1MB/C*	MIL-STD-883 class B	DIL Side Brazed	– 55 / + 125	1.5	Data sheet
EF68A50EMB/T	According to MIL-STD-883 class B	LCCC	– 55 / + 125	1.5	Data sheet

* Non considered anymore as standard package, Cerdip is preferred.
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

11.2 - Standard product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6850CV*	TMS standard	DIL Side Brazed	– 40 / + 85	1	Data sheet
EF6850JV	TMS standard	DIL Cerdip	– 40 / + 85	1	Data sheet
EF68A50CV*	TMS standard	DIL Side Brazed	– 40 / + 85	1.5	Data sheet
EF68A50JV	TMS standard	DIL Cerdip	– 40 / + 85	1.5	Data sheet
EF6850JM	TMS standard	DIL Cerdip	– 55 / + 125	1	Data sheet
EF6850CM*	TMS standard	DIL Side Brazed	– 55 / + 125	1	Data sheet
EF6850EM	TMS standard	LCCC	– 55 / + 125	1	Data sheet
EF68A50JM	TMS standard	DIL Cerdip	– 55 / + 125	1.5	Data sheet
EF68A50CM*	TMS standard	DIL Side Brazed	– 55 / + 125	1.5	Data sheet
EF68A50EM	TMS standard	LCCC	– 55 / + 125	1.5	Data sheet
EF6850C*	TMS standard	DIL Side Brazed	0 / + 70	1	Data sheet
EF6850J	TMS standard	DIL Cerdip	0 / + 70	1	Data sheet
EF68A50C*	TMS standard	DIL Side Brazed	0 / + 70	1.5	Data sheet
EF68B50J	TMS standard	DIL Cerdip	0 / + 70	2	Data sheet

* Non considered anymore as standard package, Cerdip is preferred.
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

EF6850 C M B/C

Type — EF6850

Packages:
C = Ceramic DIL (side brazed)
C1 = Gold lead, tin lead.
E = Ceramic LCC
E1 = LCC+HOT Solder DIP
J = Tin dipped Cerdip DIL

Temperature /Tcase:
M = -55°C/ +125°C
V = -40°C/ +85°C
_ = 0/ +70°C

Screening:
___ = Standard
G/B = NFC 96883 Cl.G
B/C = MIL STD 883 Cl.B
B/T = according to MIL STD 883 class B

THOMSON COMPONENTS AND TUBES CORPORATION
TCS DIVISION
40G Commerce Way, Post Office Box 540, Totowa, New Jerey 07511-0540
PHONE: (973) 812-9000 FAX: (973) 812-4191

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