BIPOLAR HIGH-SPEED 8-BIT FLASH A/D CONVERTER

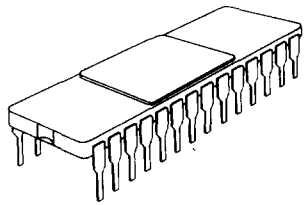
DESCRIPTION

The TS 8378 is a monolithic bipolar 8-bit parallel flash analog-to-digital converter designed for applications requiring very high-speed conversion.

The TS 8378 uses 256 parallel comparators to digitize fast moving analog input signals without external sample-and-hold circuits or input buffers.

With encode rates up to 150 MHz, the TS 8378 is specified to operate from commercial to military temperature range with an analog input frequency of 60 MHz, making it ideal for a variety of applications and environments.

The TS 8378 is packaged in hermetic ceramic 28-pin DIL configuration and also available in die form.

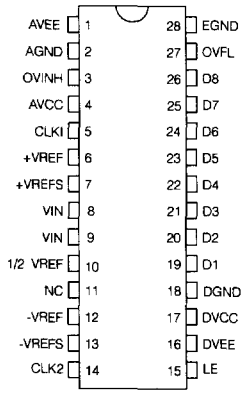


C
DIL 28
(Ceramic package)

MAIN FEATURES

- 8-bit resolution.
- 150 MHz sampling rate.
- Excellent SNR.
- Low power : 0.85 W.
- Dual power supply : 5 V and − 5.2 V.
- − 55°C / + 125°C specified.
- Guaranteed monotonicity.
- High slew rate of input stages.
- Compatible with ECL 10 K.
- Overflow bit functions.
- Output registers.
- No sample & hold required.
- Evaluation board : TSEV 8378.

PIN CONNECTIONS
(Top view)
DIL Ceramic - 28 pins



Note : For details, see «pin description»

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Video digitizing.
- Image processing.
- Medical imaging.
- High-energy physics.
- X-Ray and ultrasound imaging.
- Communication/signal intelligence.

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Parameter	Symbol	Value	Unit
Positive supply voltages (see Note 2)	AV_{CC}, DV_{CC}	+4 to +6	V
Negative supply voltages (see Note 2)	AV_{EE}, DV_{EE}	−6.2 to −4.2	V
Upper reference voltage	$+V_{REF}$, $+V_{REFS}$	+0.3	V
Midpoint reference current	I (1/2 V_{REF})	5	mA
Lower reference voltage	$-V_{REF}$, $-V_{REFS}$	−3	V
Reference voltage range	$+V_{REF}$ to $-V_{REF}$	3.2	V
Analog input (see Note 2)	V_{IN}	−3 to +0.3	V
Digital input voltage (see Note 2)	CLK1, CLK2, LE	V_{EE} to +0.3	V
Digital input voltage (see Note 2)	OV_{INH}	−0.3 to V_{CC}	V
Digital output currents	I_D	30	mA
Junction temperature	T_j	175	°C
Storage temperature	T_{stg}	−65 to +150	°C
Operating temperature range	T_{case}	−55 to +125	°C
Lead temperature (soldering 10 s)	T_{leads}	+260	°C
Maximum difference between negative supply	AV_{EE} to DV_{EE}	±0.5	V
Maximum difference between positive supply	AV_{CC} to DV_{CC}	±0.5	V

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to AGND = DGND.

USER WARNING

The power supplies must be applied before all the other signals to damage from occuring on the devices.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{CC} = DV_{CC} = +5\,V$; $AV_{EE} = DV_{EE} = -5.2\,V$; $R_L = 100\,\Omega$ to $-2\,V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	TS 8378B Min.	TS 8378B Typ.	TS 8378B Max.	TS 8378A Min.	TS 8378A Typ.	TS 8378A Max.	Unit
RESOLUTION				8			8		Bits
DIGITAL INPUTS AND OUTPUTS									
Logic compatibility				ECL 10K			ECL 10K		
Clock inputs									
• Logic «0» voltage	full	IV			−1.5			−1.5	V
• Logic «1» voltage	full	IV	−1.1			−1.1			V
Output data									
• Logic «0» voltage (see Note 1)	full	II, D			−1.5			−1.5	V
• Logic «1» voltage (see Note 2)	full	II, D	−1.1			−1.1			V
• Output delay (see Note 3)		IV		7			7		ns
MAXIMUM CLOCK FREQUENCY		III	125	150		125	150		MHz
ANALOG INPUT									
Voltage range		V		V_{REF}			V_{REF}		V
Input capacitance		IV		20			20		pF
Input resistance		V		10			10		kΩ
Analog bandwidth (see Note 4)		V		150			150		MHz
REFERENCE INPUT									
Differential reference voltage		I, D		2	3		2	3	V
Reference ladder resistance		I, D	50	85	120	50	85	120	Ω
	full	II	40		140	40		140	Ω
POWER REQUIREMENTS									
Power supply									
• Positive supply		I, D	4.5	5	5.5	4.5	5	5.5	V
	full	II	4.5	5	5.5	4.5	5	5.5	V
• Negative supply		I, D	−5.7	−5.2	−4.7	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	−5.7	−5.2	−4.7	V
Power dissipation (see Note 5)									
• Positive supply		I, D		525	725		525	725	mW
	full	II			800			800	mW
• Negative supply		I, D		310	390		310	390	mW
	full	II			430			430	mW
THERMAL RESISTANCE		V							
Junction-to-ambient (still air)				45			45		°C/W
Junction-to-case				5			5		°C/W
ACCURACY (see Note 6)									
Differential nonlinearity		I, D		0.4	0.5		0.6	0.75	LSB
	full	II			0.75			0.9	LSB
Integral nonlinearity		I, D		0.4	0.5		0.6	0.75	LSB
	full	II			0.75			0.9	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			Guaranteed over specified temperature range			

SPECIFICATIONS

Electrical operating characteristics

$AV_{CC} = DV_{CC} = +5\,V$; $AV_{EE} = DV_{EE} = -5.2\,V$; $R_L = 100\,\Omega$ to $-2\,V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	Test level	TS 8378B Min.	TS 8378B Typ.	TS 8378B Max.	TS 8378A Min.	TS 8378A Typ.	TS 8378A Max.	Unit
DYNAMIC CHARACTERISTICS (see Note 7)								
Signal to noise ratio								
F_S = 125 MHz F_{in} = 1 MHz	III	44.5	46.9		44.5	46.9		dB
F_S = 125 MHz F_{in} = 20 MHz	III	39.7	42.7		39.7	42.7		dB
F_S = 100 MHz F_{in} = 50 MHz	III	36.7	39.1		36.7	39.1		dB
F_S = 10 MHz F_{in} = 1.5 MHz	D				43.9	45		dB
Total harmonic distorsion								
F_S = 125 MHz F_{in} = 1 MHz	III	48	54		48	54		dB
F_S = 125 MHz F_{in} = 20 MHz	III	39.7	46		39.7	46		dB
F_S = 100 MHz F_{in} = 50 MHz	III	36.7	42		36.7	42		dB
F_S = 10 MHz F_{in} = 1.5 MHz	D				48	53		dB
Effective number of bits								
F_S = 125 MHz F_{in} = 1 MHz	III	7.1	7.5		7.1	7.5		Bits
F_S = 125 MHz F_{in} = 20 MHz	III	6.3	6.8		6.3	6.8		Bits
F_S = 100 MHz F_{in} = 50 MHz	III	5.8	6.2		5.8	6.2		Bits
F_S = 10 MHz F_{in} = 1.5 MHz	D				7	7.2		Bits
Aperture uncertainty	V		15			15		pS

Note 1 : With I_{OUT} = 2 mA.

Note 2 : With I_{OUT} = 12 mA.

Note 3 : See timing diagram.

Note 4 : The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Note 5 : F_S = 10 MHz - F_{in} = 1.5 MHz.

Note 6 : Histogram based on sampling of 1.5 MHz sinusoidal analog signal with and encode rate of 10 MHz.

Note 7 : Dynamic measurements are performed with an analog input signal 1 dB below full scale.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperature
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at T_{amb} = +25°C (based on A version only).

TIMING DIAGRAM

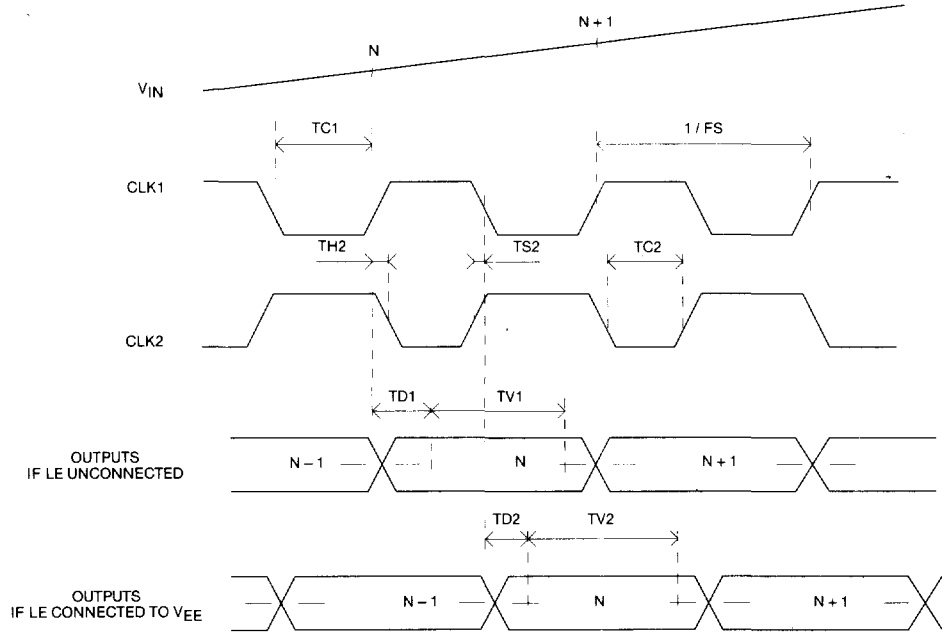


Figure 1

SWITCHING PERFORMANCES (see Notes 1 to 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
1/FS	Minimum period of CLK1 (CLK2)		6.6		ns
TC1	Minimum clock pulse width (low) of CLK1		3.3		ns
TC2	Minimum clock pulse width (low) of CLK2		3.3		ns
TH2	*Hold time of CLK2/CLK1*		0		ns
TS2	Set-up time of CLK2/CLK1		0		ns
TD1	Propagation delay (between CLK1 and outputs (LE unconnected)		7		ns
TD2	Propagation delay (between CLK1 and outputs (LE connected to V_{EE})		4		ns
TV1	Output validity time		4		ns
TV2	Output validity time		5		ns

Note 1 : Outputs terminated through 100 Ω to – 2 V. C_{load} < 10 pF. Clock command rise/fall time should be less than 2 ns in normal operating mode.

Note 2 : See definitions of terms.

Note 3 : $AV_{EE} = DV_{EE} = -5.2\,V$; $AV_{CC} = DV_{CC} = +5\,V$; $+V_{REF} = +0\,V$; $-V_{REF} = -2\,V$.

FUNCTIONAL BLOCK DIAGRAM

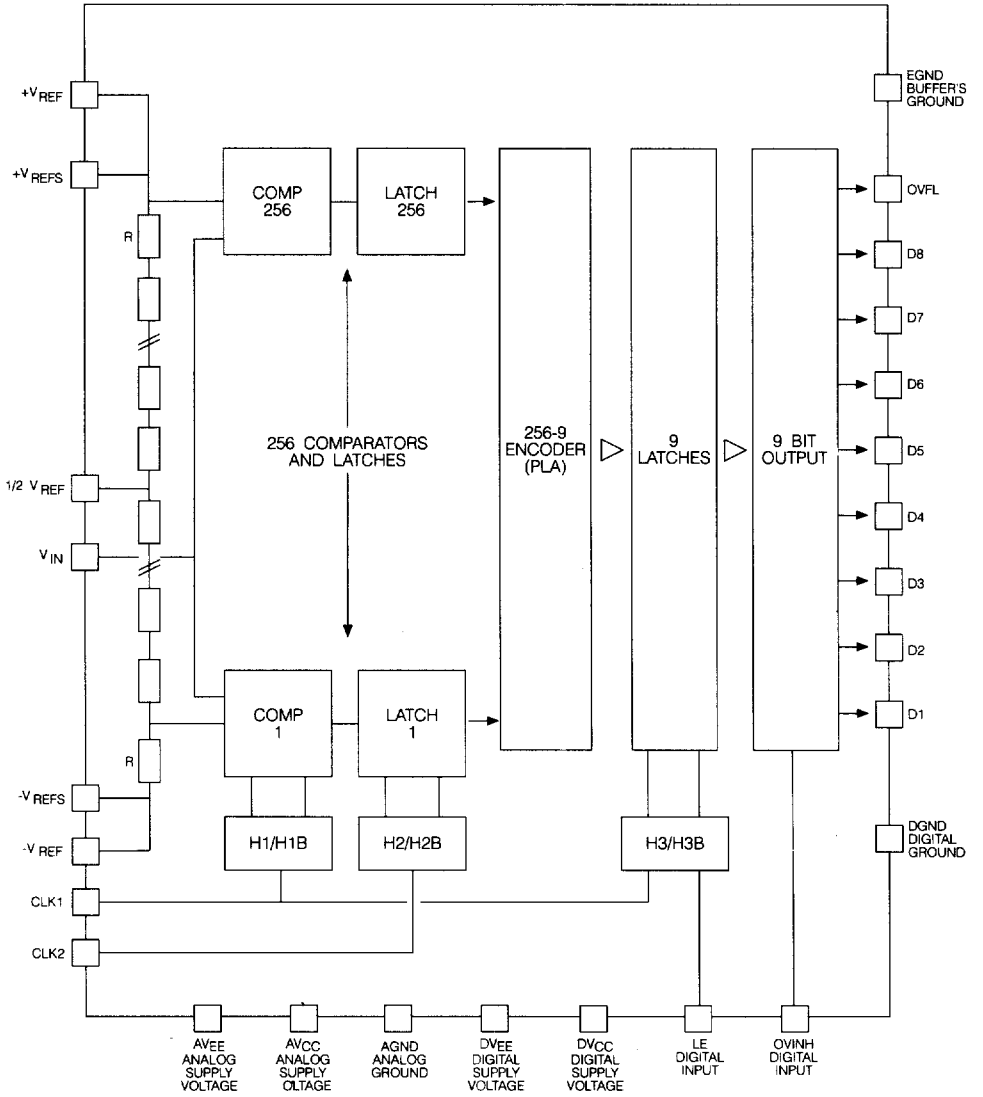


Figure 2

PIN DESCRIPTION

Pin DIL	Symbol	Function	Description
1	AV_{EE}	Negative analog supply	
2	AGND	Analog ground	
3	OV_{INH}	Overflow inhibit (see note 1)	
4	AV_{CC}	Positive analog supply	
5	CLK1	Clock input	ECL 10 K level compatibility
6	$+V_{REF}$	Positive reference voltage input	
7	$+V_{REFS}$	Positive reference voltage sense	
8	V_{IN}	Analog input	
9	V_{IN}	Analog input	
10	$1/2\ V_{REF}$	Reference midpoint	Access to the midpoint tap on the resistance ladder
11	NC	Not connected	
12	$-V_{REF}$	Negative reference voltage input	
13	$-V_{REFS}$	Negative reference voltage sense	
14	CLK2	Clock input	ECL 10 K level compatibility
15	LE	Latch enable (see note 2)	
16	DV_{EE}	Negative digital supply	
17	DV_{CC}	Positive digital supply	
18	DGND	Digital ground	
19	D1	Digital data output (LSB)	ECL 10 K level compatibility
20	D2	Digital data output	
21	D3	Digital data output	
22	D4	Digital data output	
23	D5	Digital data output	
24	D6	Digital data output	
25	D7	Digital data output	
26	D8	Digital data output (MSB)	
27	OVFL	Overflow data output	
28	EGND	Digital output ground	

Note 1 : When tied to GND (or floating), overflow bit OVFL = HIGH and output bits = LOW when the analog input voltage exceeds $+V_{REFS}$. If connected to V_{CC} throw a resistance, overflow bit OVFL = HIGH and non return to zero feature is actived (typically this pin need a voltage of 4.6 V at 25°C). See Figure 3 for the connection.

Truth table when V_{IN} exceeds $+V_{REFS}$

OV_{INH} connect to	< D1 : D8 >	OVFL
GROUND	Low	High
V_{CC}	High	Undetermined
V_{CC} throw a resistance	High	High

Note 2 : When tied to GND (or floating), output latches are disabled. If connected to V_{EE}, output latches are actived, which introduces a pipeline delay of half a clock period, but improves output data time skew, and reduces output propagation delay.

THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure having one comparator per state. This architecture enables very high speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 256 reference levels (8 bits + overflow), derived from a resistor ladder network.
Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification.

A set of 256 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal.
An encoder stage (R.O.M.) followed output latches provides output data in binary code, followed by high speed ECL output buffers.

APPLICATIONS

User warning

The power supplies must be applied before all the other signals to prevent damages from occuring on the device.

Functional description

The TS 8378 operates with input analog signals varying between $\pm V_{REF}$ reference voltages, (Nominally $+V_{REF} = 0$ V, $-V_{REF} = -2$ V), applied across an internal resistor ladder.

Maximum differential Reference voltage is 3 V, so external reference generator circuit must limit the voltage to this value, to avoid permanent damage caused to the TS 8378 by excessive current densities. The offset errors caused by input $\pm V_{REF}$ access resistances, can be cancelled using voltage sense lines ($\pm V_{REFS}$ pins).
(Maximum sense current : < 1 mA).

The typical input capacitance of the TS 8378 is 20 pF, which can be driven directly by most 50 Ω signal sources, otherwise it needs simple buffering requirements.

Full logic ECL input clock signals are recommended for the TS 8378, with fast rise and fall times (500 ps), especially when digitizing high frequency input waveforms.
Although the TS 8378 is designed and tested to operate with a 50 % clock cycle, dynamic performance at high data rates can be improved by changing the duty clock cycle.

Output datas is ECL 10K logic compatible.
The OVINH control pin handles output bits format in overflow conditions ($V_{IN} > + V_{REFS}$ sense voltage).
When OVINH is connected to Ground (or allowed to float), overflow bit (OVFL) turns to ECL Logic High and output bits to logic Low.
When OVINH is tied to V_{CC} throw a resistance, overflow bit is high and output bits remain at ECL Logic High.

The control pin LE (Latch Enable), enables the output latches to be actived.
When LE is connected to V_{EE}, output latches are actived and output propagation delay (TD) is reduced from 7 ns to 5 ns. This feature introduces a pipeline delay of half a clock cycle, but improves output data time skew. The output data change on falling edge of clock signal (CLK1), after specified output propagation delay TD.

When LE control pin is connected to Ground, the latches are disabled and output data changes on rising edge of clock signal (CLK1), (comparators in latch mode), after a typical output propagation delay of 7 ns.

Packaging

The TS 8378 is mounted in ceramic 28-pin DIL package.
Sockets may be used for prototype evaluation, but should be avoided afterwards, because it leads to increased decoupling difficulties, and limitations of TS 8378 dynamic performance.

TYPICAL EVALUATION CIRCUIT (see page 9)

Designs involving the TS 8378 must follow a few precautions to ensure optimum performance. The following design suggestions are essentially meant to avoid many of the high-speed design problems.

Multilayer printed circuit board is recommended, because it enables compact implementation, and allows easy design of low impedance continuous Supply and Ground planes.
All ground pins should be connected to the ground plane as close to the package as possible.
Proper supply decoupling by high resonant frequency chip capacitors close to the device, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

The length of digital input/output signal paths should be matched and kept short, to avoid propagation delay mismatches, increased output bits time skew, and over or undershoot caused by reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the wave form.
However, if long interconnection lengths cannot be avoided, proper design of transmission line impedance with adapted ECL termination loads has to be observed.
Chip resistors (100 Ω to −2 V) are recommended for ECL pulldown output terminations.

50 Ω impedance microstrip line with 50 Ω termination chip resistors should be used for analog and clock input pins. (Pins 8, 9 and 5, 14).

High speed ECL quad latches should be used to extend the validity time of the digital outputs and simplify their acquisition.

TYPICAL EVALUATION CIRCUIT

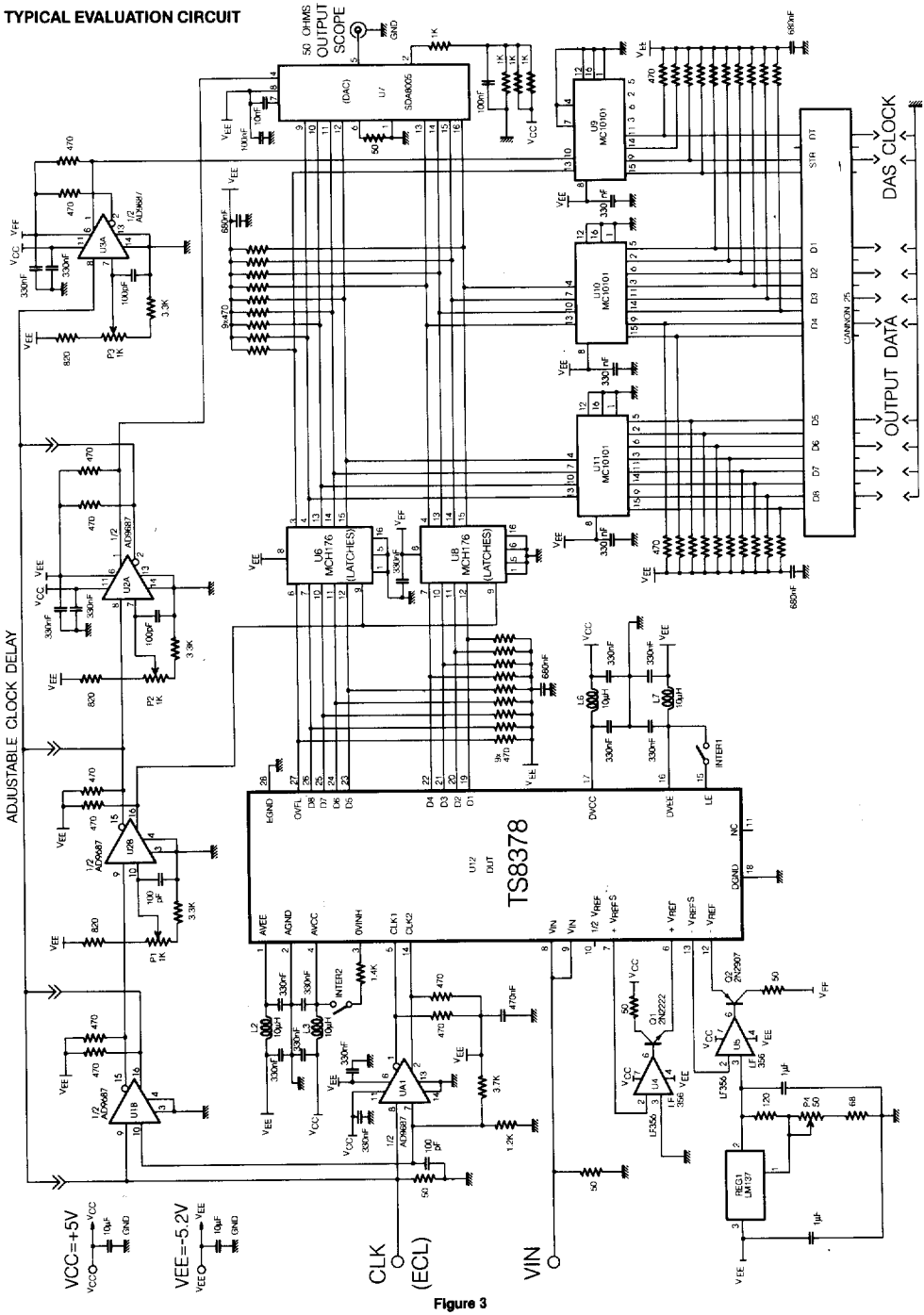


Figure 3

TYPICAL PERFORMANCE CURVES

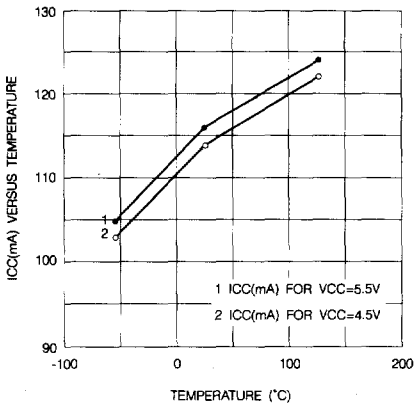


Figure 4 : I_{CC} vs. temperature.

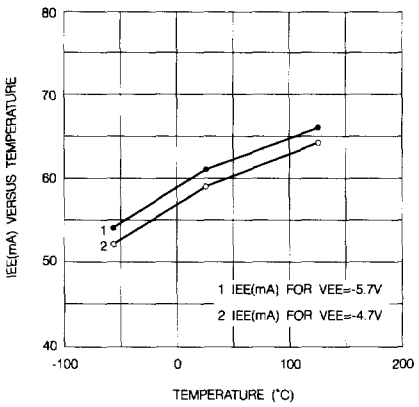


Figure 5 : I_{EE} vs. temperature.

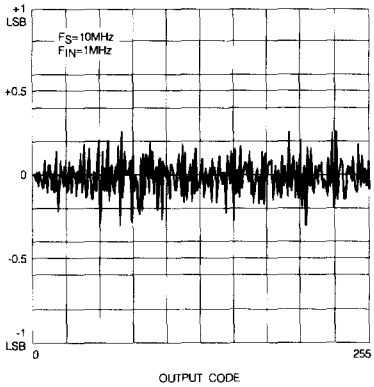


Figure 6 : Differential non linearity.

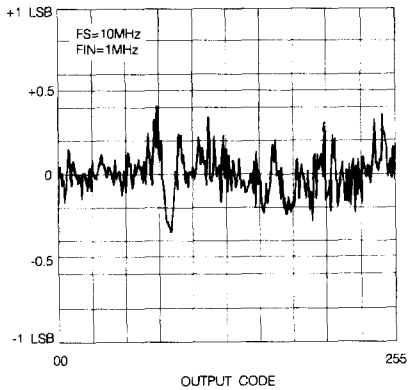


Figure 7 : Integral non linearity.

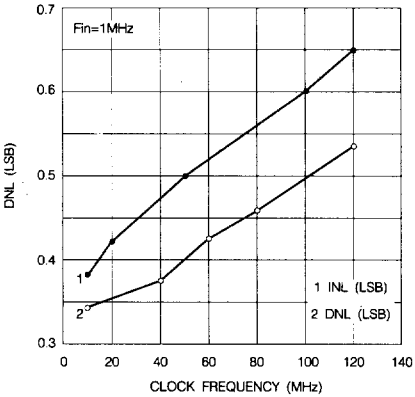


Figure 8 : Differential and integral nonlinearity vs. sampling rate.

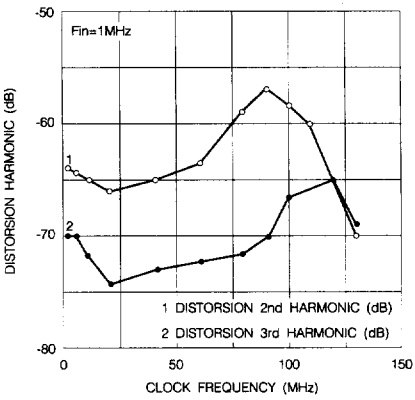


Figure 9 : Distorsion 2nd and 3rd vs. sampling.

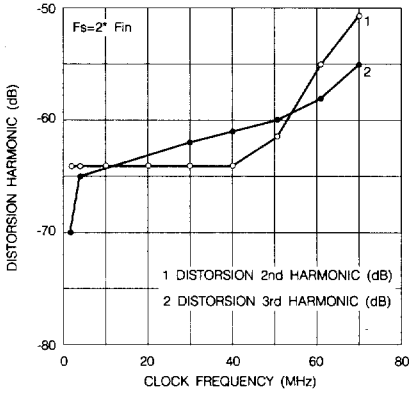


Figure 10 : Distortion 2nd and 3 ns harmonics vs. input frequency.

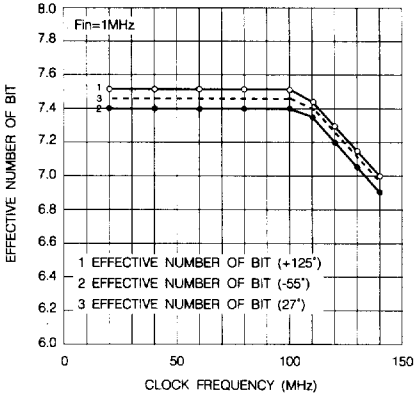


Figure 11 : Number of effective bits vs. sampling rate.

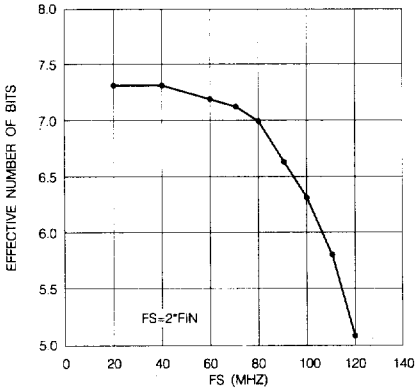


Figure 12 : Number of effective bits vs. clock frequency.

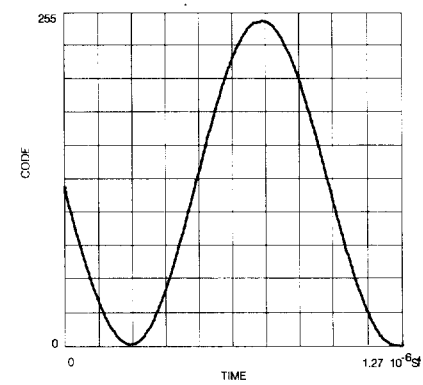


Figure 13 : Reconstructed waveform 2 MHz sampling rate, 1 MHz input frequency.

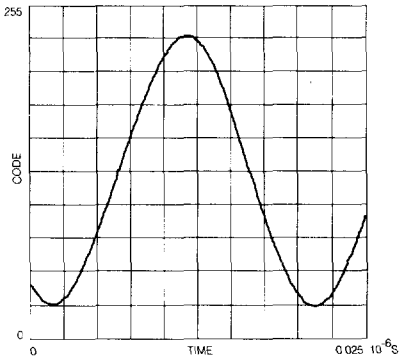


Figure 14 : Reconstructed waveform 100 MHz sampling rate, 50 MHz input frequency.

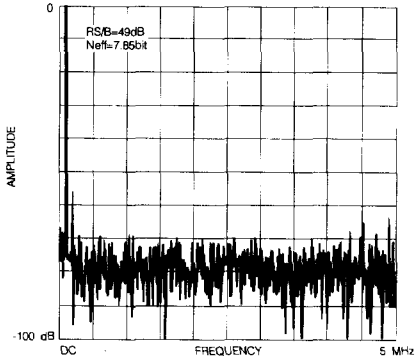


Figure 15 : 1024 point FFT of TS 8378 output at 10 MHz sampling rate, 1 MHz input frequency.

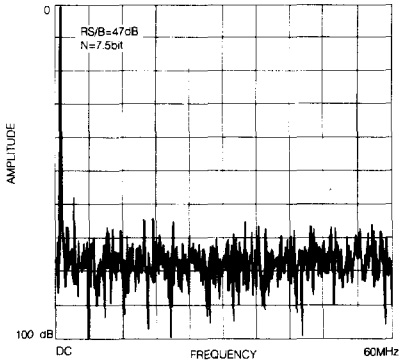


Figure 16 : 1024 point FFT of TS 8378 output at 120 MHz sampling rate, 1 MHz input frequency.

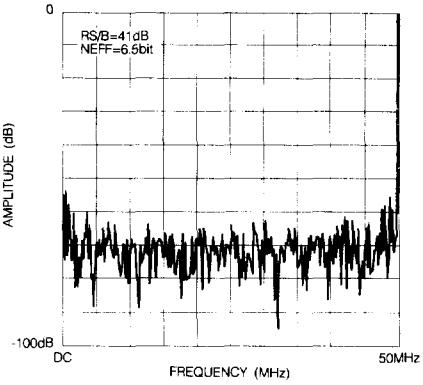


Figure 17 : 1024 point FFT of TS 8378 output at 100 MHz sampling rate, 50 MHz input frequency.

DEFINITION OF TERMS

Signal-to-noise ratio (SNR)

determined by FFT analysis,

$$SNR = 10.\log \left[\frac{P(F_{IN})}{P_n}\right] = 10.\log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)}\right] j \neq F_{in}$$

with :

- $P(F_{IN})$ spectral power of the input frequency F_{IN},
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN},
- A(j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD)

determined by FFT analysis,

$$THD = 10.\log \left[\frac{P(F_{IN})}{P_{hn}}\right] = 10.\log \left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})}\right] \text{ with } k \geqslant 2$$

with : P_{hn} harmonic noise power, which is defined as the sum of the powers of all harmonics of F_{IN}.

Number of effective bits (N_{eff})

determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e)

$$G_e = \frac{G - G_O}{G_O}$$

with :

- G_O slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL)

Measured after trimming the offset and gain errors to zero.

The integral nonlinearity for an output code i, INL (i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

The ADC integral nonlinearity INL is the maximum value of all |INL(i)|.

Differential nonlinearity (DNL)

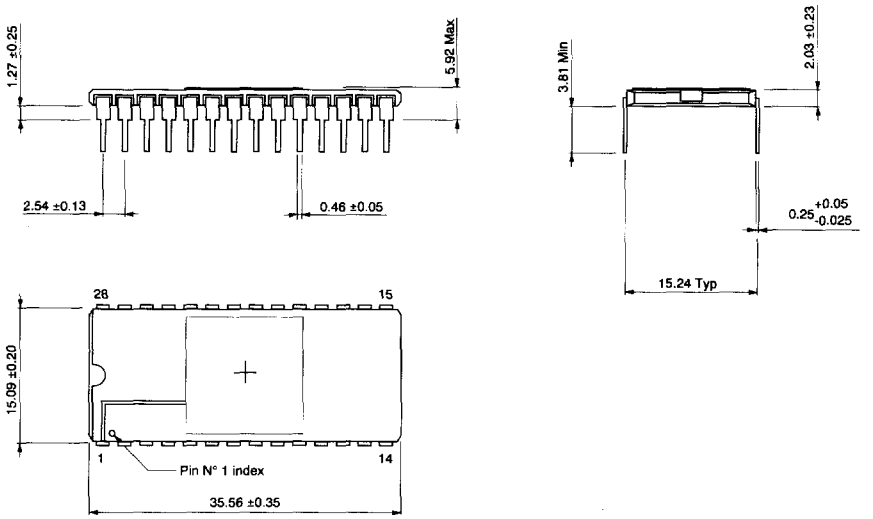
Measured after trimming the offset and gain errors to zero.

The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal LSB step size.

The ADC differential nonlinearity DNL is the maximum value of all |DNL(i)|.

MECHANICAL PACKAGE DATA

DIL 28 - CERAMIC SIDE BRAZED PACKAGE (Dimensions in mm)



DIE MECHANICAL INFORMATION : JTS 8378

Pad layout : V563

Pad size : 0.120 x 0.120 mm

Die size : 4.030 x 6.430 mm

Die thickness : 380 μm

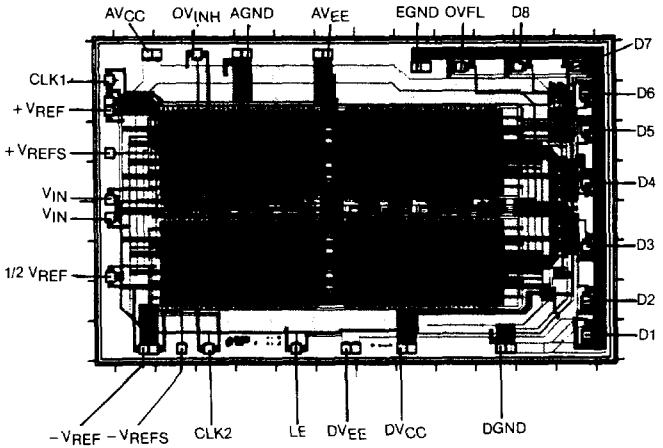
Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

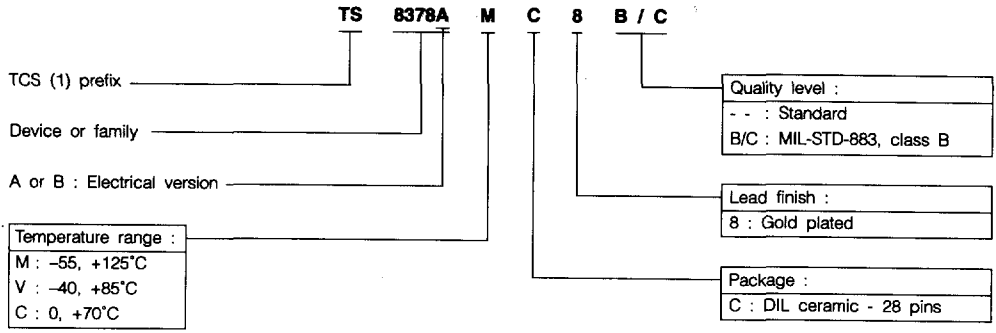
Qualification lot package : DIL 28

Back side potential : AV_{EE}

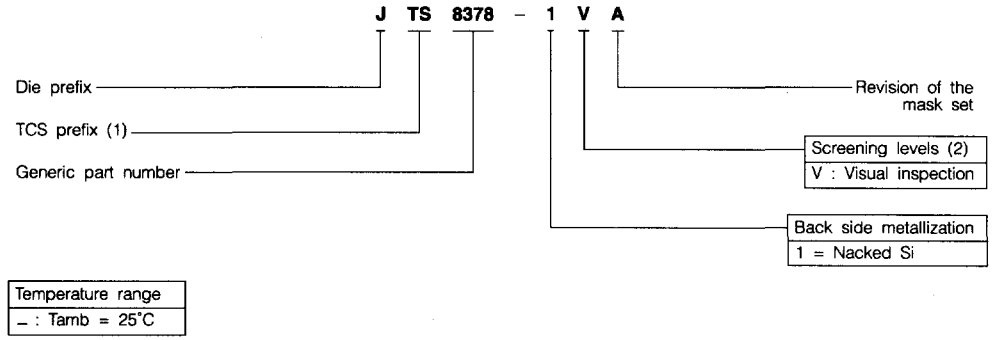


ORDERING INFORMATION

Packaged device



Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sales office.