HB54A5129F1-A75B/B75B/10B

512 MB Registered DDR SDRAM DIMM
64-Mword × 72-bit, 1-Bank Module
(18 pcs of 64 M × 4 Components)

HITACHI

ADE-203-1138 (Z)
Preliminary
Rev. 0.0
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Description

The HB54A5129F1 is a 64M × 72 × 1-bank Double Data Rate (DDR) SDRAM Module, mounted 18 pieces of 256-Mbit DDR SDRAM (HM5425401BTT) sealed in TSOP package, 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). Read and write operations are performed at the cross points of the CK and the $\overline{CK}$. This high speed data transfer is realized by the 2-bit prefetch piplined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 184-pin socket type package (dual lead out)
  - Outline: 133.35 mm (Length) × 43.18 mm (Height) × 4.00 mm (Thickness)
  - Lead pitch: 1.27 mm
- 2.5 V power supply (V_{CC}/V_{CCQ})
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 143 MHz/133 MHz/125 MHz (max)
- Data inputs and outputs are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2/4/8
  - Burst read stop capability

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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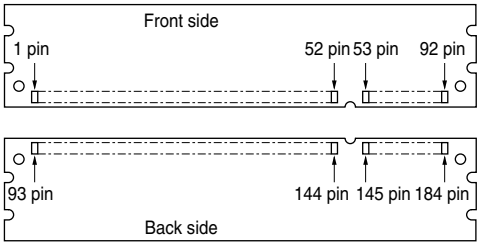
- Programmable burst sequence
  - — Sequential
  - — Interleave
- Start addressing capability
  - — Even and Odd
- Programmable $\overline{\text{CAS}}$ latency: 3/3.5
- 8192 refresh cycles: 7.8 μs (8192 row/64 ms)
- 2variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	$\overline{\text{CAS}}$ latency	Package	Contact pad
HB54A5129F1-A75B*[1]	143 MHz	3.5	184-pin dual lead out socket type	Gold
HB54A5129F1-B75B*[2]	133 MHz	3.5		
HB54A5129F1-10B*[2]	125 MHz	3.5		

Notes: 1. 133 MHz operation at $\overline{\text{CAS}}$ latency = 3.
2. 100 MHz operation at $\overline{\text{CAS}}$ latency = 3.

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DM8/DQS17
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	CB6
5	DQS0	51	CB3	97	DM0/DQS9	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	$\overline{RESET}$	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DM1/DQS10	153	DQ44
16	NC	62	V_{CCQ}	108	V_{CC}	154	$\overline{RAS}$
17	NC	63	$\overline{WE}$	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	$\overline{CAS}$	111	NC	157	$\overline{S0}$
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V_{CCQ}	76	NC	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{CCQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	WP	136	V_{CCQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	$\overline{CK0}$	184	V_{CCSPD}

Pin Description

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9, A11
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
$\overline{S0}$	Chip select
CKE0	Clock enable
CK0	Clock input
$\overline{CK0}$	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8/DQS9 to DQS17	Input and output data strobe
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
WP	Write protect for serial PD
SA0 to SA2	Serial address input
V_{CC}	Power for internal circuit
V_{CCQ}	Power for DQ circuit
V_{CCSPD}	Power for serial EEPROM
V_{REF}	Input reference voltage
V_{SS}	Ground
V_{CCID}	V_{CC} indentication flag
$\overline{RESET}$	Reset pin (forces register inputs low)
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	1	1	07	SDRAM DDR
3	Number of row address	0	0	0	0	1	1	0	1	0D	13
4	Number of column address	0	0	0	0	1	0	1	1	0B	11
5	Number of DIMM banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width continuation	0	0	0	0	0	0	0	0	00	0 (+)
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04	SSTL 2.5 V
9	DDR SDRAM cycle time, CL = X -A75B	0	1	1	1	0	0	0	0	70	CL = 2.5*[5]
	-B75B	0	1	1	1	0	1	0	1	75	
	-10B	1	0	0	0	0	0	0	0	80	
10	SDRAM access from clock (t_{AC}) -A75B/B75B	0	1	1	1	0	0	0	0	70	0.7 ns*[5]
	-10B	1	0	0	0	0	0	0	0	80	0.8 ns*[5]
11	DIMM configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	7.8 µs Self refresh
13	Primary SDRAM width	0	0	0	0	0	1	0	0	04	× 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04	× 4
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0E	2, 4, 8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
18	SDRAM device attributes: $\overline{CAS}$ latency	0	0	0	0	1	1	0	0	0C	2/2.5
19	SDRAM device attributes: $\overline{CS}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{WE}$ latency	0	0	0	0	0	0	1	0	02	1
21	SDRAM module attributes	0	0	1	0	0	1	1	0	26	Registered
22	SDRAM device attributes: General	0	0	0	0	0	0	0	0	00	± 0.2 V
23	Minimum clock cycle time at CLX - 0.5 -A75B	0	1	1	1	0	1	0	1	75	CL = 2*[5]
	-B75B/10B	1	0	1	0	0	0	0	0	A0	
24	Maximum data access time (t_{AC}) from clock at CLX - 0.5 -A75B/B75B	0	1	1	1	0	0	0	0	70	0.7 ns*[5]
	-10B	1	0	0	0	0	0	0	0	80	0.8 ns*[5]
25	Minimum clock cycle time at CLX - 1	0	0	0	0	0	0	0	0	00	
26	Maximum data access time (t_{AC}) from clock at CLX - 1	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time (t_{RP})	0	1	0	1	0	0	0	0	50	20 ns
28	Minimum row active to row active delay (t_{RRD})	0	0	1	1	1	1	0	0	3C	15 ns
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	0	1	0	1	0	0	0	0	50	20 ns
30	Minimum active to precharge time (t_{RAS}) -A75B/B75B	0	0	1	0	1	1	0	1	2D	45 ns
	-10B	0	0	1	1	0	0	1	0	32	50 ns
31	Module bank density	1	0	0	0	0	0	0	0	80	1 bank 512MB

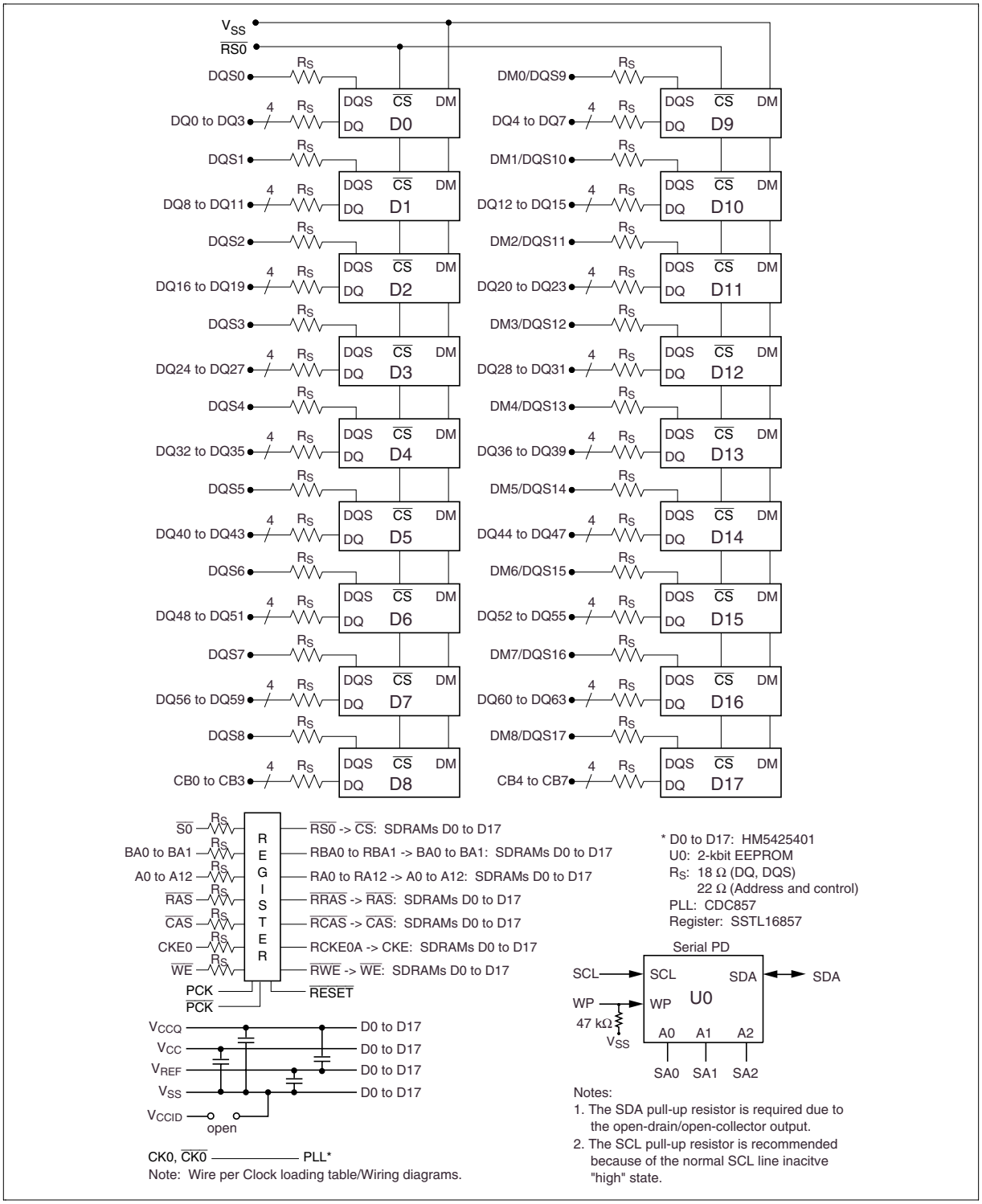
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
32	Address and command setup time before clock (t_{IS}) -A75B/B75B	1	0	1	1	0	0	0	0	B0	1.1 ns*5
	-10B	1	1	0	0	0	0	0	0	C0	1.2 ns*5
33	Address and command hold time after clock (t_{IH}) -A75B/B75B	1	0	1	1	0	0	0	0	B0	1.1 ns*5
	-10B	1	1	0	0	0	0	0	0	C0	1.2 ns*5
34	Data input setup time before clock (t_{DS}) -A75B/B75B	0	1	0	1	0	0	0	0	50	0.5 ns*5
	-10B	0	1	1	0	0	0	0	0	60	0.6 ns*5
35	Data input hold time after clock (t_{DH}) -A75B/B75B	0	1	0	1	0	0	0	0	50	0.5 ns*5
	-10B	0	1	1	0	0	0	0	0	60	0.6 ns*5
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD revision	0	0	0	0	0	0	0	0	00	Initial
63	Checksum for bytes 0 to 62 -A75B	0	0	0	1	0	1	1	0	16	22
	-B75B	0	1	0	0	0	1	1	0	46	70
	-10B	1	0	1	1	0	1	1	0	B6	182
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Module part number	0	1	0	0	1	0	0	0	48	H
74	Module part number	0	1	0	0	0	0	1	0	42	B
75	Module part number	0	0	1	1	0	1	0	1	35	5
76	Module part number	0	0	1	1	0	1	0	0	34	4
77	Module part number	0	1	0	0	0	0	0	1	41	A
78	Module part number	0	0	1	1	0	1	0	1	35	5
79	Module part number	0	0	1	1	0	0	0	1	31	1
80	Module part number	0	0	1	1	0	0	1	0	32	2
81	Module part number	0	0	1	1	1	0	0	1	39	9

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
82	Module part number	0	1	0	0	0	1	1	0	46	F
83	Module part number	0	0	1	1	0	0	0	1	31	1
84	Module part number	0	0	1	0	1	1	0	1	2D	—
85	Module part number -A75B	0	1	0	0	0	0	0	1	41	A
	-B75B	0	1	0	0	0	0	1	0	42	B
	-10B	0	0	1	1	0	0	0	1	31	1
86	Module part number -A75B/B75B	0	0	1	1	0	1	1	1	37	7
	-10B	0	0	1	1	0	0	0	0	30	0
87	Module part number -A75B/B75B	0	0	1	1	0	1	0	1	35	5
	-10B	0	1	0	0	0	0	1	0	42	B
88	Module part number -A75B/B75B	0	1	0	0	0	0	1	0	42	B
	-10B	0	0	1	0	0	0	0	0	20	(Space)
89 to 90	Module part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number	*3									
99 to 127	Manufacturer specific data	*4									

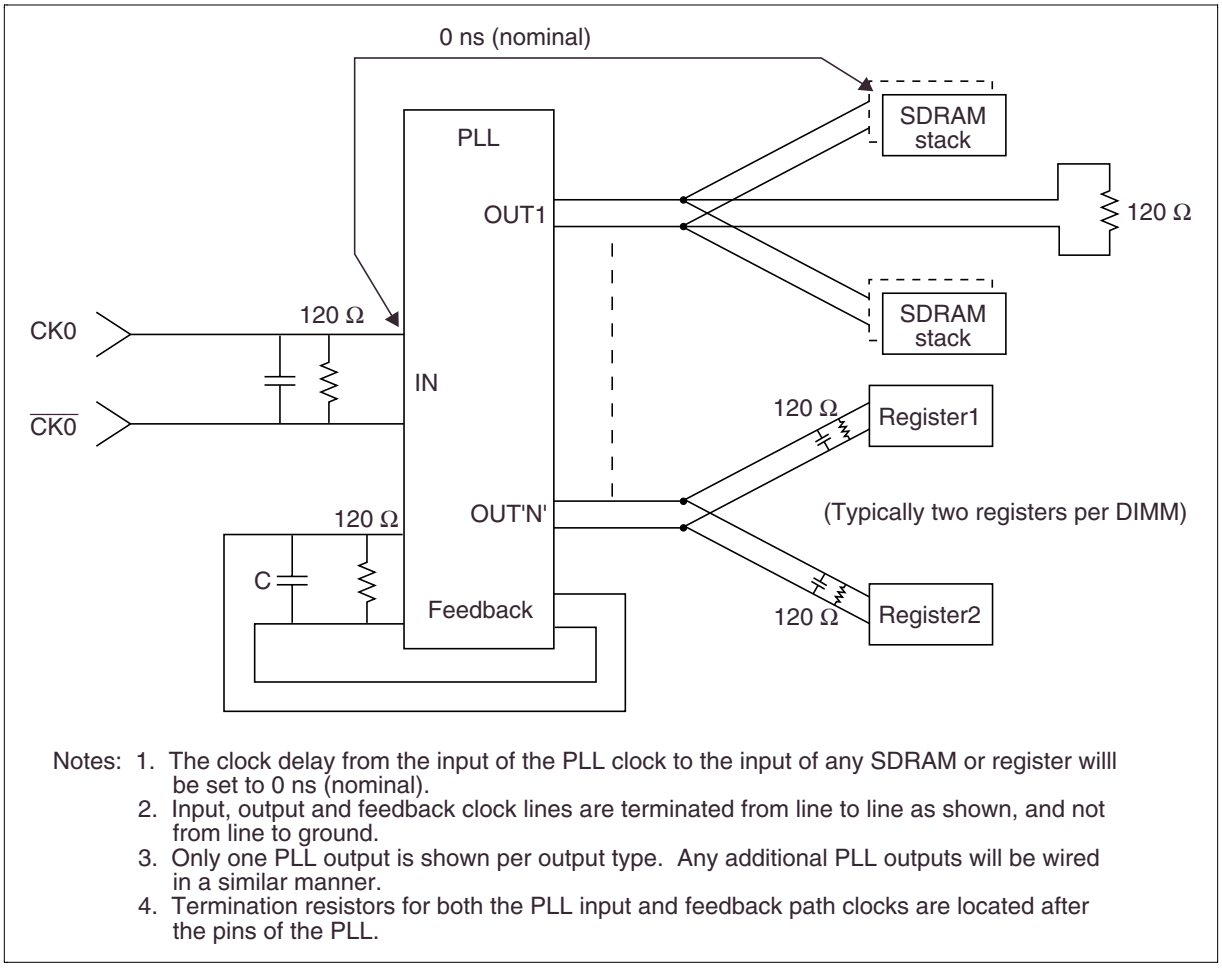
Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High” These SPD are based on JEDEC Committee Ballot JC-42.5-99-129.

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 127 are not defined (“1” or “0”).
5. These specifications are defined based on component specification, not module.

Block Diagram



Differential Clock Net Wiring (CK0, $\overline{CK0}$)



Notes: 1. The clock delay from the input of the PLL clock to the input of any SDRAM or register willl be set to 0 ns (nominal).
2. Input, output and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for both the PLL input and feedback path clocks are located after the pins of the PLL.

Pin Functions (1)

CK (CLK), $\overline{CK}$ ($\overline{CLK}$) (input pin): The CK and the $\overline{CK}$ are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the V_{REF} level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the $\overline{CK}$. When a write operation, DMs and DQs are referred to the cross point of the DQS and the V_{REF} level. DQSs for write operation are referred to the cross point of the CK and the $\overline{CK}$.

$\overline{S}$ ($\overline{CS}$) (input pin): When $\overline{S}$ is Low, commands and data can be input. When $\overline{S}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the V_{REF} level in a bank active command cycle. Column address (AY0 to AY9, AY11) is loaded via the A0 to the A9, the A11 at the cross point of the CK rising edge and the V_{REF} level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0/BA1 (input pin): BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CK cycle (= L_{CKEPW}) at least, that is, if CKE changes at the cross point of the CK rising edge and the V_{REF} level with proper setup time t_{IS}, at the next CK rising edge CKE level must be kept with proper hold time t_{IH}.

Pin Functions (2)

DQ, CB (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

V_{CC} and V_{CCQ} (power supply pins): 2.5 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)

V_{CCSPD} (power supply pin): 2.5 V is applied (For serial EEPROM).

V_{SS} (power supply pin): Ground is connected.

$\overline{\text{RESET}}$ (input pin): LVCMOS reset input. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

Detailed Operation Part and Timing Waveforms

Refer to the HM5425161B/HM5425801B/HM5425401B Series datasheet. DM pins of component device fixed to V_{SS} level on the module board. DIMM $\overline{\text{CAS}}$ latency = Device CL + 1 for registered type.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{ss}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}, V_{CCQ}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	18	W	
Operating temperature	Topr	0 to +55	°C	
Storage temperature	Tstg	–50 to +100	°C	

Note: 1. Respect to V_{SS}

DC Operating Conditions (Ta = 0 to +55°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}, V_{CCQ}	2.3	2.5	2.7	V	1, 2
	V_{SS}	0	0	0	V	
Input reference voltage	V_{REF}	1.15	1.25	1.35	V	1
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	1
DC Input high voltage	V_{IH}	V_{REF} + 0.18	—	V_{CCQ} + 0.3	V	1, 3
DC Input low voltage	V_{IL}	–0.3	—	V_{REF} – 0.18	V	1, 4
DC Input signal voltage	V_{IN} (dc)	–0.3	—	V_{CCQ} + 0.3	V	5
DC differential input voltage	V_{SWING} (dc)	0.36	—	V_{CCQ} + 0.6	V	6

Notes: 1. All parameters are referred to V_{SS}, when measured.
2. V_{CCQ} must be lower than or equal to V_{CC}.
3. V_{IH} is allowed to exceed V_{CC} up to 4.6 V for the period shorter than or equal to 5 ns.
4. V_{IL} is allowed to outreach below V_{SS} down to –1.0 V for the period shorter than or equal to 5 ns.
5. V_{IN} (dc) specifies the allowable dc execution of each differential input.
6. V_{SWING} (dc) specifies the input differential voltage required for switching.

DC Characteristics (Ta = 0 to +55˚C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS} = 0 V)

		HB54A5129F1								
		-A75B		-B75B		-10B				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current (ACTV-PRE)	I_{CC0}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RC} = min	1, 2, 5
Operating current (ACTV-READ-PRE)	I_{CC1}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 3.5, t_{RC} = min	1, 2, 5
Idle power down standby current	I_{CC2P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	4
Idle standby current	I_{CC2N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, $\overline{CS}$ ≥ V_{IH}	4
Active power down standby current	I_{CC3P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	3
Active standby current	I_{CC3N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RAS} = max	3
Operating current (Burst read operation)	I_{CC4R}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 3.5	1, 2, 5, 6
Operating current (Burst write operation)	I_{CC4W}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 3.5	1, 2, 5, 6
Auto refresh current	I_{CC5}	—	TBD	—	TBD	—	TBD	mA	t_{RFC} = min, Input ≤ V_{IL} or ≥ V_{IH}	
Self refresh current	I_{CC6}	—	TBD	—	TBD	—	TBD	mA	Input ≥ V_{CC} – 0.2 V Input ≤ 0.2 V	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vin ≥ V_{SS}	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vout ≥ V_{SS}	
Output high voltage	V_{OH}	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V	I_{OH} (max) = –15.2 mA	
Output low voltage	V_{OL}	—	V_{TT} – 0.76	—	V_{TT} – 0.76	—	V_{TT} – 0.76	V	I_{OL} (min) = 15.2 mA	

Notes. 1. These I_{CC} data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The I_{CC} data on this table are measured with regard to t_{CK} = min in general.

Capacitance (Ta = 25°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	TBD	TBD	pF	1
Input capacitance (Command)	C_{I2}	TBD	TBD	pF	1
Data and DQS input/output capacitance (I/O)	C_O	TBD	TBD	pF	1, 2

Notes: 1. These parameters are measured on conditions: f = 100 MHz, Vout = V_{CCQ}/2, ΔVout = 0.2 V.
2. Dout circuits are disabled.

AC Characteristics (Ta = 0 to +55˚C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS} = 0 V)

		HB54A5129F1							
		-A75B		-B75B		-10B			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
System clock cycle time ($\overline{CAS}$ latency = 3)	t_{CK}	7.5	15	10	15	10	15	ns	10
($\overline{CAS}$ latency = 3.5)	t_{CK}	7	15	7.5	15	8	15	ns	
Input clock high level time	t_{CH}	TBD	—	TBD	—	TBD	—	t_{CK}	
Input clock low level time	t_{CL}	TBD	—	TBD	—	TBD	—	t_{CK}	
CLK to DQS skew	t_{DQSCK}	TBD	TBD	TBD	TBD	TBD	TBD	ns	2
DATA to CLK skew	t_{AC}	TBD	TBD	TBD	TBD	TBD	TBD	ns	2
Dout to DQS skew	t_{DQSQ}	–0.5	0.5	–0.5	0.5	–0.6	0.6	ns	3
Dout/DQS valid window	t_{DV}	0.35	—	0.35	—	0.35	—	t_{CK}	4
DQS valid window	t_{DQSV}	0.35	—	0.35	—	0.35	—	t_{CK}	4
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Dout-High impedance delay from CLK/$\overline{CLK}$	t_{HZ}	TBD	TBD	TBD	TBD	TBD	TBD	ns	5
Dout-Low impedance delay from CLK/$\overline{CLK}$	t_{LZ}	TBD	TBD	TBD	TBD	TBD	TBD	ns	6
DQ input pulse width	t_{DIPW}	1.7	—	1.7	—	2	—	ns	7
Data to data strobe setup time	t_{DS}	0.5	—	0.5	—	0.6	—	ns	8
Data to data strobe hold time	t_{DH}	0.5	—	0.5	—	0.6	—	ns	8
Clock to DQS write preamble setup time	t_{WPRES}	TBD	—	TBD	—	TBD	—	ns	
Clock to DQS write preamble hold time	t_{WPREH}	TBD	—	TBD	—	TBD	—	t_{CK}	
DQS last edge to High-Z time (DQS write postamble)	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	9
Clock to the DQS first rising edge for write delay	t_{DQSS}	TBD	TBD	TBD	TBD	TBD	TBD	t_{CK}	

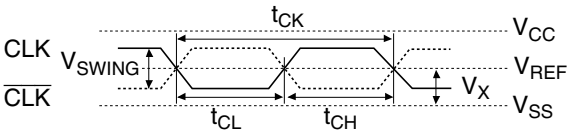
		HB54A5129F1							
		-A75B		-B75B		-10B			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
DQS falling edge to CLK setup time	t_{DSS}	TBD	—	TBD	—	TBD	—	t_{CK}	
DQS falling edge hold time to CLK	t_{DSH}	TBD	—	TBD	—	TBD	—	t_{CK}	
DQS high pulse width (DQS write)	t_{DQSH}	0.35	—	0.35	—	0.35	—	t_{CK}	
DQS low pulse width (DQS write)	t_{DQSL}	0.35	—	0.35	—	0.35	—	t_{CK}	
Input command and address setup time	t_{IS}	TBD	—	TBD	—	TBD	—	ns	8
Input command and address hold time	t_{IH}	TBD	—	TBD	—	TBD	—	ns	8
Active command period	t_{RC}	65	—	65	—	70	—	ns	
Auto refresh to active/Auto refresh command cycle	t_{RFC}	75	—	75	—	80	—	ns	
Active to Precharge command period	t_{RAS}	45	120000	45	120000	50	120000	ns	
Active to column command period	t_{RCD}	20	—	20	—	20	—	ns	
Last data in to precharge	t_{WR}	TBD	—	TBD	—	TBD	—	ns	
Precharge to active command period	t_{RP}	20	—	20	—	20	—	ns	
Active to active command period	t_{RRD}	15	—	15	—	15	—	ns	
Average periodic refresh interval	t_{REF}	—	7.8	—	7.8	—	7.8	µs	

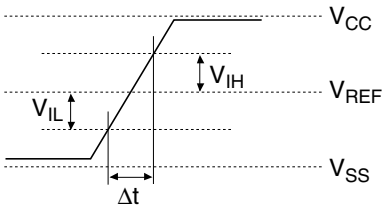
Notes. 1. On all AC measurements, we assume the test conditions shown in the next page. For timing parameter definitions, see 'Timing Waveforms' section.

2. This parameter defines the signal transition delay from the cross point of CLK and $\overline{CLK}$. The signal transition is defined to occur when the signal level crossing V_{TT}.
3. The timing reference level is V_{TT}.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing V_{TT}.
5. t_{HZ} is defined as Dout transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CLK and $\overline{CLK}$. This parameter is not referred to a specific Dout voltage level, but specify when the device output stops driving.
6. t_{LZ} is defined as Dout transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific Dout voltage level, but specify when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing V_{REF}.
8. The timing reference level is V_{REF}.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
10. t_{CK} max is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
11. V_{CC} is assumed to be 2.5 V ± 0.2 V. V_{CC} power supply variation per cycle expected to be less than 0.4 V/400 cycle.

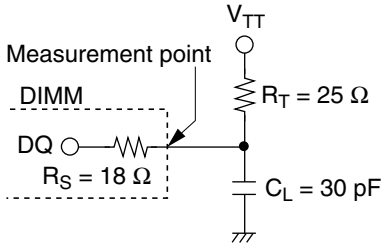
Test Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input reference voltage	V_{REF}	1.15	1.25	1.35	V
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
AC input high voltage	V_{IH} (ac)	V_{REF} + 0.35	—	—	V
AC input low voltage	V_{IL} (ac)	—	—	V_{REF} – 0.35	V
AC differential input high voltage	V_{SWING} (ac)	0.7	—	V_{CCQ} + 0.6	V
AC differential cross point voltage	V_X (ac)	V_{REF} – 0.2	V_{REF}	V_{REF} + 0.2	V
Input signal slew rate	SLEW	—	1	—	V/ns





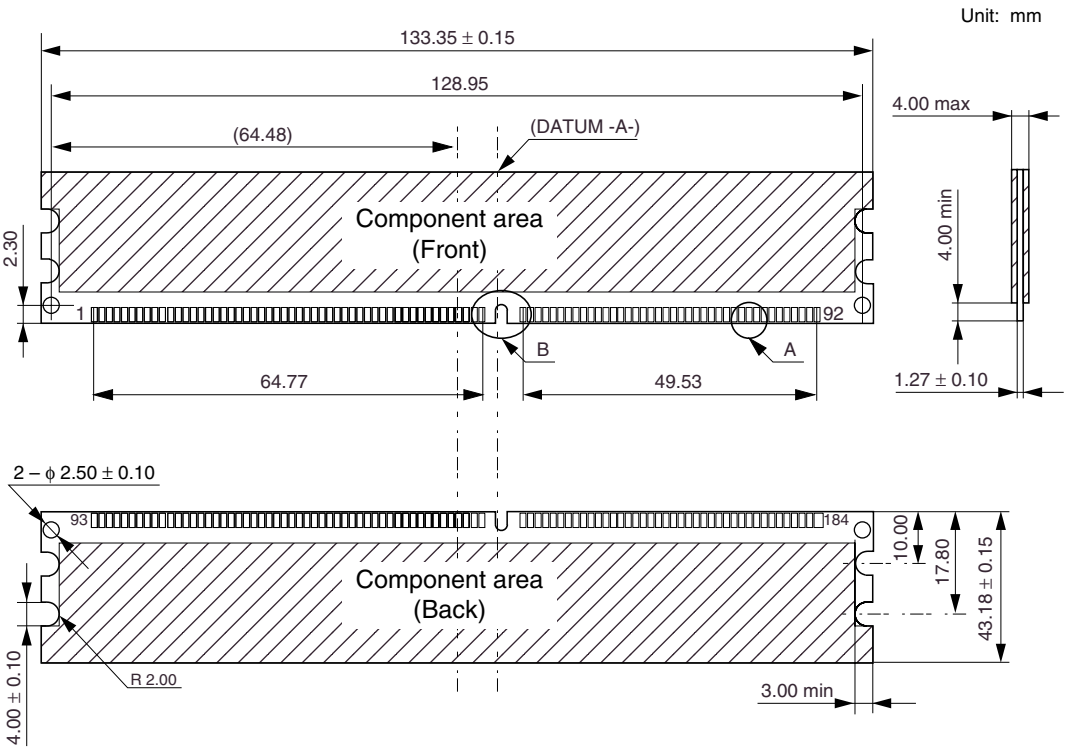
$SLEW = (V_{IH}\ (ac) - V_{IL}\ (ac))/\Delta t$



Timing Parameter Measured in Clock Cycle for Registered DIMM

		Number of clock cycle	
Parameter	**Symbol**	**Min**	**Max**
Write to pre-charge command delay (same bank)	t_{WPD}	3 + BL/2	
Read to pre-charge command delay (same bank)	t_{RPD}	BL/2	
Write to read command delay (to input all data)	t_{WRD}	2 + BL/2	
Burst stop command to write command delay ($\overline{CAS}$ latency = 3)	t_{BSTW}	2	
($\overline{CAS}$ latency = 3.5)	t_{BSTW}	3	
Burst stop command to DQ High-Z ($\overline{CAS}$ latency = 3)	t_{BSTZ}	3	
($\overline{CAS}$ latency = 3.5)	t_{BSTZ}	3.5	
Read command to write command delay (to output all data) ($\overline{CAS}$ latency = 3)	t_{RWD}	2 + BL/2	
($\overline{CAS}$ latency = 3.5)	t_{RWD}	3 + BL/2	
Pre-charge command to High-Z ($\overline{CAS}$ latency = 3)	t_{HZP}	3	
($\overline{CAS}$ latency = 3.5)	t_{HZP}	3.5	
Write command to data in latency	t_{WCD}	2	
Write recovery	t_{WR}	1	
Register set command to active or register set command	t_{MRD}	2	
Self refresh exit to non-read command	t_{SNR}	10	
Self refresh exit to read command	t_{SRD}	200	
Power down entry	t_{PDEN}		1
Power down exit to command input	t_{PDEX}		1
CKE minimum pulse width	t_{CKEPW}	1	

Physical Outline



Note: Tolerance on all dimensions ± 0.13 unless otherwise specified.

FD400170W

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