

74164, LS164

Shift Registers

8-Bit Serial-In Parallel-Out Shift Register
Product Specification

Logic Products

FEATURES

- Gated serial Data inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data inputs

DESCRIPTION

The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one set-up time before the rising clock edge. A LOW level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74164	36MHz	37mA
74LS164	36MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74164N, N74LS164N
Plastic SO	N74LS164D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

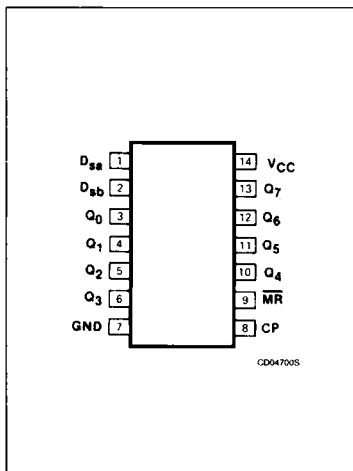
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1uI	1LSuI
All	Outputs	5uI	10LSuI

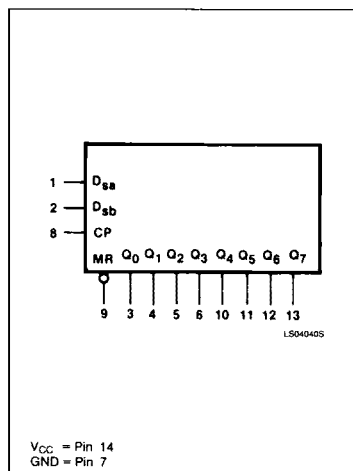
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

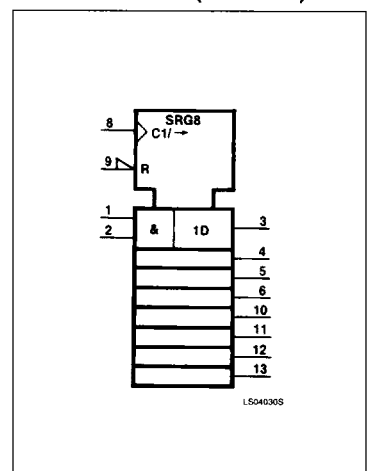
PIN CONFIGURATION



LOGIC SYMBOL



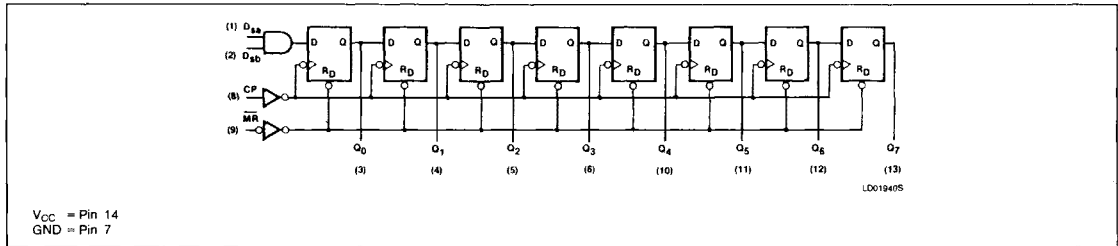
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	MR	CP	D _{sa}	D _{sb}	Q ₀	Q ₁ — Q ₆	Q ₇
Reset (clear)	L	X	X	X	L	L — L	L
Shift	H	↑	l	l	L	q ₀ — q ₆	q ₆
	H	↑	l	h	L	q ₀ — q ₆	q ₆
	H	↑	h	l	L	q ₀ — q ₆	q ₆
	H	↑	h	h	H	q ₀ — q ₆	q ₆

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
- Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the
- q = LOW-to-HIGH Clock transition.
- X = Don't care.
- ↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-400			-400	μA
I _{OL}	LOW-level output current			8			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

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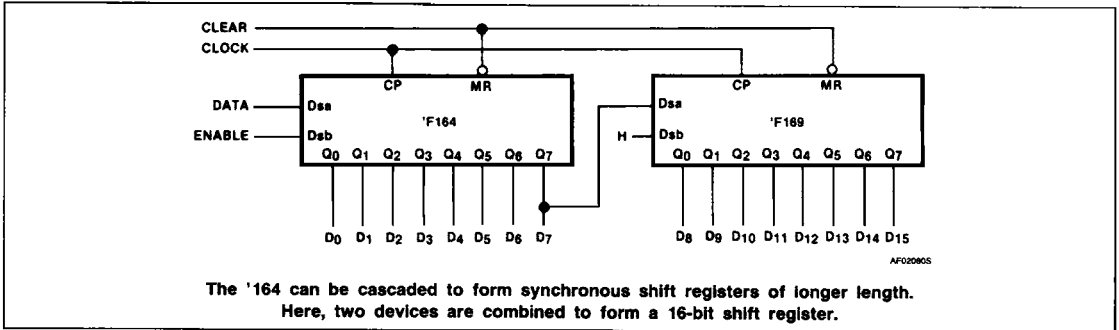
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74164			74LS164			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.35	0.5		V
		I _{OL} = 4mA (74LS)			0.25	0.4		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						mA
		V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	9		-27.5	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		37	54		16	27	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION DIAGRAM



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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 800\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum shift frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		27 32		27 32	ns
t_{PHL} Propagation delay MR to output	Waveform 2		36		36	ns
t_{PLH} Propagation delay t_{PHL} Clock to output	$C_L = 50\text{pF}$ for these parameters	Waveform 1	30 37			ns
t_{PHL} Propagation delay MR to output		Waveform 2	42			ns

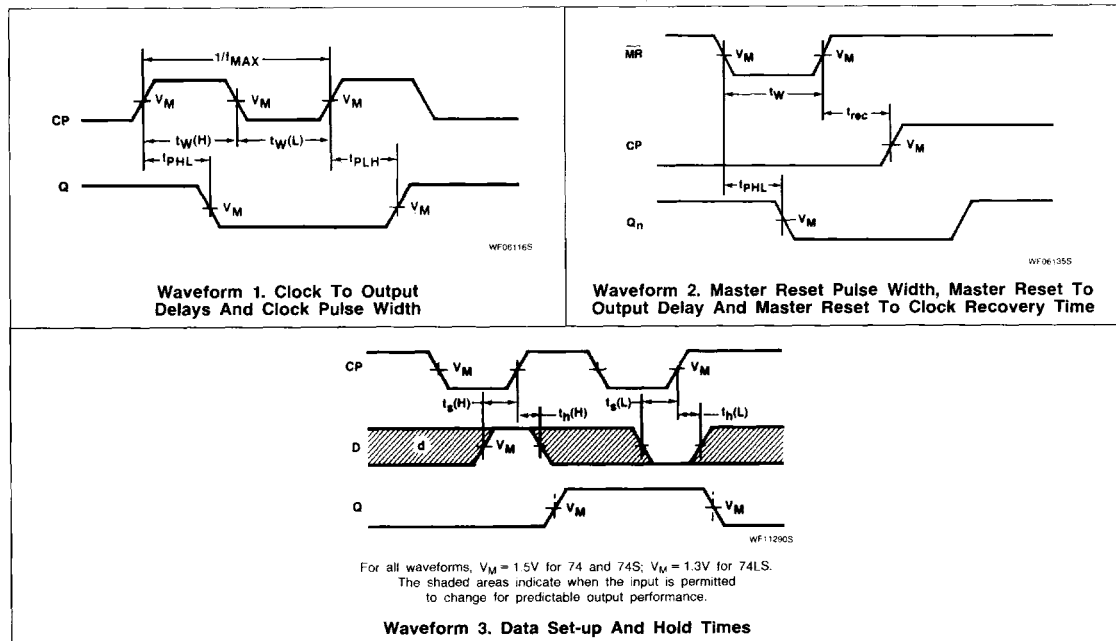
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_w Clock pulse width	Waveform 1	20		20		ns
t_w MR pulse width	Waveform 2	20		20		ns
t_s Set-up time data to clock	Waveform 3	15		15		ns
t_h Hold time data to clock	Waveform 3	5.0		5.0		ns
t_{rec} MR to clock recovery time	Waveform 2	30		30		ns

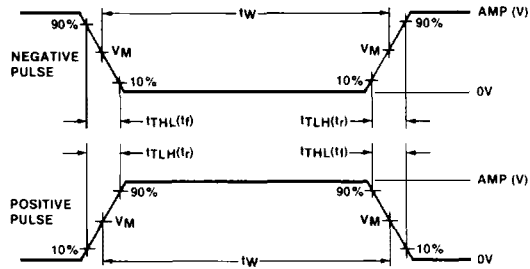
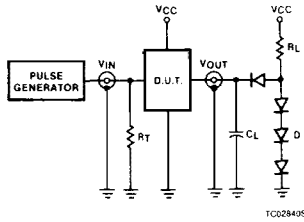
AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns