

DATA SHEET

74LVC00A

Quad 2-input NAND gate

Product specification
Supersedes data of 2003 May 07

2003 Sep 04

Quad 2-input NAND gate

74LVC00A

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC00A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74LVC00A provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.1	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	15	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND to } V_{CC}$.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level;
L = LOW voltage level.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC00AD	−40 to +125 °C	14	SO14	plastic	SOT108-1
74LVC00ADB	−40 to +125 °C	14	SSOP14	plastic	SOT337-1
74LVC00APW	−40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC00ABQ	−40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V _{CC}	supply voltage

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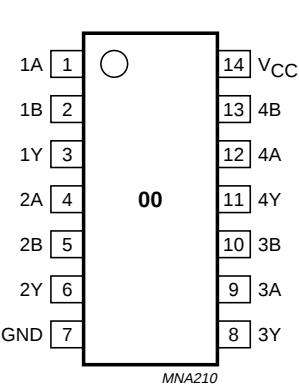
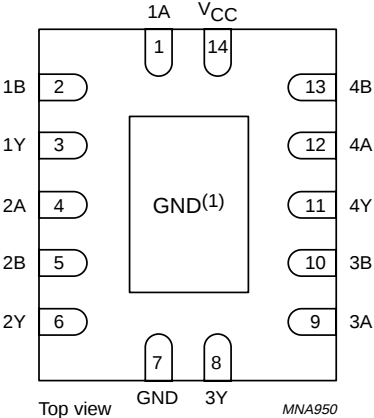


Fig.1 Pin configuration SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

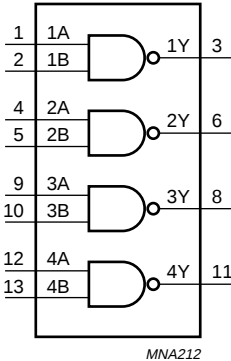


Fig.3 Logic symbol.

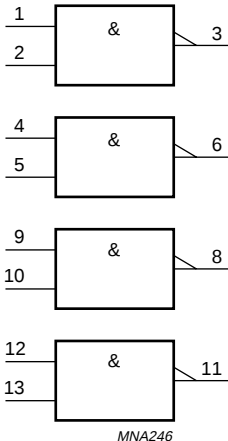
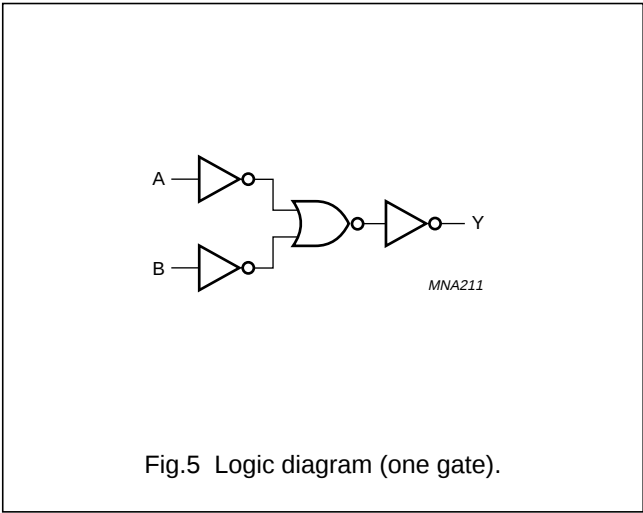


Fig.4 Logic symbol (IEEE/IEC).

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V _I	input voltage		0	5.5	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	operating ambient temperature		−40	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 1.2 to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		−0.5	+6.5	V
I _{IK}	input diode current	V _I < 0	−	−50	mA
V _I	input voltage	note 1	−0.5	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0	−	±50	mA
V _O	output voltage	note 1	−0.5	V _{CC} + 0.5	V
I _O	output source or sink current	V _O = 0 to V _{CC}	−	±50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		−	±100	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	power dissipation	T _{amb} = −40 to +125 °C; note 2	−	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	−	−	V
			2.7 to 3.6	2.0	−	−	V
V _{IL}	LOW-level input voltage		1.2	−	−	GND	V
			2.7 to 3.6	−	−	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −100 μA	2.7 to 3.6	V _{CC} − 0.2	−	−	V
		I _O = −12 mA	2.7	V _{CC} − 0.5	−	−	V
		I _O = −18 mA	3.0	V _{CC} − 0.6	−	−	V
V _{OL}	LOW-level output voltage	I _O = −24 mA	3.0	V _{CC} − 0.8	−	−	V
		V _I = V _{IH} or V _{IL}					
		I _O = 100 μA	2.7 to 3.6	−	−	0.2	V
		I _O = 12 mA	2.7	−	−	0.4	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	−	±0.1	±5	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	−	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} − 0.6 V; I _O = 0	2.7 to 3.6	−	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	−	−	V
			2.7 to 3.6	2.0	−	−	V
V _{IL}	LOW-level input voltage		1.2	−	−	GND	V
			2.7 to 3.6	−	−	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −100 μA	2.7 to 3.6	V _{CC} − 0.3	−	−	V
		I _O = −12 mA	2.7	V _{CC} − 0.65	−	−	V
		I _O = −18 mA	3.0	V _{CC} − 0.75	−	−	V
V _{OL}	LOW-level output voltage	I _O = −24 mA	3.0	V _{CC} − 1	−	−	V
		V _I = V _{IH} or V _{IL}					
		I _O = 100 μA	2.7 to 3.6	−	−	0.3	V
		I _O = 12 mA	2.7	−	−	0.6	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.0	−	−	±20	μA
			3.6	−	−	40	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	−	−	5000	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} − 0.6 V; I _O = 0	2.7 to 3.6	−	−		

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC CHARACTERISTICS

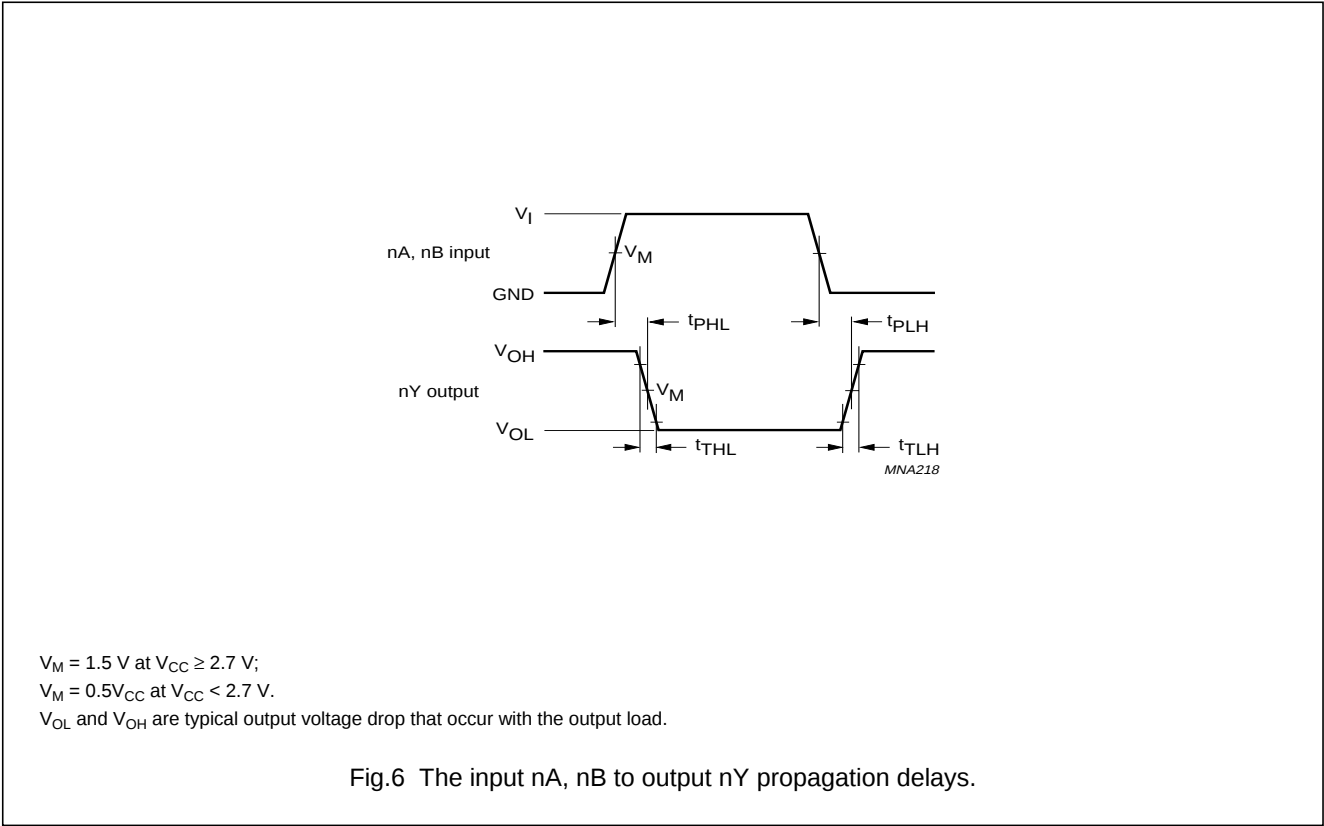
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = −40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	V _{CC} = 1.2	–	12	–	ns
			V _{CC} = 2.7	1.0	2.4	5.1	ns
			V _{CC} = 3.0 to 3.6	1.0	2.1 ⁽¹⁾	4.3	ns
t _{sk(0)}	skew	note 2	V _{CC} = 3.0 to 3.6	–	–	1.0	ns
T _{amb} = −40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	V _{CC} = 1.2	–	–	–	ns
			V _{CC} = 2.7	1.0	–	6.5	ns
			V _{CC} = 3.0 to 3.6	1.0	–	5.5	ns
t _{sk(0)}	skew	note 2	V _{CC} = 3.0 to 3.6	–	–	1.5	ns

Notes

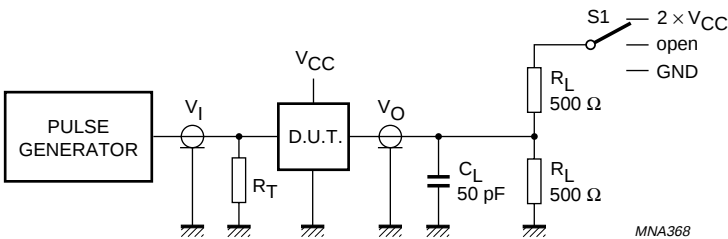
1. Typical value is measured at V_{CC} = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



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V_{CC}	V_I	t_{PLH}/t_{PHL}
1.2 V	V_{CC}	open
2.7 V	2.7 V	open
3.0 to 3.6 V	2.7 V	open

Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

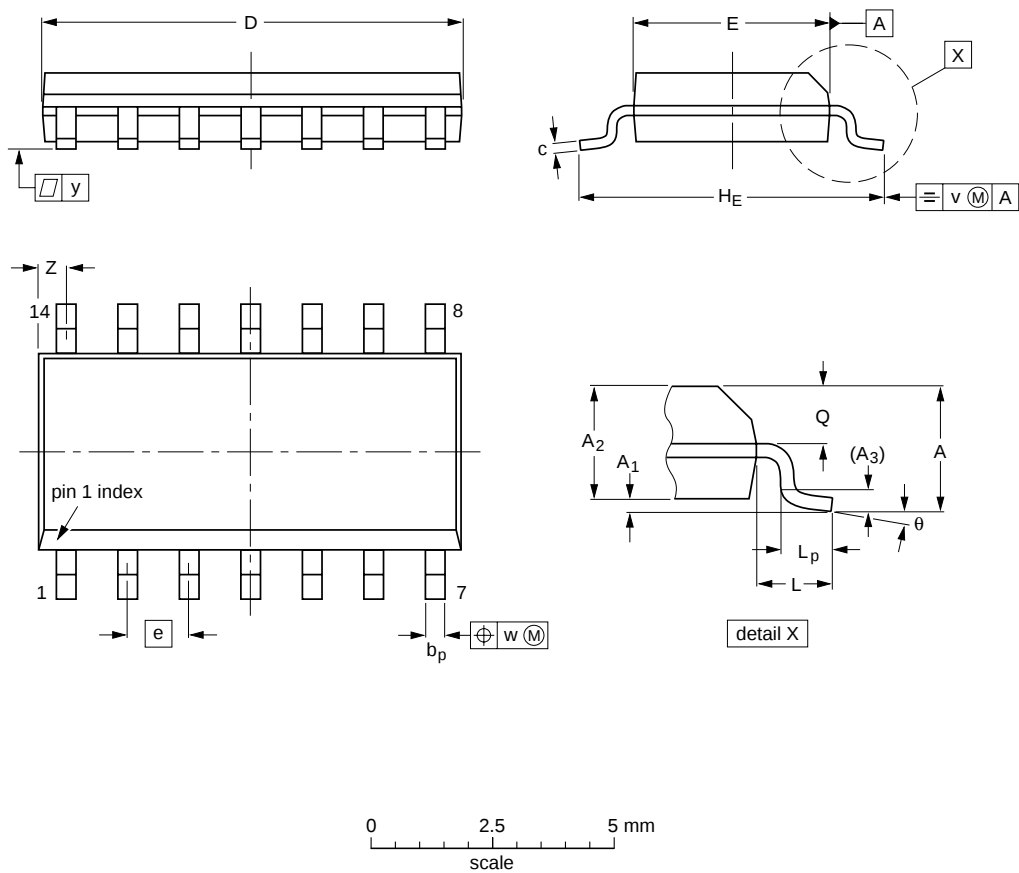
Quad 2-input NAND gate

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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

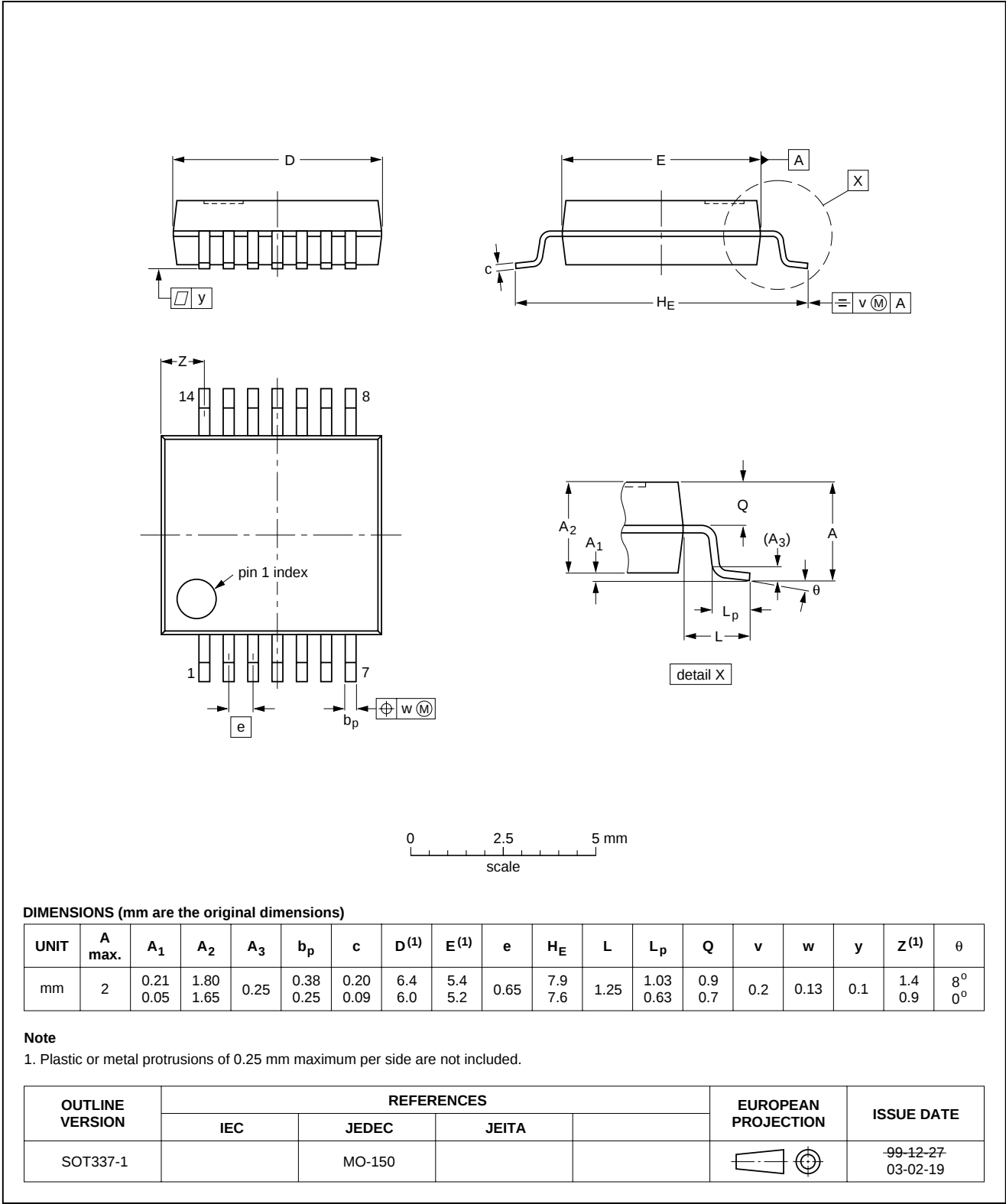
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

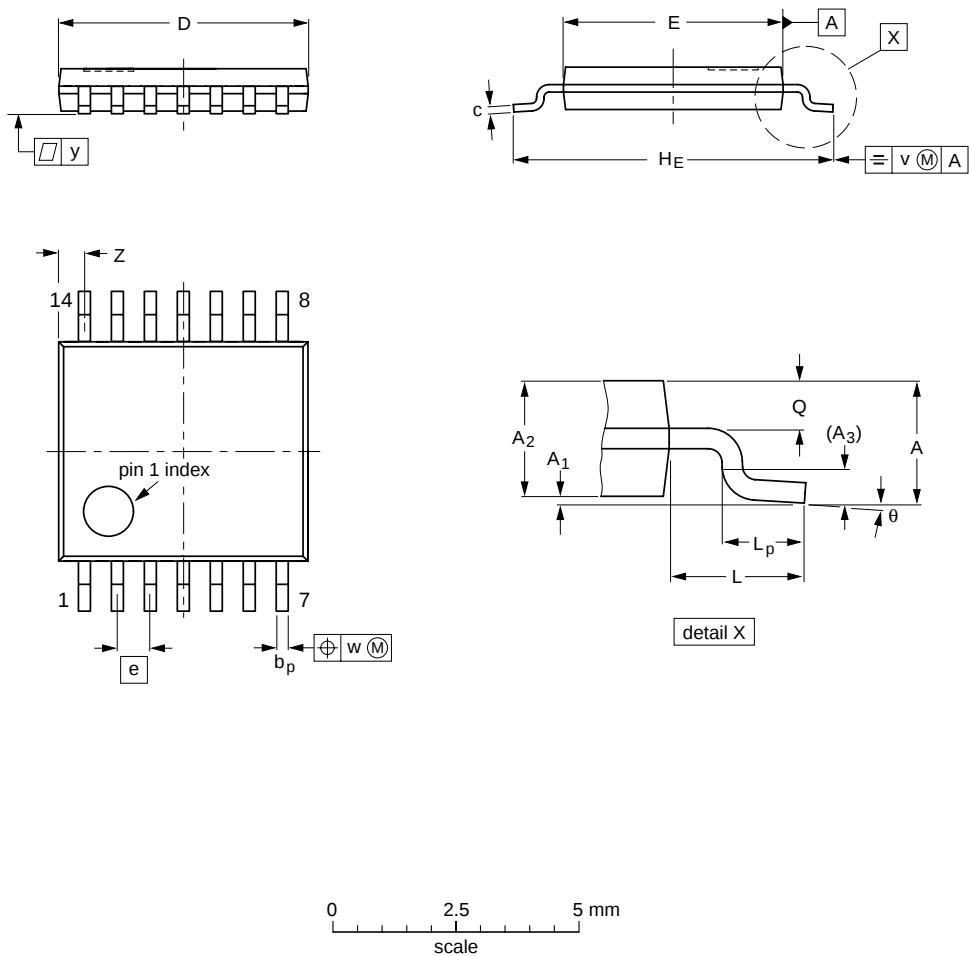


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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

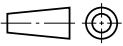


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

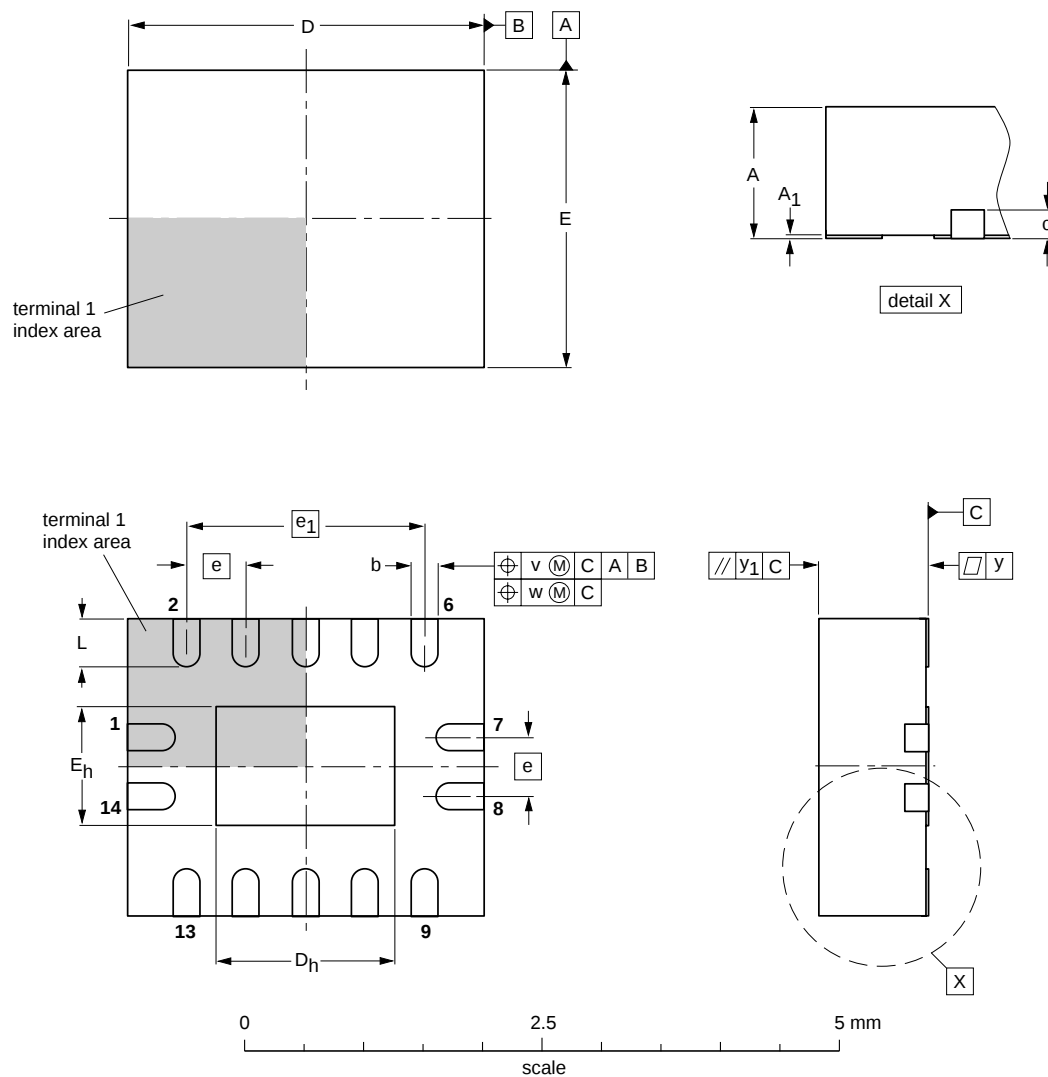
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

Quad 2-input NAND gate

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LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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