

# S71WS-R based MCP Products

## 1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM

*Data Sheet (Advance Information)*

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## 1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM



Data Sheet (Advance Information)

### Features

- Power supply voltage of 1.7 to 1.95V
- Flash access time: 80 ns
- Flash burst frequencies: 80 MHz, 104 MHz
- pSRAM Access time: 70 ns
- pSRAM burst frequency: 104 MHz
- Package:
  - 8.0 x 11.6 mm MCP
- Operating Temperature
  - –30°C to +85°C (wireless)

The S71WS-R series is a product line of stacked packages and consists of:

- One or two S29WS-R NOR flash memory die
- CellularRAM die

The products covered by this document are listed in the table below.

Flash Device	CellularRAM Density (Mb)			
	32 Mb	64 Mb	128 Mb	256 Mb (2 x 128 Mb)
S29WS512R	—	—	S71WS512RD0	S71WS512RE0
S29WS256R	—	S71WS256RC0	S71WS256RD0	—
S29WS128R	S71WS128RB0	S71WS128RC0	—	—

**Note:**

For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

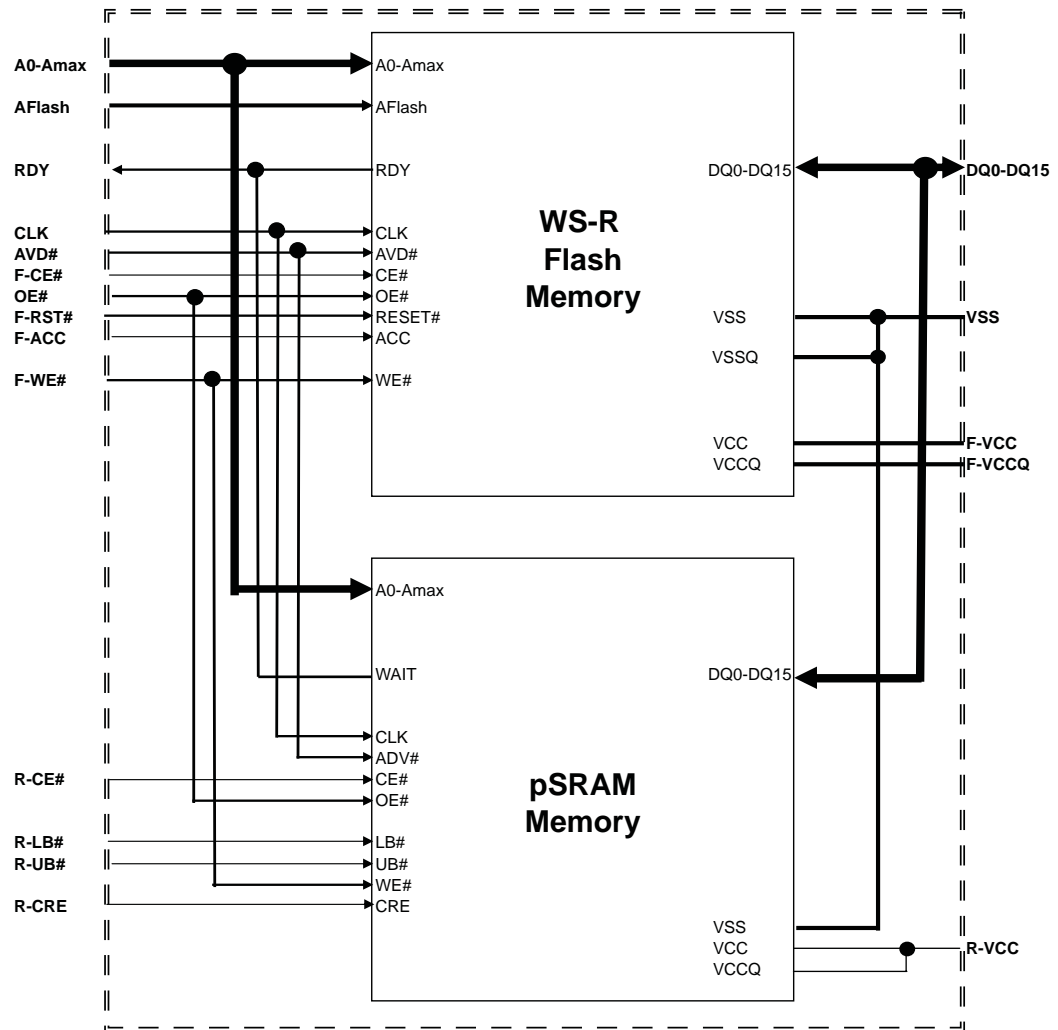
For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS-R	S29WS-R_00
128 Mb CellularRAM Type 5	custcomspec_00
128 Mb/64 Mb CellularRAM Type 2	Cellram_07
32 Mb CellularRAM Type 2	CellularRAM_08

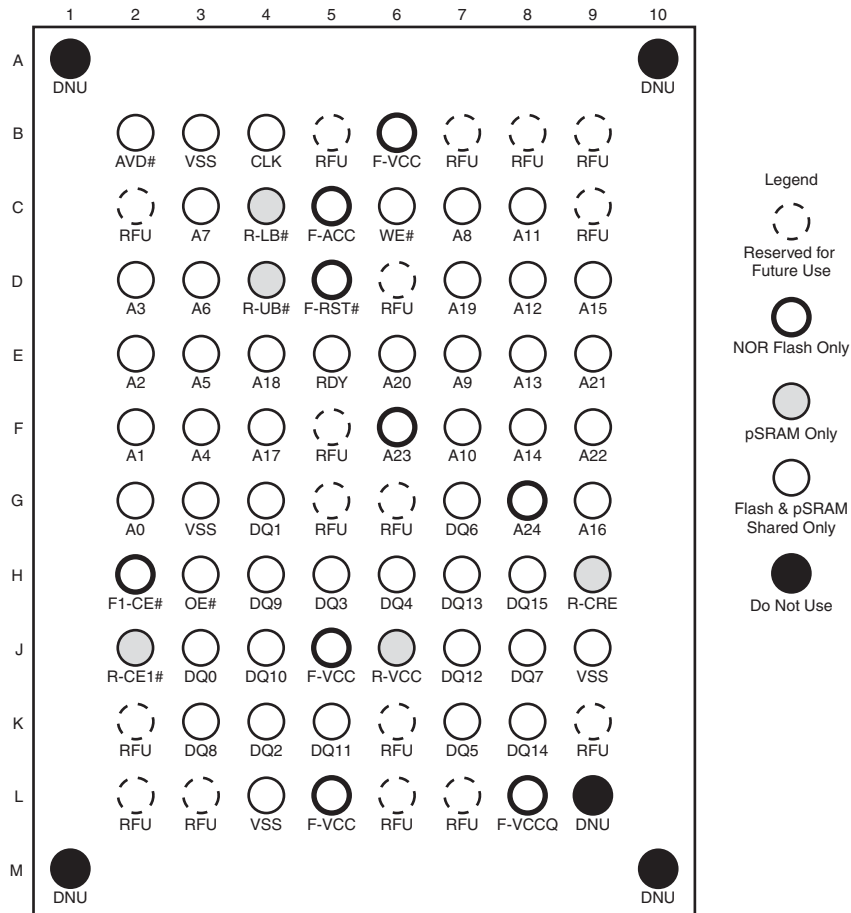
# 1. Product Selector Guide

Device	Model Number	Flash Density (Mb)	CellularRAM Density (Mb)	Flash Speed (MHz)	CellularRAM Speed (MHz)	CellularRAM Supplier	Package	Flash Boot Option								
S71WS512RE0HH3	29	512	256	104	104		84 ball MCP 8 x 11.6 x 1.4mm	Top Boot								
S71WS512RE0HH3	09							Uniform Boot								
S71WS512RD0HH3	29		128	80				Type 2	84 ball MCP 8x11.6x1.2mm	Top Boot						
S71WS512RD0HH3	2A									Uniform Boot						
S71WS512RD0HH3	09							Type 5		104	Top Boot					
S71WS512RD0HH3	0A									80	Uniform Boot					
S71WS512RD0HH3	2S									104	Top Boot					
S71WS512RD0HH3	2T									80	Uniform Boot					
S71WS512RD0HH3	0S									104	Top Boot					
S71WS512RD0HH3	0T									80	Uniform Boot					
S71WS256RD0HH3	29	256			128	104				104		Top Boot				
S71WS256RD0HH3	2A					80						Uniform Boot				
S71WS256RD0HH3	09		104	Top Boot												
S71WS256RD0HH3	0A		80	Uniform Boot												
S71WS256RC0HH3	29		64	104		Type 2	84 ball MCP 8x11.6x1.2mm	Top Boot								
S71WS256RC0HH3	2A							80	Uniform Boot							
S71WS256RC0HH3	09							104	Top Boot							
S71WS256RC0HH3	0A							80	Uniform Boot							
S71WS128RC0HH3	29							128	64			104			Top Boot	
S71WS128RC0HH3	2A											80			Uniform Boot	
S71WS128RC0HH3	09	104								Top Boot						
S71WS128RC0HH3	0A	80								Uniform Boot						
S71WS128RB0HH3	29	32								104						Top Boot
S71WS128RB0HH3	2A															80
S71WS128RB0HH3	09		104	Top Boot												
S71WS128RB0HH3	0A		80	Uniform Boot												

## 2. MCP Block Diagram



### 3. Connection Diagrams



**Note**  
1.  $V_{CC}$  pins must ramp simultaneously.

MCP	Flash-only Addresses	Shared Addresses
S71WS512RE0	A24	A23-A0
S71WS512RD0	A24-A23	A22-A0
S71WS256RD0	A23	A22-A0
S71WS256RC0	A23-A22	A21-A0
S71WS128RC0	A22	A21-A0
S71WS128RB0	A22-A21	A20-A0

#### 3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

#### 3.2 Look-ahead Ballout for Future Designs

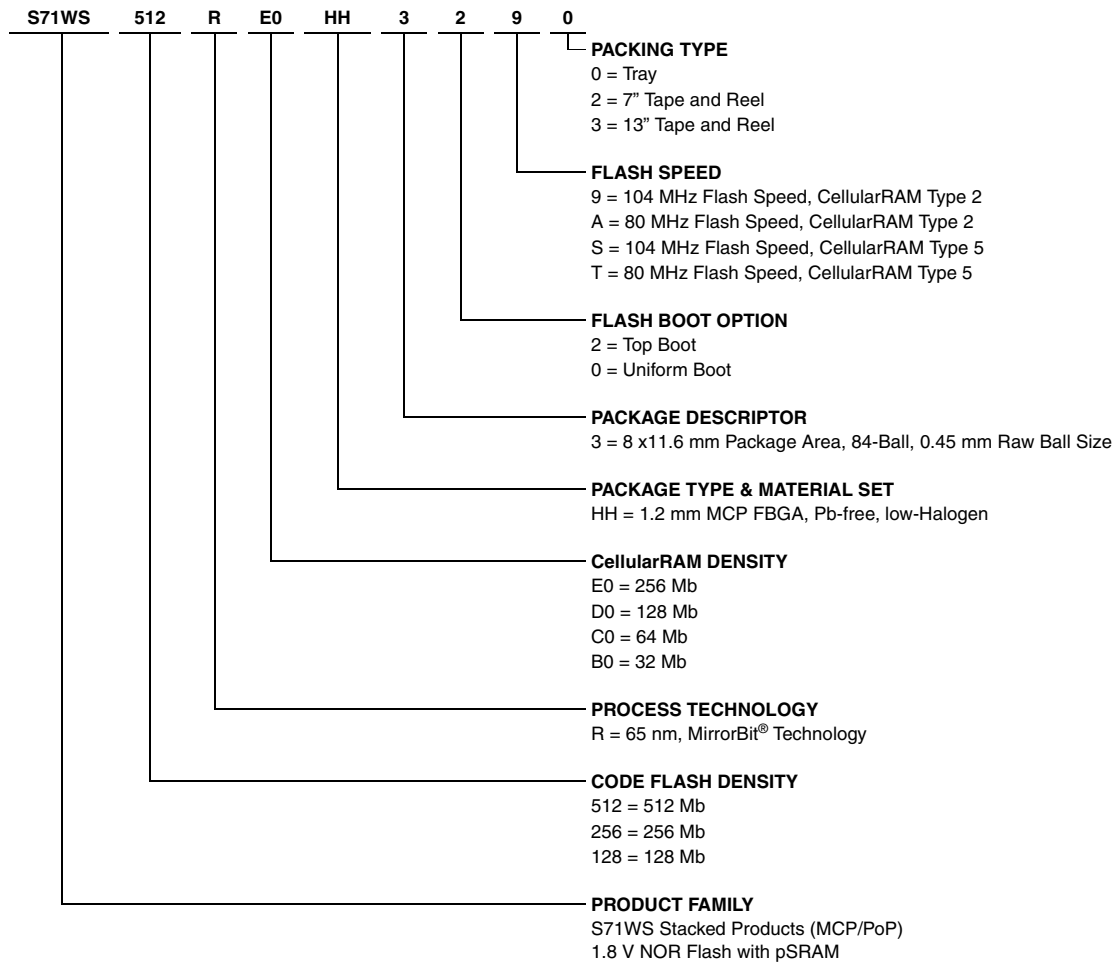
Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design\_Scalable\_Wireless\_A0\_E). Contact your local Spansion sales representative for more details.

### 3.3 NOR Flash and pSRAM Input/Output Descriptions

Signal	Description	Flash	pSRAM
Amax-A0	NOR Flash/pSRAM Address inputs	X	X
DQ15-DQ0	Flash Data input/output, shared between NOR and pSRAM	X	X
F-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.	X	
OE#	Output Enable input. Asynchronous relative to CLK for Burst mode.	X	X
WE#	Write Enable input.	X	X
F-V <sub>CC</sub>	NOR Flash device power supply (1.7 V - 1.95 V).	X	
F-V <sub>CCQ</sub>	Input/Output Buffer power supply.	X	
V <sub>SS</sub>	Ground	X	X
RFU	Reserved for Future Use		
RDY	Flash ready output. Indicates the status of the Burst read. V <sub>OL</sub> = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.	X	X
CLK	NOR Flash Clock, shared with CLK of burst-mode pSRAM.. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	X
AVD#	NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs. V <sub>IL</sub> = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V <sub>IH</sub> = device ignores address inputs	X	X
F-RST#	NOR Flash hardware reset input. V <sub>IL</sub> = device resets and returns to reading array data	X	
F-ACC	NOR Flash accelerated input. At V <sub>IH</sub> , accelerates programming; automatically places device in unlock bypass mode. At V <sub>IL</sub> , disables all program and erase functions. Should be at V <sub>IH</sub> for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM		X
R-CRE	Control Register Enable (pSRAM). For CellularRAM only.		X
R-VCC	pSRAM Power Supply		X
R-UB#	Upper Byte Control (pSRAM)		X
R-LB#	Lower Byte Control (pSRAM)		X
DNU	Do Not Use		

## 4. Ordering Information

The order number is formed by a valid combinations of the following:



### 4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

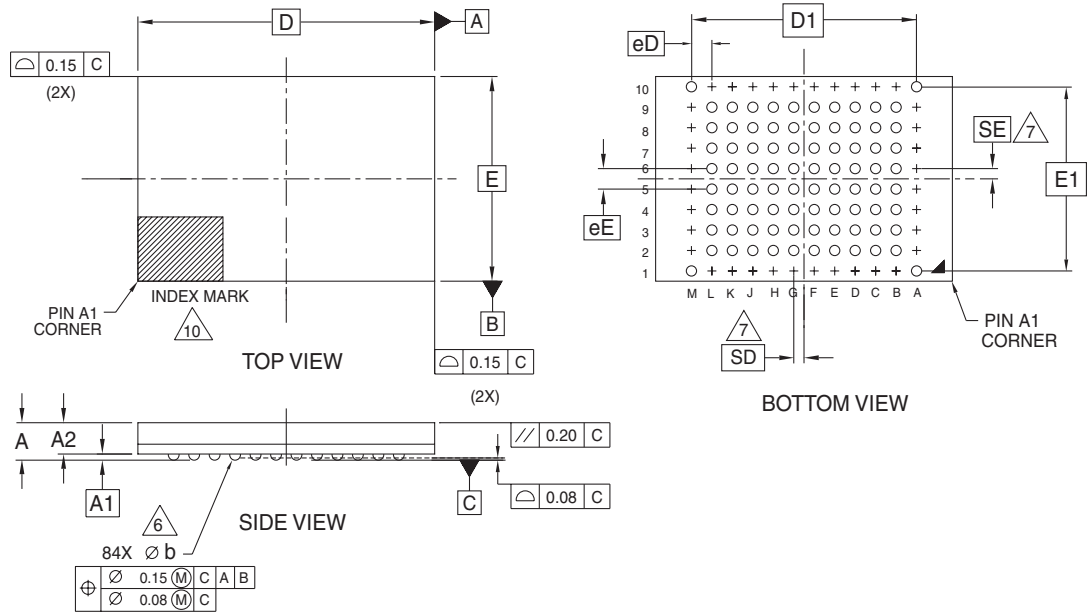
Valid Combination							
Product Family	Code Flash Denisty (Mb)	Process Technology	CellularRAM Density	Package Type / Material	Flash Boot Option	Flash Speed	Packing Type
S71WS	128	R	B0, C0	HH3	2, 0	9, A	0,2,3 (Note 1)
	256		C0, D0				
	512		D0			9, A, S, T	
			E0				

**Notes:**

- Packing Type 0 is standard. Specify other options as required.
- BGA package marking omits leading S and packing type designator from ordering part number.

## 5. Physical Dimensions

### 5.1 8 x 11.6 x 1.4 mm— 84-ball Fine Pitch Ball Grid Array (FBGA) Package



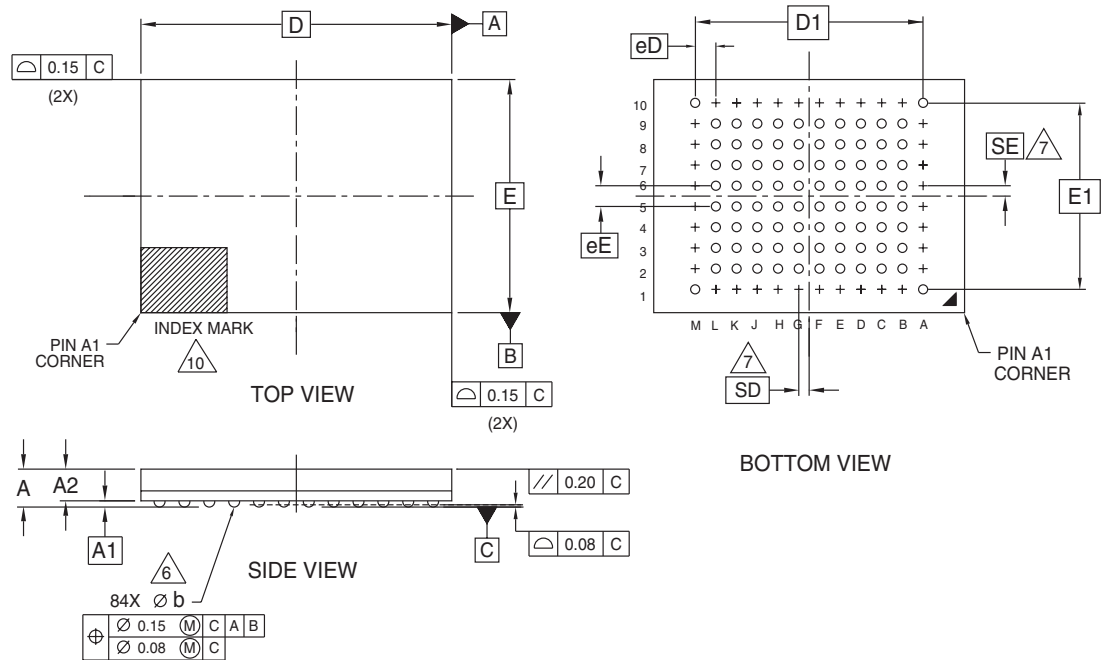
PACKAGE	FTA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
?	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- $\boxed{e}$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- $\triangle 6$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- $\triangle 7$  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{e}{2}$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- $\triangle 10$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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## 5.2 8 x 11.6 x 1.2 mm— 84-ball Fine Pitch Ball Grid Array (FBGA) Package



PACKAGE	TLA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- $e$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- $\triangle 6$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- $\triangle 7$  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $e/2$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- $\triangle 10$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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## 6. Revision History

Section	Description
<b>Revision 01 (April 14, 2008)</b>	
	Initial release
<b>Revision 02 (May 20, 2008)</b>	
Global	Added S71WS128RC0
Product Selector Guide	Updated model numbers for all OPNs
Ordering Information	Updated model numbers for all OPNs
Valid Combinations	Updated model numbers for all OPNs
<b>Revision 03 (November 19, 2008)</b>	
Global	Updated S71WS512RD0HH3 Added OPNs S71WS512RE0HH329/09
Product Selector Guide	Updated model numbers for all OPNs
Ordering Information	Updated model numbers for all OPNs

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