VTC Inc.
Value the Customer™

VM65011

ANALOG PRML CHANNEL for DVC APPLICATIONS

970801

ADVANCE INFORMATION

August,1997

FEATURES

- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently-variable real zeros
- Programmable five-tap transversal filter for PR4 equalization
- Self-adapting option for FIR tap weights
- Analog/sampled AGC
- Fast timing recovery loop which locks to random data
- Programmable data dropout detector
- Automatic tracking frequency servo tone filters and demodulator
- Programmable write current reference for Read/Write preamp
- Register-programmable power management (<5 mW Power Down Mode)
- Serial interface port for access to internal configuration registers to load and verify register contents
- Single power supply (5V ±10%) with optional 3.3V CMOS output supply
- Small footprint 64-pin PQFP package

DESCRIPTION

The VM65011 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement a Partial Response Maximum Likelihood (PRML) read channel for DVC systems with user data rates from 19 to 42* Mbps (* or higher).

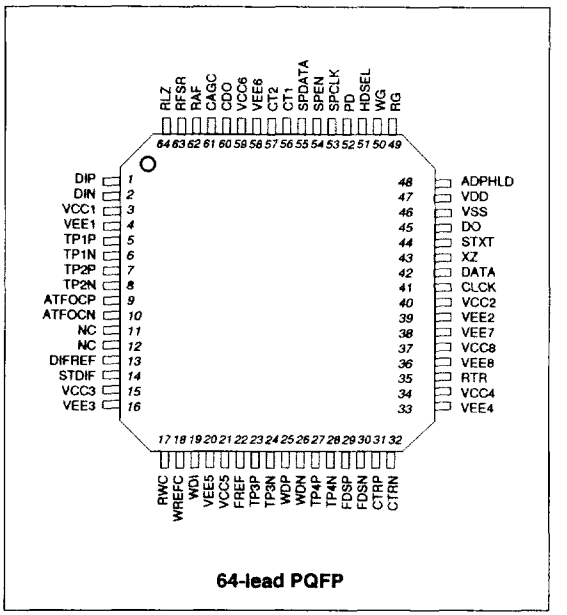
BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 64-Lead PQFP package.

Functional blocks include AGC, programmable continuous time filter, adaptive FIR filter, maximum likelihood Viterbi detector, TTL to differential PECL write data converter, programmable write current control, 2-tone ATF servo processor and data dropout detector.

Programmable functions such as filter cutoff/boost, FIR tap weights, adaption parameters, preamp write current, dropout detector gain and ATF gain are controlled by writing to the serial port registers. External component changes are required to change data rates.

For additional information, call VTC.

CONNECTION DIAGRAM



64-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC} ..... -0.3V to +7V
- V_{DD} ..... -0.3V to +7V

Input Voltages
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Analog Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V

Storage Temperature T_{stg} ..... -65°C to 150°C

Junction Temperature T_J ..... 150°C

Thermal Impedance Characteristics, Θ_{JA}:
- 64-Lead PQFP ..... 39°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} ..... +5V ± 10%
- V_{DD} ..... 3.3V ± 10% or +5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

MIXED SIGNAL CIRCUITS

BLOCK DIAGRAM DESCRIPTION

AUTOMATIC GAIN CONTROL:
- Dual mode AGC, analog during acquisition, sampled during read data
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Externally adjustable charge pump currents
- Low drift AGC hold circuitry
- Internal Low Z for write mode
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

LOW PASS FILTER/EQUALIZER:
- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 5 to 15 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable group delay of ±30%
  - Minimized size and power

FIR FILTER/EQUALIZER:
- Five tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- Independent and/or dependent self adaption of tap weights
- ADP hold feature controlled by external pin or internal 6T detector
- User programmable adaption parameters:
  - Integration time
  - Dead zone control
  - Tap starting points
  - Number of taps to adapt
  - Selection of which taps to independently adjust

MAXIMUM LIKELIHOOD DETECTOR:
- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length of 10 or 21
- Excess zeros counter monitoring consecutive recovered data zeros to aid in tape dropout detection

TIMING RECOVERY:
- Single external capacitor required
- Fast acquisition, sampled data phase lock loop which locks to random data
- Decision-directed clock recovery from data samples
- Programmable damping ratio

AUTOMATIC TRACKING FREQUENCY:
- Phase-locked loop to select 465kHz and 697.5kHz servo tones buried in the data spectrum
- Programmable VGA to compensate for head and signal variations
- Front end bandpass with gain and test output
- Low-tone gain adjustment capability for channel response compensation
- Output difference amplifier with separate bias pin allowing differential measurement
- Servo burst output indicator with programmable threshold

DROPOUT DETECTOR:
- Programmable VGA to compensate for head and signal variations
- Programmable one-shot delay to control detection sensitivity

WRITE CIRCUITRY:
- Five-bit programmable write current reference for preamp
- TTL to differential pseudo ECL write data converter

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BLOCK DIAGRAM

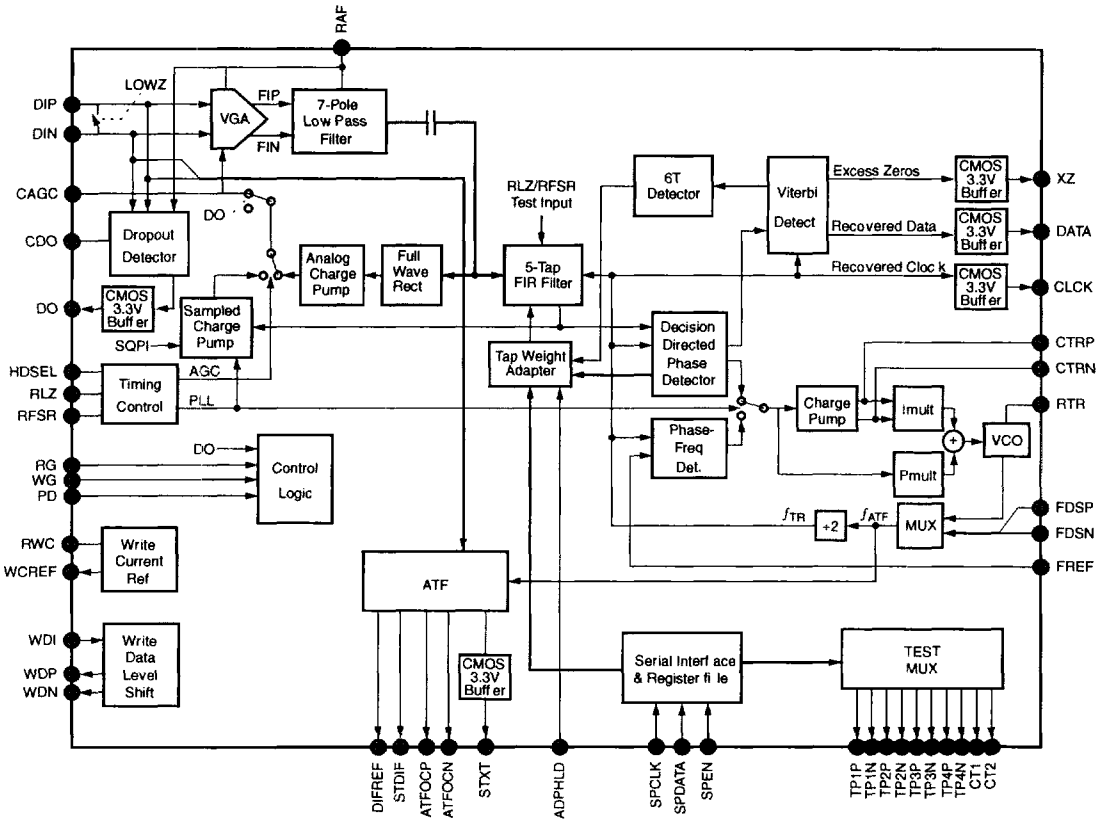

Diagram 1 VM65011 Top-Level Block Diagram

PIN FUNCTIONS AND DESCRIPTION

PIN TYPE	PIN NAME	PIN#	INFORMATION
Power Pins	VCC1	3	CT filter, analog AGC, analog test mux power
	VCC2	40	FIR filter, Viterbi detector, timing recovery power
	VCC3	15	ATF and write current reference power
	VCC4	34	Timing recovery VCO analog power
	VCC5	21	Write Data and test point ECL output and TTL input power
	VCC6	59	Internal digital CMOS and tub connection power
	VCC8	37	Viterbi digital CMOS and tub connection power
	VDD	47	3.3/5 V CMOS interface circuitry power
Ground Pins	VEE1	4	CT filter, analog AGC, analog test mux ground
	VEE2	39	FIR, Viterbi detector, timing recovery ground
	VEE3	16	ATF and write current reference ground
	VEE4	33	Timing recovery VCO analog ground
	VEE5	20	Write Data and test point ECL output ground
	VEE6	58	Internal digital CMOS ground
	VEE7	38	Bipolar substrate connection
	VEE8	36	Viterbi digital CMOS ground
	VSS	46	3.3/5 V CMOS interface circuitry ground
3.3/5V CMOS Inputs	WDI	19	Write Data In from microcontroller. This input is converted to a PECL signal and output on pins WDP and WDN. WDI is also used as the test input clock to the VCO.
	FREF	22	41.85 MHz input reference frequency
	ADPHLD	48	Adaptive FIR Hold (active high)
	RG	49	Read Gate. Selects read mode (active high)
	WG	50	Write Gate. Selects write mode (active high)
	HDSEL	51	Head Select. Low selects Head 0 registers, high selects Head 1 registers, transition initiates head switch sequence
	PD	52	Power down control signal. When this signal is asserted, the chip is powered down. (active high)
	SPCLK	53	Serial port clock (latch on positive edge)
	SPEN	54	Serial port I/O enable (active high)
3.3/5V CMOS Outputs	CLCK	41	Recovered Clock.
	DATA	42	Recovered Data.
	XZ	43	Excess Zeros. High level indicates number of consecutive zeros in recovered data has exceeded a programmable value.
	STXT	44	Servo Tone Exceeds Threshold. High or low tone is selected via serial interface and compared against programmable threshold. Results of comparison is output on this pin.
	DO	45	Drop Out indicator. High level indicates tape drop out.
5V CMOS Bidirectional Input/Outputs	SPDATA	55	Bidirectional serial port data signal
5V CMOS Outputs	CT1	56	CMOS Test Output 1
	CT2	57	CMOS Test Output 2
Pseudo ECL Differential Inputs	FDSP FDSN	29 30	Timing Recovery (Data Separator) test Frequency input

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PIN TYPE	PIN NAME	PIN#	INFORMATION
Pseudo ECL Differential Outputs, V_{CC} referenced	WDP WDN	25 26	Write data output
	TP3P TP3N	23 24	Digital Bipolar Test point 3 output
	TP4P TP4N	27 28	Digital Bipolar Test point 4 output
External Resistor Connections	RWC	17	Write Current reference resistor. An external resistor from this pin to VEE3 establishes range of programmable reference current (output on WREFC) used by preamp as a write current reference. 3.5kΩ <R_{WC}< 12kΩ, 4.7kΩ nominally.
	RTR	35	Timing Recovery PLL reference resistor. An external resistor is connected from this pin to VEE4 to establish a precise internal reference current for the timing recovery VCO center frequency. 2kΩ <R_{TR}< 6kΩ, 2.5kΩ nominally.
	RAF	62	AGC and CT Filter reference resistor. An external resistor is connected from this pin VEE1 to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency, AGC charge pump currents, and Dropout Detector decay current. 4kΩ <R_{AF}< 32kΩ, 6kΩ nominally.
	RFSR	63	Fast Recovery reference resistor. A resistor between this pin and VEE1 defines the duration of the fast recovery period. 10kΩ <R_{FSR}< 40kΩ, 20kΩ nominally. Also used as a differential analog test input in conjunction with RLZ.
	RLZ	64	Low Z duration control. A resistor between this pin and VEE1 defines the duration of the Low Z period. 10kΩ <R_{FSR}< 40kΩ, 20kΩ nominally. Also used as a differential analog test input in conjunction with RFSR
External Capacitor Connections	CTRP CTRN	31 32	Timing Recovery PLL loop filter. Differential connections for the timing recovery PLL loop filter capacitor, nominally 1200pF.
	CDO	60	Dropout time constant capacitor, nominally 1600pF to VEE1.
	CAGC	61	AGC Gain capacitor, nominally 820 pF to VEE1
Analog Differential Inputs	DIP DIN	1 2	Analog Read Data input
Analog Outputs	TP1P TP1N	5 6	Differential analog test point 1 output
	TP2P TP2N	7 8	Differential analog test point 2 output
	ATFOCP ATFOCN	9 10	ATF input bandpass filter output and analog test point
	DIFREF	13	Differential Reference bias for STDIF. Nominal output value of 1.5V.
	STDIF	14	Servo Tone Differential output. Indicates amplitude difference between high and low tone servo filters relative to a 1.5V common-mode bias. STDIF is higher than DIFREF if the high servo tone's amplitude is greater than the low servo tone's amplitude. Nominal output range is 0.75V to 2.25V. Tone levels are equal if STDIF=DIFREF=1.5V.
	WREFC	18	Programmable Write Reference Current used by preamp.