73S1113F
EMV Smart-Card Terminal Controller
with Built-in ISO-7816 Interface and USB

DATA SHEET

NOVEMBER 2005

DESCRIPTION

The TERIDIAN Semiconductor Corporation 73S1113F is a CMOS single chip ISO-7816 smart-card terminal micro-controller that implements all the functions required to build a low-cost smart-card terminal with a USB interface, suitable for various applications including EMVCo compliant payment terminals. Its enhanced set of features supports several configurations allowing low component count and a fast design cycle. Based on an 80C52 core, it incorporates communication and man-machine interfaces. The TERIDIAN 73S1113F device is applicable to either portable or host-connected applications. Embedded Flash memory makes the TERIDIAN 73S1113F a complete system-on-chip suitable for both development and production phases.

This data-sheet presents the package and pin description, as well as the electrical features that are unique to the TERIDIAN 73S1113F. It also presents a brief description of the architecture and of its embedded functions.

Refer to the 73S11xxF Hardware User's Guide for more detailed information about the microcontroller architecture, description of the registers, description of the different blocks that are common to the TERIDIAN 73S11xxF smart card terminal controller family.

Also refer to the TERIDIAN 73S11xxF Software User's Guide for a complete description of the Application Programming Interface (API).

APPLICATIONS

- **CCID-compliant PINpad Smart Card Terminals**
- **USB Smart Card Readers**
- **Micosoft® WHQL-compliant Smart Card Terminals**
- **E-commerce Terminals**

ADVANTAGES

- **True System-on-Chip solution, with built-in communication interfaces and peripherals**
- **Compact solution, that requires only a few external components**
- **Embedded 64kB Flash and 5kB RAM are the largest memory size among 8-bit smart card reader controllers in the industry**
- **Low-cost solution for portable and host-connected terminals**
- **Software API (Application Programming Interface) includes the ready-to-use protocol layers for asynchronous cards and USB**
  - **→ Faster development time**
  - **→ Time-to-Market**
- **Ready-to-use USB Smart Card reader application, provided with a Microsoft WHQL approved driver**

Designed for Microsoft® Windows®XP

FEATURES

80C52 core:

- 12 clock-cycle / instruction
- CPU clocked up to 24MHz (with a 12MHz crystal)
- 16-bit PC (64kB program linear memory address space)

Memory:

- 64kB internal Flash (Program Memory)
- 128 Bytes Flash Info Memory Block
- Flash memory guaranteed for 10,000 erase-write cycles
- 1kB IRAM (internal RAM for registers) + 4kB internal XRAM (User Data Memory)
- Interface for external program / data memory
- Boot-ROM loader program allows both In-System-Programming and In-Application-Programming of the embedded flash (ISP and IAP modes)
- ISP programming mode can be permanently disabled by protection fuses

Oscillator:

- Single low-cost 12MHz crystal
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C52 2-priority level structure
- 8 different sources of interrupt

Power Down Modes:

- 2 standard 80C52 Power Down and IDLE modes

Timers:

- (3) Standard 80C52 timers T0, T1 and T2

Built-in ISO-7816 card interface:

- Independent step-up converter generates VCC for the card (3V or 5V)
- Compliant with EMV 4.0 (EMV2000)
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4-C8 signals)
- 4.5kV ESD protection on all interface pins

Communication with smart cards:

- ISO-7816 UART 9600 to 115kbps (with 12MHz crystal) for protocols T=0, T=1
- 2-Byte FIFO for transmit and receive
- Hardware support to manage additional external card interfaces

Communication interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- USB 1.1 Full Speed 12Mbps Interface (backward compatible with USB 2.0), PC/SC compliant with 4 Endpoints:
  - Control (16B FIFO)
  - Interrupt IN (32B FIFO)
  - Bulk IN (128B FIFO)
  - Bulk OUT (128B FIFO)

Man-Machine Interface and I/Os:

- 5x5 Keyboard (hardware scanning, debouncing and scrambling)
- (7) Dedicated LCD I/Os (Control of any external HD44780 standard LCD driver) – Can be also used as standard I/Os
- (8) User I/Os

Voltage Detection:

- (1) Analog Input (Voltage detection range: 0.2V to 2.5V)

Operating Voltage:

- 2.7V to 3.6V (3V to 3.6V when USB is in use)

Operating Temperature:

- 0°C to 85°C

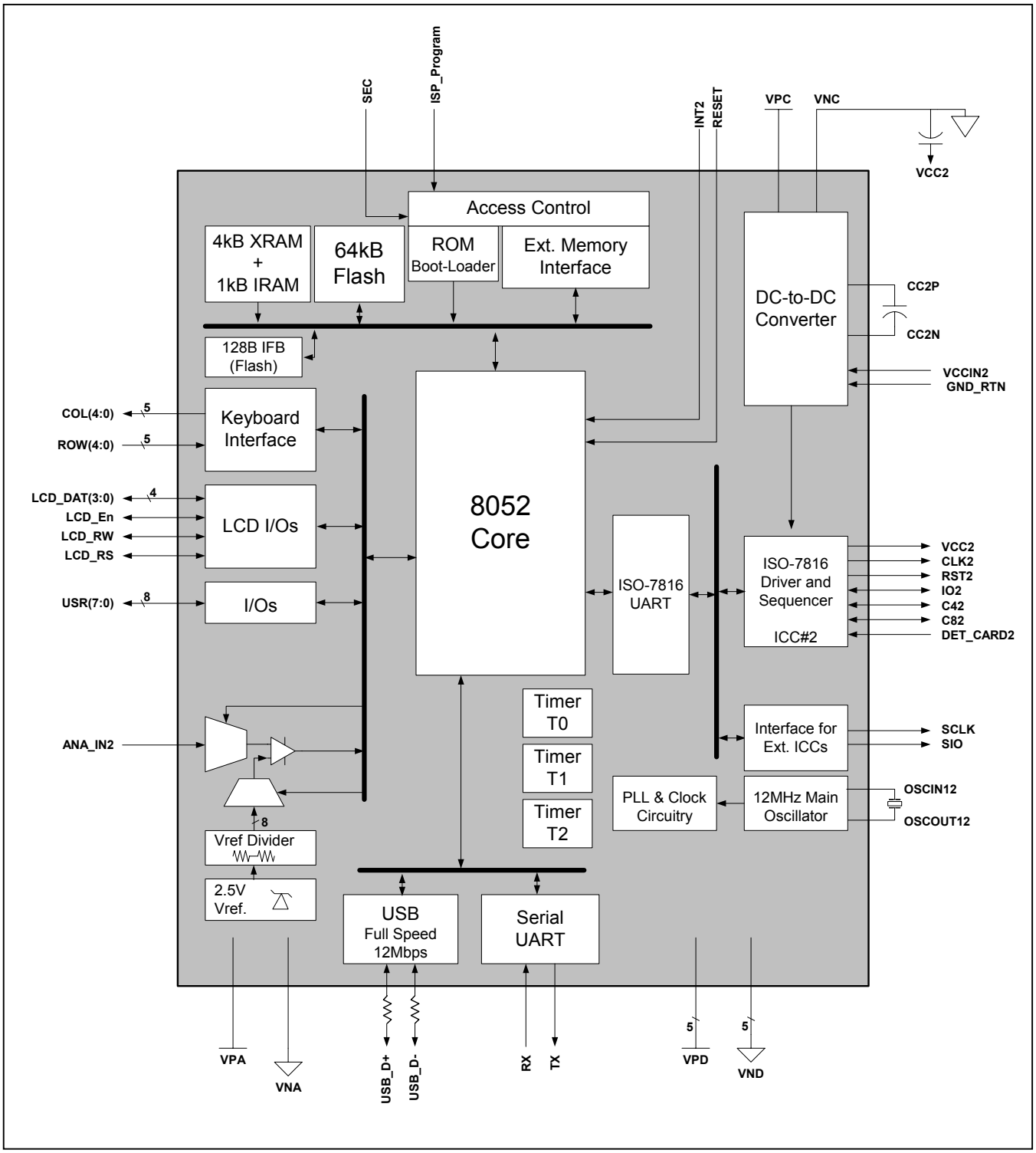
Package:

- 64 pin LQFP

Software:

- Two-level Application Programming Interface (ANSI C-language libraries)
- USB, T=0/T=1 and EMV-compliant smart card protocol layers
- PIN Management functions compatible with CCID requirements

FUNCTIONAL DIAGRAM



MICROCONTROLLER

The 73S1113F core is an 8-bit 80C52 micro-controller, with embedded 5kB of RAM (data memory) and 64kB of flash (program memory). An additional Information Block Flash cell (128B IFB) is available for storage of device ID, serial number, firmware version etc.
An embedded ROM boot-loader allows downloading of the flash memory (either program or IFB) through the serial port. This programming mode can be forced externally (In-System-Programming = ISP mode) or also can be called by the application (In-Application-Programming = IAP mode) through the Application Programming Interface. The 73S1113F flash memory can also be programmed with a parallel PROM programmer. Embedded security fuses allow the user to permanently disable the ISP mode. It allows the 73S1113F, once programmed with an application, to run independently without possibility from the external world to re-download a non-authorized application. Other features include:

- The 73S1113F has an on-chip oscillator that requires a 12MHz crystal. Internal clock circuitry generates clock signals to the different blocks and to the CPU (that can be clocked at 6, 12 or 24MHz).
- The 73S1113F has the standard 8052 2-priority level interrupt structure, with 8 different interrupt sources: 2 external interrupts (pins INT2 and INT0), 3 timer interrupts, 1 serial/USB interrupt, 1 smart-card interrupt and a shared interrupt (keypad and analog comparator inputs).
- The 73S1113F incorporates 3 timers, T0, T1 and T2 that can be clocked internally or externally by the respective input signals on the pins USR0, USR1 and USR2.
- Standard 8052 Power Down mode and IDLE mode are supported for power saving modes. The clock for each block, as well as the analog circuitry (analog input, voltage reference and USB transceiver) and the DC-to-DC converter (VCC generator for the card) can be independently enabled or disabled by firmware to optimize power consumption.
- Management of the embedded card interface, peripherals and communication capabilities are controlled by means of dedicated registers in RAM. Management of the interrupts, of the power saving modes and of the clock circuitry is also controlled through registers.

ISO-7816 INTERFACE AND UART

The feature set of the TERIDIAN 73S1113F includes one built-in smart-card interface, controlled by an ISO-7816 compliant sequencer. The built-in smart card interface has a DC-DC converter, which is able to generate the card power supply, VCC=3V or 5V. The sequencer handles the activation / deactivation of the card signals. The card interface includes an input for the card presence switch (programmable polarity) and auxiliary I/O lines for C4 / C8 signals. A hardware ISO-7816 UART with a dedicated FIFO allows easy implementation of asynchronous card protocols T=0 and T=1. This UART can be bypassed to allow a firmware UART to handle other protocols such as synchronous card protocols. Control and use of the ISO-7816 UART is widely and easily configurable with dedicated registers located in XRAM. A 2-line interface enables the 73S1113F to control additional external smart card (ICC) interfaces, typically for multiple-SAM configurations. The ISO-7816 UART is shared between all the smart card interfaces (internal and external).

COMMUNICATION, HUMAN-MACHINE INTERFACE AND I/Os

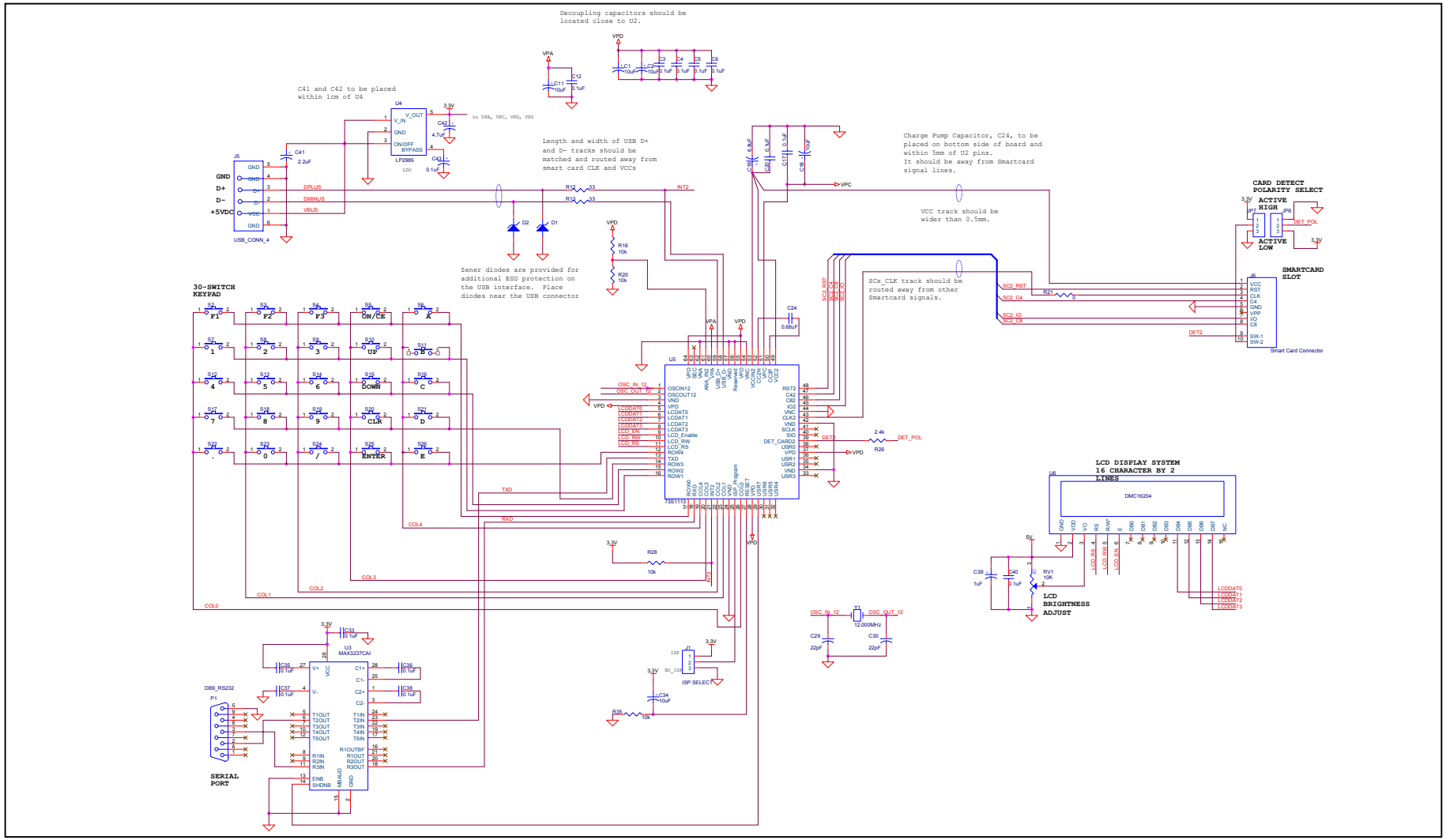
- The 73S1113F has a full-speed (12Mbps) USB slave interface with 4 endpoints for implementation of computer-connected terminals. A standard 8052 serial UART allows the 73S1113F to communicate with any host or peripheral on a serial link, at a data transmission rate from 1200 to 115kbps. Communication with a computer through RS232 can be easily implemented only using an external level shifter.
- Keyboard implementation is supported with a built-in 5x5 keyboard interface with hardware scanning and debouching. It also features a scrambling capability (change of the scanning order).
- 7 I/O lines are dedicated to control an external standard LCD driver, allowing a wide choice of LCDs to be controlled by the 73S1113F, such as 7-wire, Hitachi-type HD44780.
- Additional input/outputs feature 8 user I/Os and 1 analog input for voltage detection (for battery monitoring or any DC voltage comparison).

PIN DESCRIPTION

Pin Name	64 LQFP Pin #	# Pins	Type	Description
VND	3, 24, 34, 42, 57	5	GND	Digital ground
VPD	4, 28, 37, 55, 64	5	Supply	Digital power. 2.7V - 3.6V Must be greater than 3V when using the USB interface. \Each pin to be decoupled to VND with a 0.1μF capacitor.
VNA	62	1	GND	Analog ground
VPA	60	1	Supply	Analog power. 2.7V - 3.6V To be decoupled to VNA with a 0.1μF capacitor.
VPC	51	1	Supply	DC/DC Step-up Converter power (2.7 - 3.6V). Each pin to be decoupled to VNC with one 0.1μF and one 10μFcapacitor.
VNC	44, 54	2	GND	DC/DC Step-up Converter ground
OSCIN12	1	1	I	12MHz crystal input. Can drive clock in and leave OSCOUT12 unconnected
OSCOUT12	2	1	O	12MHz crystal output. Leave unconnected if not using a crystal
CLK2	43	1	O	ICC Clock Signal
IO2	45	1	I/O	ICC I/O Signal
RST2	48	1	O	ICC RST Signal
CC2P	50	1	I/O	Step-up Converter Capacitor 2 Positive Node (0.68μF Low ESR)
CC2N	52	1	I/O	Step-up Converter Capacitor 2 Negative Node
VCC2IN	53	1	I	Card interface voltage supply for interface circuits – take from VCC2 filter capacitor
VCC2	49	1	O	ICC VCC Signal Must be decoupled to GND with a 6.8μF low-ESR capacitor.
C42	47	1	I/O	ICC C4 Signal
C82	46	1	I/O	ICC C8 Signal
DET_CARD2	39	1	I	ICC presence contact input pin. Programmable polarity (to be connected accordingly to the card presence switch with a pull-up / pull-down)
SIO	40	1	I/O	I/O for external ICC interfaces. Internal pull-up configuration – no external pull-up required.
SCLK	41	1	O	ICC clock for external Smart-Card interfaces
SEC	63	1	I	Digital security input that controls the internal protection fuse. Active High. Internal pull-down allows NC for normal operation. When set, permanently deactivates the ISP programming mode.
ANA_IN2	61	1	I	Analog Input – (Voltage detection input 0.2V to 2.5V ±3%
RESET	27	1	I	73S1113F Reset. Active high
ISP_Program	25	1	I	Forces internal Flash programming in ISP mode at reset. Active High. 0 = Indicates the user does not want to program the flash if checksum passes. Internal pull-down allows NC for normal operation
Reserved	56	1	-	To be connected to VND

Pin Name	64 LQFP Pin #	# Pins	Type	Description
COL (4)	19	5	O	Keypad column drive lines
COL (3)	20			
COL (2)	22			
COL (1)	23			
COL (0)	26			
ROW (4)	12	5	I	Keypad row sense lines, includes pull-up function
ROW (3)	14			
ROW (2)	15			
ROW (1)	16			
ROW (0)	17			
TXD	13	1	O	Transmit data - Serial output port from the 73S1121F serial UART
RXD	18	1	I	Receive data - Serial input port to the 73S1121F serial UART
USR (7)	29	8	I/O	User programmable I/O port.
USR (6)	30			
USR (5)	31			
USR (4)	32			
USR (3)	33			
USR (2)	35			
USR (1)	36			
USR (0)	38			
INT2	21	1	I	External interrupt input pin
USB_D-	58	1	I/O	USB D- Requires a 33 Ω series resistor
USB_D+	59	1	I/O	USB D+ Requires a 33 Ω series resistor
LCDDAT (3)	8	4	I/O	LCD driver dedicated I/O lines - Data pins. Can be used as standard I/Os
LCDDAT (2)	7			
LCDDAT (1)	6			
LCDDAT (0)	5			
LCD_Enable (LCDDAT (4))	9	1	I/O	LCD driver dedicated I/O line: LCD Enable. Can be used as standard I/O
LCD_RW (LCDDAT (5))	10	1	I/O	LCD driver dedicated I/O line: LCD Read/Write. Can be used as standard I/O
LCD_RS (LCDDAT (6))	11	1	I/O	LCD driver dedicated I/O line: LCD Register Select. Can be used as standard I/O
TOTAL		**64**		

TYPICAL APPLICATION SCHEMATIC



ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to the device.

PARAMETER	RATING
Supply Voltage (V_{PD}, V_{PA}, V_{PC})	-0.5V to 4.0V
Pin Input Voltage (except OSCIN12, OSCIN32)	-0.5V to 6.0V
Pin Input Voltage (OSCIN12, OSCIN32)	-0.5V to VPD + 0.5V
Storage Temperature	-60 to 150°C
Pin Current	±50mA
Maximum continuous Total Power Dissipation (at T_A = 85 °C)	850 mW
Maximum Operating Junction Temperature	125 °C
ESD Tolerance – Card interface pins*	+/- 4.5kV
ESD Tolerance – USB interface pins**	+/- 750V
ESD Tolerance – Other pins	+/- 500V

Note*: ESD testing on Card pins is HBM condition, 3 pulses, each polarity referenced to ground.

Note**: The ESD voltage rating when installed on a circuit board with the 33 Ω series resistors is greater than ± 5KV at the USB connector. To obtain ESD voltage ratings above 12KV, additional protection circuitry such as zener diodes must be attached per the application schematic.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage $V_{PA}/V_{PD}/V_{PC}$ with respect to $V_{NA}/V_{ND}/V_{NC}$ when not using USB I/F	2.7V to 3.6V
Supply Voltage $V_{PA}/V_{PD}/V_{PC}$ with respect to $V_{NA}/V_{ND}/V_{NC}$ when using USB I/F	3.0V to 3.6V
Supply Voltage V_{PD} with respect to V_{ND} for RAM data retention	2.0V to 3.6V
12MHz Oscillator Frequency	12.000 MHz ±100ppm
Operating Temperature	0°C to +85°C
Input Voltage for DP/DM	0V to 3.6V
Input Voltage for ANA_IN(2)	0V to 3.6V

THERMAL RESISTANCE

PARAMETER	RATING
$R_{th\ (J-A)}$ Thermal Resistance Junction to Ambient	47º C/W

DC CHARACTERISTICS: DIGITAL I/OS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Digital I/O except for OSC12 I/O						
V_{IL1}	Input Low Voltage		-0.5		0.8	V
V_{IH1}	Input High Voltage		0.7*V_{PD}		5.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{PD} - 0.45			V
I_{IL1}	Input Low Leakage Current	$V_{SS} < V_{in} < V_{IL1}$ Pull-ups Disabled[1]			1	µA
I_{IH1}	Input High Leakage Current	$V_{IH1} < V_{in} < V_{DD}$ Pull-downs Disabled[2]			1	µA
I_{IL3}	Input Low Leakage Current	$V_{SS} < V_{in} < V_{IL1}$ Pull-ups Enabled[1]			35	µA
I_{IH3}	Input High Leakage Current	$V_{IH1} < V_{in} < 5.5V$ Pull-downs Enabled[2]			120	µA

DC CHARACTERISTICS: OSCILLATOR I/OS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Oscillator (OSC) I/O Parameters						
V_{IL12}	Input Low Voltage - OSCIN12		-0.5		0.075* V_{PD}	V
V_{IH12}	Input High Voltage - OSCIN12		0.7*V_{PD}		V_{PD} + 0.5	V
$V_{OLOSC12}$	Output Low Voltage - OSCOUT12	I_{OL} = 3.0mA			0.7	V
$V_{OHOSC12}$	Output High Voltage - OSCOUT12	I_{OH} =-3.0mA	V_{PD} - 0.9			V
I_{IL2}	Input Leakage Current - OSCIN12	$V_{SS} < V_{in} < V_{IL2}$	1		30	µA
I_{IH2}	Input High Leakage Current - OSCIN12	$V_{IH2} < V_{in} < V_{DD}$	1		30	µA
$t_{OSC12MStart}$	12MHz Oscillator start up time	Osc V_{PP} = 90% stable V_{PP} @ V_{PC} = 3.3V, 25°C		500		µs

[1] Pull-ups on USR1(7:0),ROW(4:0)
[2] Pull-downs on ISP_Program

DC CHARACTERISTICS: USB INTERFACE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Receiver parameters						
V_{DI}	Differential input sensitivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Transmitter levels						
V_{OL}	Low Level Output Voltage	USBCon = 1 (D+ pull-up enabled)			0.3	V
V_{OH}	High Level Output Voltage	15K ohm resistor to ground	V_{PD} - 0.1		V_{PD}	V
Leakage parameters						
I_{OZ}	High-Z state data line leakage current	0V < VIN < 3.6V			±5	µA
Output resistance						
Z_{DRV}	Driver output resistance with external 36Ω resistor	Steady state drive	28		44	Ω
Z_{pu}[3]	Pull-up Resistor (to V_{PD})	USBCon = 1	1.2	1.5	1.8	kΩ

[3] USB specifies that this value be 1.5k Ω +/- 5%. An external resistor could be used instead (MIUSCTRL bit 0 set by firmware)

DC CHARACTERISTICS: ICC INTERFACE - CLK AND RST SIGNALS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Clock Line CLK2 (V_{CC} = $V_{CC}2$)						
V_{OHC}	High Level Output Voltage	0 < I_{OH} < 50µA, V_{CC} = Min	V_{CC} - 0.5		V_{CC}	V
V_{OLC}	Low Level Output Voltage	-50µA < I_{OL} < 0, V_{CC} = Min	0		0.4	V
$t_{r\text{-}clk}$, $t_{f\text{-}clk}$	Rise / Fall time	C_{load} = 30pF max	-		8% of clock period	
P_{ERTLC}	Signal perturbation low	Signal low	- 0.25		0.4	V
P_{ERTHC}	Signal perturbation high	Signal high	V_{CC} - 0.5		V_{CC} + 0.25	V
δ	Duty Cycle	Clocks in stable operation	45		55	%
Reset Line RST2 (V_{CC} = $V_{CC}2$)						
V_{OHR}	High Level Output Voltage	0 < I_{OH} < 50µA, V_{CC} = Min	V_{CC} - 0.5		V_{CC}	V
V_{OLR}	Low Level Output Voltage	-50µA < I_{OL} < 0, V_{CC} = Min	0		0.4	V
$t_{r\text{-}RST}$, $t_{f\text{-}RST}$	Rise / Fall time	C_{load} = 30pF Max	-		0.8	µs
P_{ERTLR}	Signal perturbation low	Signal low	- 0.25		0.4	V
P_{ERTHR}	Signal perturbation high	Signal high	V_{CC} - 0.5		V_{CC} + 0.25	V

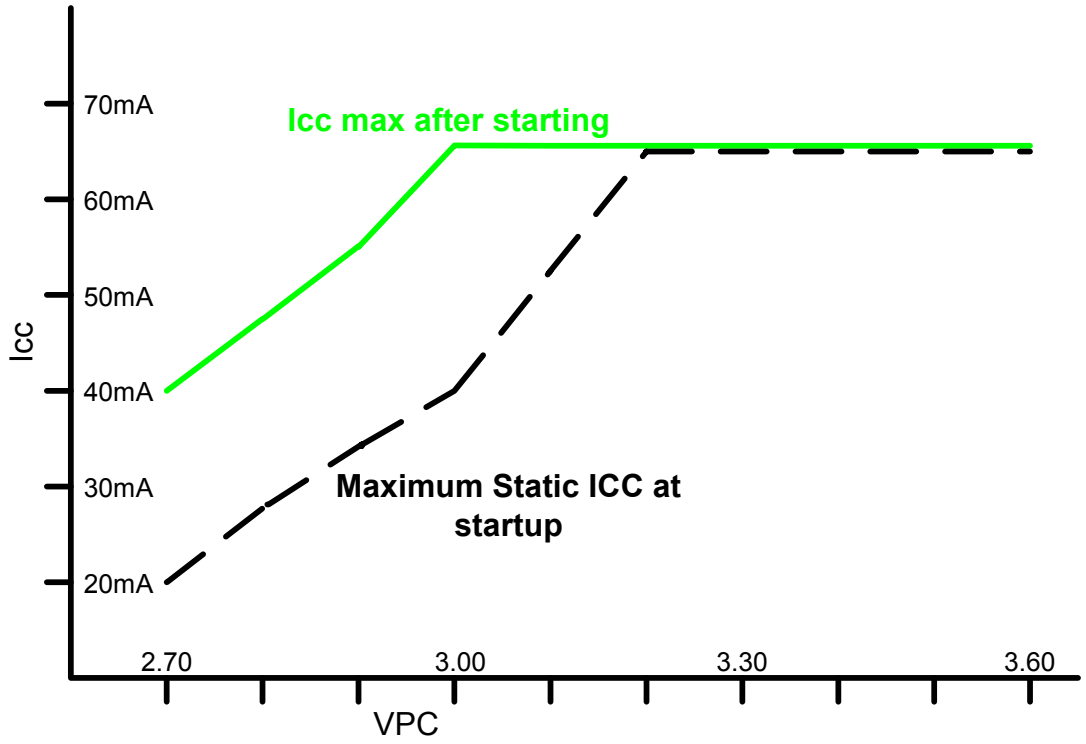
DC CHARACTERISTICS: ICC INTERFACE – I/O SIGNALS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Data Lines IO2, C42/C82 (V_{CC} = $V_{CC}2$)						
V_{OHSC}	High Level Output Voltage	0 < I_{OH} < 20µA, V_{CC} = Min	0.8 * V_{CC}		V_{CC}	V
V_{OLSC}	Low Level Output Voltage	-1ma < I_{OL} < 0, V_{CC} = Min	0		0.4	V
$t_{r\text{-}SC}$, $t_{f\text{-}SC}$	Rise / Fall time (Output)	C_{load} = 30pF Max	-		0.8	µs
P_{ERTLSC}	Signal perturbation low	Signal low	-0.25		0.4	V
P_{ERTHSC}	Signal perturbation high	Signal high	0.8 * V_{CC}		V_{CC} + 0.25	V
I_{OLS}C (Inactive)	Current from I/O when inactive and pin grounded				-500	V
V_{ILSC}	High Level Input Voltage		0.6 * V_{CC}		V_{CC}	V
V_{ILSC}	Low Level Input Voltage		0		0.5	V
I_{IHSC}	High Level Input Current	V_{in} = V_{IHSC} range	-300		20	µA
I_{ILSC}	Low Level Input Current	V_{in} = V_{ILSC} range	-1000		20	µA
I_{SCSC}	Short Circuit Current	33Ω to opp. supply	-15		15	mA
I_{RTFTSC}	Rise / Fall time (Input)		-		1.2	µs
R_{PUSC}	Pull-up to VCC	Static	10	12.5	17	kΩ

DC CHARACTERISTICS: ICC INTERFACE – VCC SIGNALS (DC-DC CONVERTER)

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Card Power Supply ($V_{CC}2$)						
V_{CC2}	Output Voltages to ICC2 (with 40nA.s dynamic loads and VNOISE included) 2.9V < VPC < 3.6V	5V output	4.6	5.0	5.4	V
		3V output	2.7	3.0	3.3	V
		Deactivated	-0.25	0.0	0.4	V
V_{NOISE}	Peak to peak ripple and noise on VCC	C_L = 6.8 µF and C_{cp} = 0.68 µF		150	200	mV_{pp}
I_{CC2}	Maximum Output Currents to ICC2. 3.0V < VPC < 3.6V	5V output	65		200	mA
		3V output	65		200	mA
I_{OC}	ICC over-current.	Each output measured separately		100	200	mA
$I_{STARTUP}$*	V_{CC} Startup current	Assertion of $\overline{CMDVCC}$			See Curve	mA

Note: The following diagram shows the maximum start up and maximum operating current for V_{CC}. If the load placed on V_{CC} draws more current than line indicated by "Maximum Static ICC at startup" when V_{CC} is asserted, the DC-DC converter may not be able to achieve the minimum voltage levels as specified for $V_{CC}2$ above. Once the startup load condition has been met, the load can be increased to draw up to the current limit indicated by the line labeled "I_{CC} max after starting". This type of load increase is expected as the clock signal to the card is asserted and data transfer takes place. The diagram shows the worst case condition, which is at 85°C.



DC CHARACTERISTICS: VOLTAGE REFERENCE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_{lvdet}	V_{PD} Low Voltage Flash Erase/Write Protect	Analog enabled (Disable_Analog = 0)	2.350	2.500	2.650	V

DC CHARACTERISTICS: ANALOG INPUTS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_2	Voltage Threshold 2	ACOMP(3:1) =2	1.242	1.28	1.318	V

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PA}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Analog Current (V_{PA})						
$I_{DDA-off}$	Supply current on V_{PA} when Analog and USB Off	Disable_Analog = 1 Disable_USBXcvr=1		1	5	µA
I_{DDA-on}	Supply current on V_{PA} when Analog On and USB Off	Disable_Analog = 0 Disable_USBXcvr=1		1.0	1.5	mA
$I_{DDA-USBon}$	Supply current on V_{PA} when Analog and USB On	Disable_USBXcvr=0 Disable_Analog = 0		1.5	2.5	mA

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PD}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Digital Current (V_{PD})						
I_{DDPD}	Digital supply current on V_{PD}, PD Mode , oscillators and clocks Off	OSCIN12 Off, CPU in PD mode, All other clocks Off		1	10	µA
$I_{DDIDLE12M}$	Digital supply current on V_{PD}, IDLE Mode – 12MHz oscillator and clock circuitry (PLL) On	OSCIN12 On, CPU in IDLE mode, Disable_PLL=0, All other clocks Off, CPU clock=6MHz CPU clock=12MHz CPU clock=24MHz		3.1 3.4 3.8	5 5 5.5	mA
I_{DDRun}	Digital supply current on V_{PD}, Normal Mode – 12MHz oscillator and clock circuitry (PLL) On	OSCIN12 On, All other clocks Off, CPU clock=6MHz CPU clock=12MHz CPU clock=24MHz		5.5 7.0 10	7.5 9.0 13	mA
$I_{DDSuspend}$	Digital supply current on V_{PD}, USB in Suspend mode	OSCIN12 Off, USB suspended, All internal clocks Off, CPU in PD mode		11	25	µA
V_{DDDR}	RAM data retention supply voltage		2.0			V

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PC}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
DC-to-DC converter Current (V_{PC})						
$I_{DDon565}$	Supply current on V_{PC} when V_{CC}=5V and 65mA load	VCC2 = 5V. ICC2 = 65mA, ICC IO, C4, C8 = high		135	150	mA
$I_{DDon365}$	Supply current on V_{PC} when V_{CC}=3V and 65mA load	VCC2 = 3V. ICC2 = 65mA, ICC IO, C4, C8 = high		140	150	mA
$I_{DDon527}$	Supply current on V_{PC} when V_{CC}=5V and 27mA load	VCC2 = 5V. ICC2 = 27mA, ICC IO, C4, C8 = high		60	70	mA
$I_{DDon327}$	Supply current on V_{PC} when V_{CC}=3V and 27mA load	VCC2 = 3V. ICC2 = 27mA, ICC IO, C4, C8 = high		60	75	mA
$I_{DDon502}$	Supply current on V_{PC} when V_{CC}=5V and 2mA load	VCC2 = 5V. ICC2 = 2mA, ICC IO, C4, C8 = high		6	8	mA
$I_{DDon302}$	Supply Current on V_{PC} when V_{CC}=3V and 2mA load	VCC2 = 3V, ICC2 = 2mA, ICC IO, C4, C8 = high		6	8	mA
$I_{DDSCStdby5}$	Supply current on VPC when V_{CC}=5V and cards are in power down mode	VCC2 = 5V, ICC2 = 0mA, ICC IO, C4, C8 = high Card clock stopped		1	2	mA
$I_{DDSCStdby3}$	Supply current on V_{PC} when V_{CC}=3V and cards are in power down mode	VCC2 = 3V, ICC2 = 0mA, ICC IO, C4, C8 = high Card clock stopped		1	2	mA
$I_{DDSCOff}$	Supply current on V_{PC} when DC-DC converter is Off	V_{CC2} = 0V, 2MHz dc/dc clock Off, Analog circuitry Off		1	5	µA

AC CHARACTERISTICS: 8052 EXTERNAL MEMORY INTERFACE TIMING

SYMBOL	PARAMETER	MIN	Typ.	MAX	UNIT
F_{OSC}	Processor Clock Frequency	0	12.00	24	MHz
T_{OSC}	Processor Clock Period		83.33		ns

AC CHARACTERISTICS: USB INTERFACE

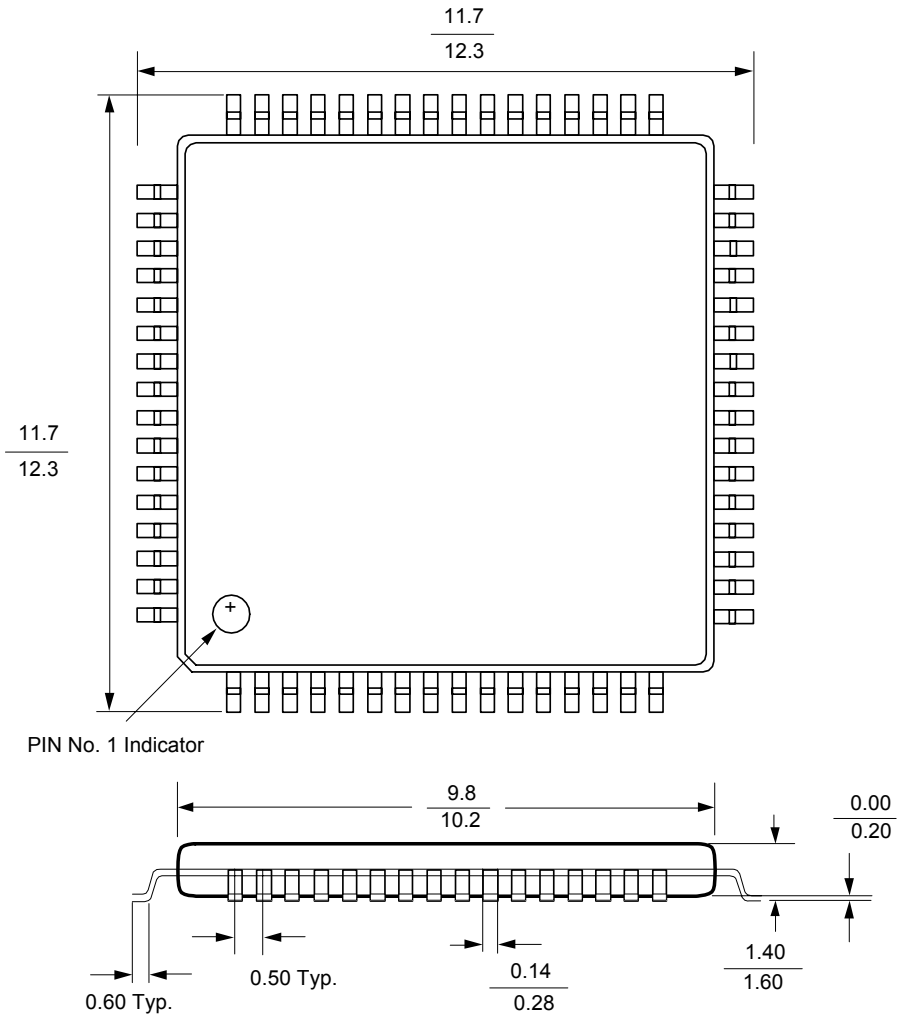
SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
C_L = 50pF, series 33Ω 1% source termination resistor included						
T_{R_USB}	Rise Time	10% to 90%	4		20	ns
T_{F_USB}	Fall Time	90% to 10%	4		20	ns
T_{RFM}	Rise/fall time matching	(USBTR/USBTF)	75		1.33	%
V_{CRS}	Output signal crossover voltage	Includes VDI range	1.3		2.3	V
T_{DJ1}[4,5]	Source Jitter to Next Transition	Measured as in Figure 4.4.2.1 of USB 2.0 Specification	-3.5		3.5	ns
T_{DJ2}[1, 2]	Source Jitter For Paired Transitions	Measured as in Figure 4.4.2.1 of USB 2.0 Specification	-4		4	ns
T_{JR1}	Receiver Jitter to Next Transition	Measured as in Figure 4.4.2.2 of USB 2.0 Specification	-18.5		18.5	ns
T_{JR2}	Receiver Jitter for Paired Transitions	Measured as in Figure 4.4.2.2 of USB 2.0 Specification	-9		9	ns
T_{EOPT}	Source SE0 interval of EOP	Figure 4.4.2.3 of USB 2.0 Specification	160		175	ns
T_{EOPR}[6]	Receiver SEO interval of EOP	Figure 4.4.2.3 of USB 2.0 Specification	82			ns

4 For both transitions of differential signaling.
5 Excluding first transition from the Idle state.
[6] Must accept as valid EOP.

MECHANICAL DRAWINGS

CAUTION: Use handling procedures necessary for a static sensitive component

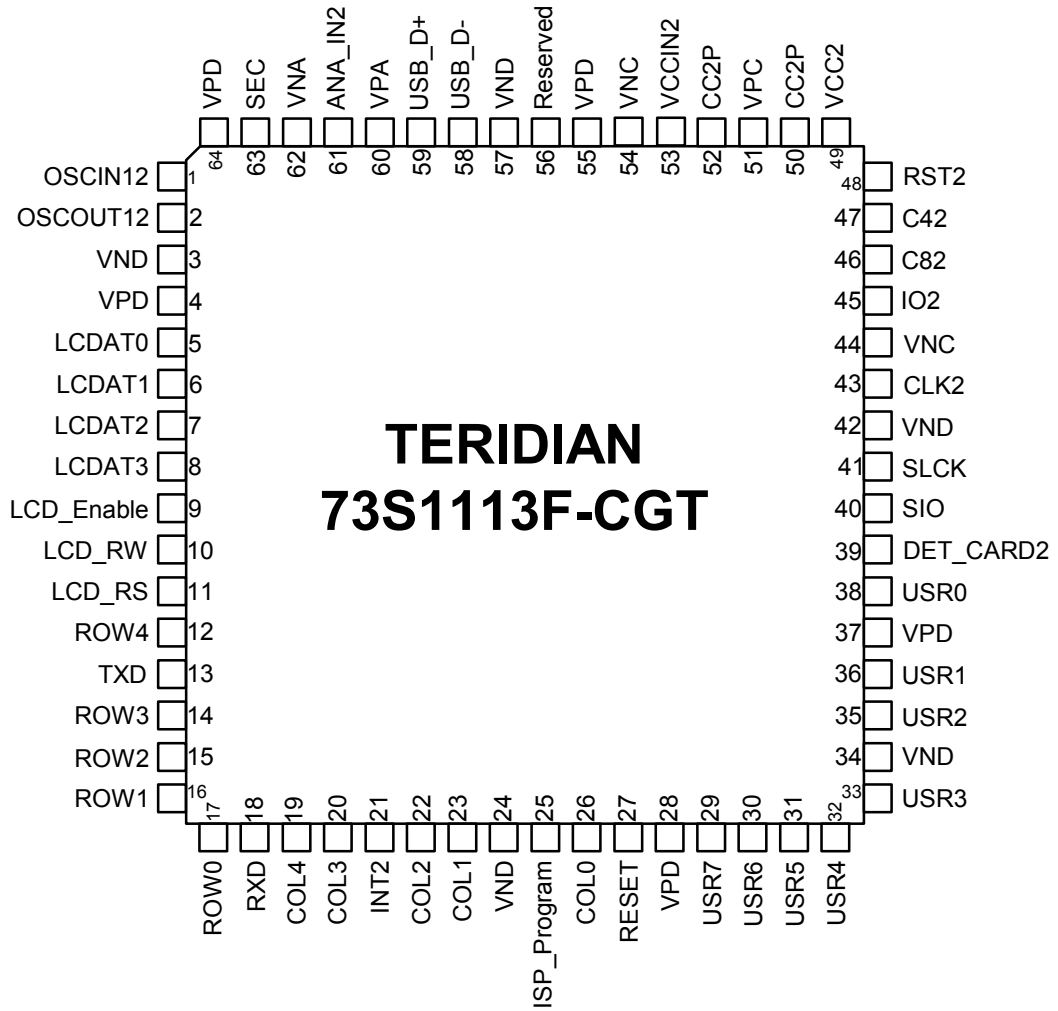
The following figure shows the package outline of the 73S1113F in its LQFP 64-pin packaged form. It is available in both tray and tape-reel conditioning.



Controlling dimensions in mm

LQFP 64 – Package Outline

PACKAGE PIN DESIGNATIONS



LQFP64 Pin Assignment (Top View)

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGING MARK
73S1113F - 64 pin LQFP	73S1113F-CGT	73S1113F-CGT
73S1113F - 64 pin LQFP Tape / Reel	73S1113F-CGTR	73S1113F-CGT
73S1113F - 64 pin LQFP Lead-Free	73S1113F-CGT / F	73S1113F-CGT
73S1113F - 64 pin LQFP Lead-Free Tape / Reel	73S1113F-CGTR / F	73S1113F-CGT

Data Sheet

TERIDIAN Semiconductor Corp. • 6440 Oak Canyon Rd. • Irvine, CA • 92618-5201
TEL (714) 508-8800 • FAX (714) 508-8877
http://www.teridiansemi.com

11/2/05 Rev. 2.3