
HD74HC323

8-bit Universal Shift/Storage Register (with 3-state Outputs)

HITACHI

ADE-205-489 (Z)
1st. Edition
Sep. 2000

Description

This eight-bit universal register features multiplexed I/O ports to achieve full eight bit data handling in a single 20-pin package. HD74HC323 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S_0 and S_1 high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

Features

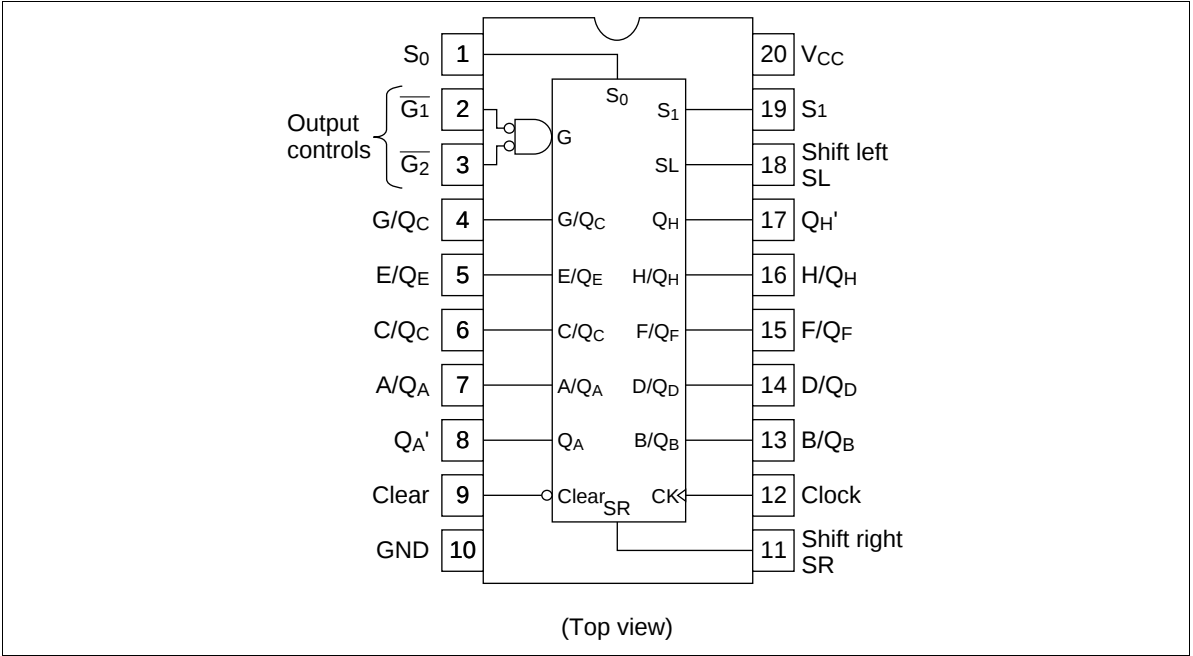
- High Speed Operation: t_{pd} (Clock to Q) = 20 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Inputs		Serial Inputs/Outputs																	
		Function Select		Output Control		Clock	Outputs												
Mode	Clear	S ₁	S ₀	$\overline{G}_1\uparrow$	$\overline{G}_2\uparrow$		S _L	S _R	A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '	
Clear	L	X	L	L	L		X	X	L	L	L	L	L	L	L	L	L	L	
	L	L	X	L	L		X	X	L	L	L	L	L	L	L	L	L	L	
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}	
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}	
Shift	H	L	H	L	L		X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}	
Right	H	L	H	L	L		X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}	
Shift	H	H	L	L	L		H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H	
Left	H	H	L	L	L		L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L	
Load	H	H	H	X	X		X	X	a	b	c	d	e	f	g	h	a	h	

a ... h = the level of the steady-state input at A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

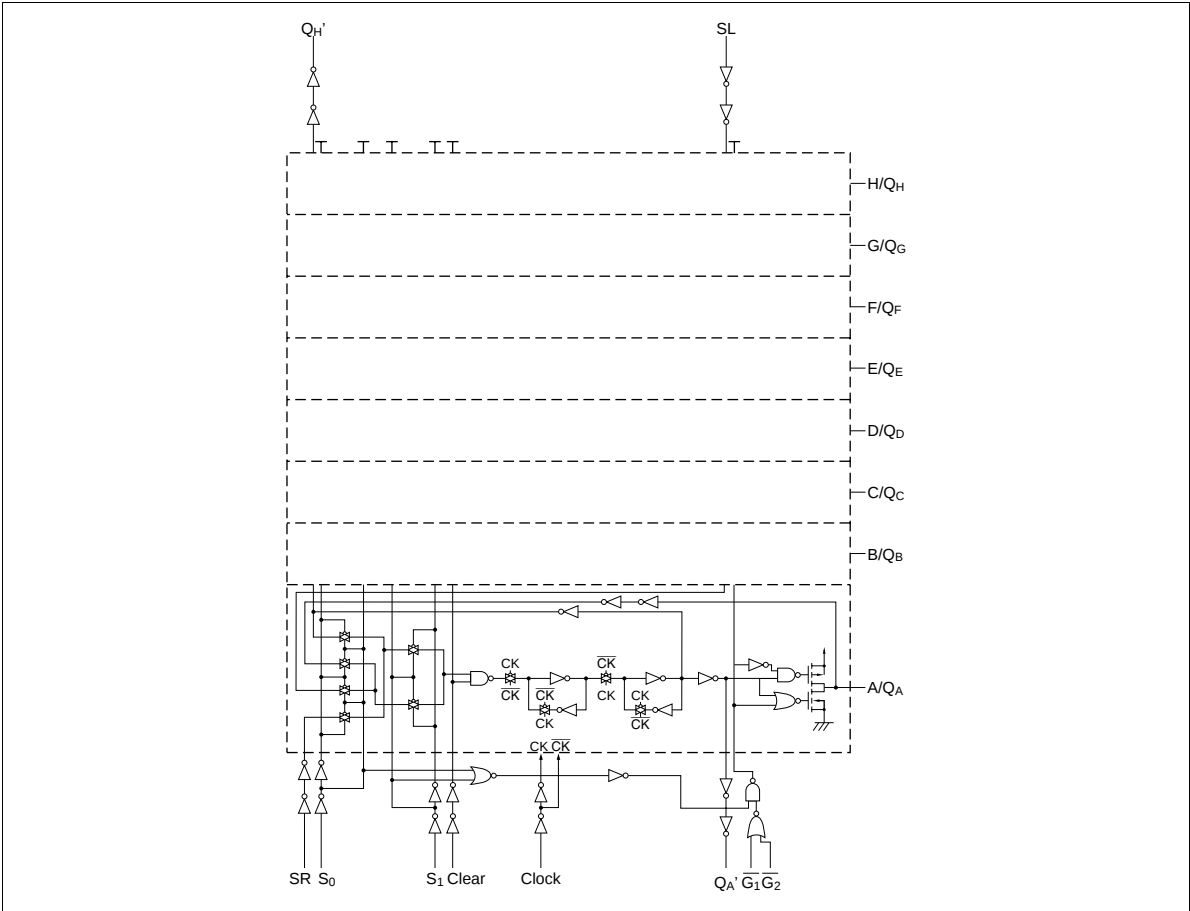
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	±35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Logic Diagram



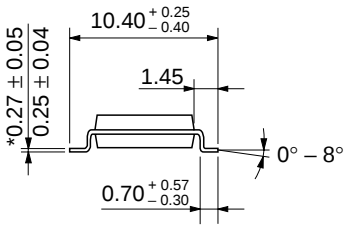
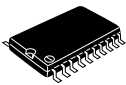
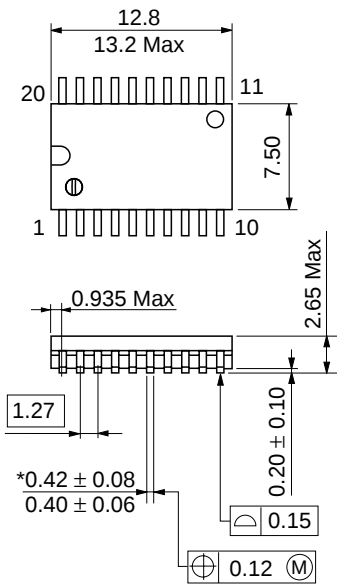
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C				Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max					
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V				
		4.5	3.15	—	—	3.15	—					
		6.0	4.2	—	—	4.2	—					
	V _{IL}	2.0	—	—	0.5	—	0.5	V				
		4.5	—	—	1.35	—	1.35					
		6.0	—	—	1.8	—	1.8					
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA		
		4.5	4.4	4.5	—	4.4	—					
		6.0	5.9	6.0	—	5.9	—					
		4.5	4.18	—	—	4.13	—				Q _A to Q _H	I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—					I _{OH} = -7.8 mA
		4.5	4.18	—	—	4.13	—				Q _A ’, Q _H ’	I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—					I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA		
		4.5	—	0.0	0.1	—	0.1					
		6.0	—	0.0	0.1	—	0.1					
		4.5	—	—	0.26	—	0.33				Q _A to Q _H	I _{OH} = 6 mA
		6.0	—	—	0.26	—	0.33					I _{OH} = 7.8 mA
		4.5	—	—	0.26	—	0.33				Q _A ’, Q _H ’	I _{OH} = 4 mA
		6.0	—	—	0.26	—	0.33					I _{OH} = 5.2 mA
		Off-state output current	I _{OZ}	6.0	—	—	±0.5				—	±5.0
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND			
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA			

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	31	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	Clock to Q_A' or Q_H'
		4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
	t_{PHL}	2.0	—	—	175	—	220	ns	Clock to Q
		4.5	—	20	35	—	44		
		6.0	—	—	30	—	37		
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	Q_A' , Q_H'
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
	t_{THL}	2.0	—	—	60	—	75	ns	Q
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohite-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic Components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 585160
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Hitachi Asia Ltd. Hitachi Tower 16 Collyer Quay #20-00, Singapore 049318 Tel: <65>-538-6533/538-8577 Fax: <65>-538-6933/538-3877 URL: http://www.hitachi.com.sg Hitachi Asia Ltd. (Taipei Branch Office) 4/F, No. 167, Tun Hwa North Road, Hung-Kuo Building, Taipei (105), Taiwan Tel: <886>-(2)-2718-3666 Fax: <886>-(2)-2718-8180 Telex: 23222 HAS-TP URL: http://www.hitachi.com.tw
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Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
URL: <http://www.hitachi.com.hk>

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