

VFJA401

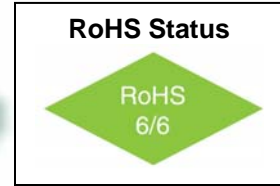
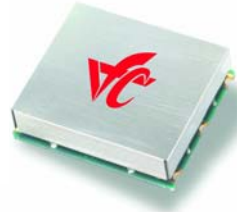
Quad Input to 800MHz

Jitter Attenuator w/ F_{OUT} to 200 MHz



Features

- 10 MHz to 200MHz Output Frequency Range
- 200 MHz to 800 MHz Input Frequency Range
- Ultra Low Jitter and Phase Noise: -130 dBc/Hz @ 1KHz
- Low Power: < 150mW typical

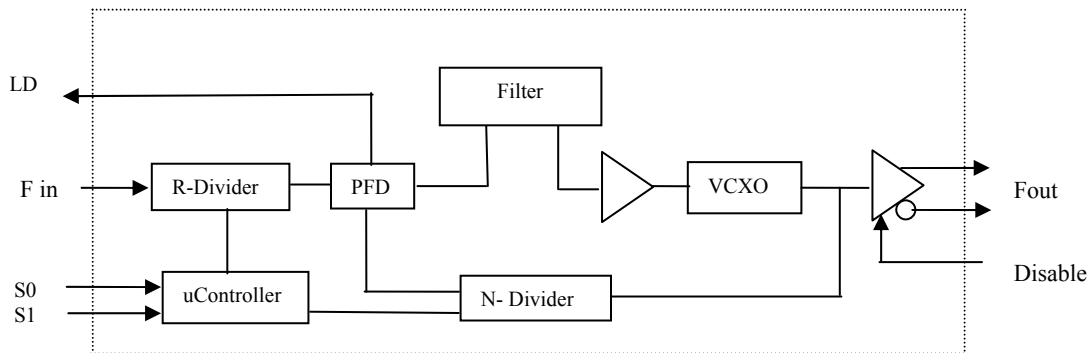


Applications

- Sonet / SDH / ATM
- 10 Gigabit Ethernet
- Wireless Infrastructure

Description

The VFJA401 is a Jitter Attenuator capable of providing an output frequency up to 200 MHz. Two select inputs [S1,S0] allow the user to select 1 of 4 preset input frequencies. A Lock Detect signal indicates when the output signal is frequency locked to the input. Operating with a +3.3 volt power supply the device typically consumes 150 mW. The output is configured as a differential LVPECL signal and requires external termination resistors. The VFJA401 is available in a 19.5mm x 15.5 mm surface mount package.



Block Diagram



VFJA401

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Break Down Voltage	V _{cc}		-0.5		5.5	V	
Storage Temperature	T _s		-55		+105°	°C	

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note	
Output Frequency Range	F _{out}		10		200	MHz		
Input Frequency Range	F _{in}		200		800	MHz		
Input Level	V _{in}	AC coupled internally	0.4		3.3	V p-p		
Output Level Logic "1"	V _{oh}	50 Ohm to V _{cc} -2V or Thevenin Equivalent	V _{cc} -0.96		V _{cc} -0.81	V		
Output Level Logic "0"	V _{ol}		V _{cc} -1.85		V _{cc} -1.65	V		
Phase Jitter		12KHz to 20MHz		0.20	0.5	ps(rms)		
SSB Phase Noise	Φ _n	100Hz 1KHz 10KHz 100KHz		-100 -130 -145 -150		dBc/Hz	@ 155.52MHz	
APR			± 32			ppm		
Modulation BW			10			Hz	Note 1	
Duty Cycle		@ 50%	45	50	55	%		
Rise / Fall Time	Tr/Tf	20% to 80%			0.6	ns		
Start up time				2	10	ms		
Supply Voltage	V _{cc}		3.15	3.30	3.45	V		
Input Current	I _{cc}			45	55	mA		
Operating Temperature Range	T _a		0° -40°		+70° +85°	°C	Order code B Order code G	
Lock Detect	LD	Output HIGH (> 2.5 V) : In Lock; Output LOW (< .5V): Out of Lock						LVC MOS
Enable / Disable Function		Input HIGH (>2.5V): Output Disabled Input LOW (<0.5V) or floating: Output Enabled						LVC MOS
Enable / Disable Time	Te/Td				100	ns		

Notes:

1. Consult factory for Bandwidth options



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How to Order

VFJA401 — Suffix

Sample Frequencies Table 2

P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)	P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)
-001	00	622.080	19.44	-002	00	622.080	38.88
	01	644.5314	19.44		01	644.5314	38.88
	10	669.32658	19.44		10	669.32658	38.88
	11	693.48315	19.44		11	693.48315	38.88
-003	00	622.080	77.76	-004	00	622.080	155.52
	01	644.5314	77.76		01	644.5314	155.52
	10	669.32658	77.76		10	669.32658	155.52
	11	693.48315	77.76		11	693.48315	155.52

Once Input and Output frequencies have been submitted and approved, the Factory will assign a part number.



