

# TS 68000

## HMOS HIGH DENSITY N-CHANNEL SILICON-GATE DEPLETION LOAD 16/32 BIT MICROPROCESSOR

### DESCRIPTION

The TS 68000 is the first implementation of the 68000 16/32 microprocessor architecture. The TS 68000 has a 16-bit data bus and 24-bit address bus. It is completely code-compatible with the TS 68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the TS 68020 32-bit implementation of the architecture. Any user-mode programs written using the TS 68000 instruction set will run unchanged on the TS 68008 and TS 68020. This is possible because the user programming model is identical for all three processors and the instruction sets are proper sub-sets of the complete architecture.

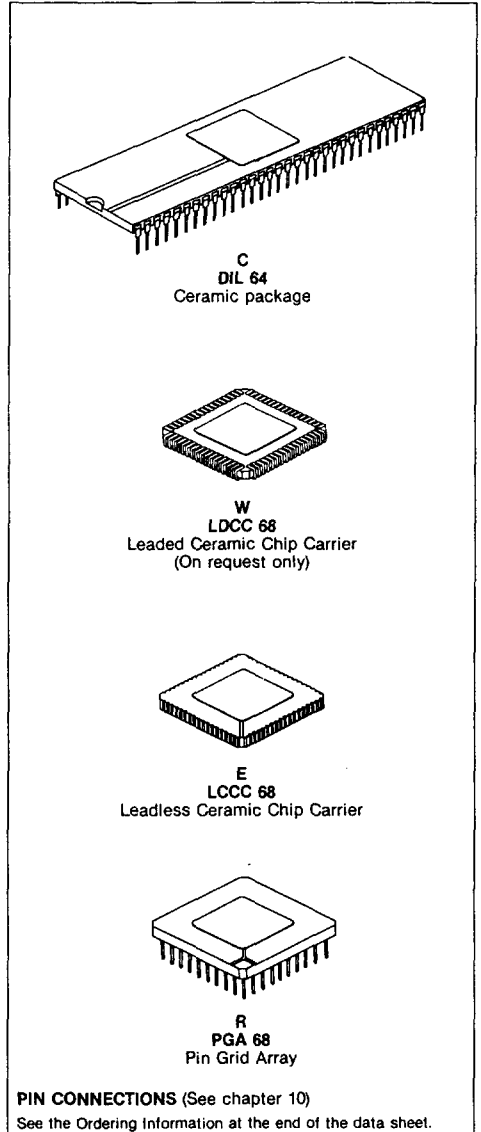
### MAIN FEATURES

- 16/32-bit data and address register.
- 16 megabytes direct addressing range.
- 56 powerful instruction types.
- Operations on five main data types.
- Memory mapped I/O.
- 14 addressing modes.
- 3 available versions : 8 / 10 and 12.5 MHz.
- Military temperature range :  
-55°C / + 125°C (8 / 10 and 12.5 MHz).
- Power supply : 5.0 V<sub>DC</sub> ± 5 %.

### SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 class B.
- DESC 82021.
- TCS standard.



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## 1 - SCOPE

This drawing describes the specific requirements for the microprocessor 68000, 8, 10 and 12.5 MHz in compliance either with MIL-STD-883 class B rev C, CECC 90000 class B or TCS STANDARD.

## 2 - APPLICABLE DOCUMENTS

### 2.1 - MIL-STD-883

- 1) MIL-STD-883 : test methods and procedures for electronics.
- 2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
- 3) Desc Drawing 8202102 (8 MHz) - 8202103 (10 MHz) - 8202104 (12.5 MHz).

### 2.2 - CECC 90000

- 1) CECC 90000.
- 2) Specification CECC 90110-001 8 / 10 and 12.5 MHz.

## 3 - REQUIREMENTS

### 3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

### 3.2 - Design and construction

#### 3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be as shown in § 10.

#### 3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1895.

#### 3.2.3 - Package

The microcircuits are packaged in a hermetically sealed ceramic package which is conformed to case outlines of MIL-STD-1835 (when defined).

- 64 lead DIL / SB - C8 - C7
- 68 lead LDCC - W8 (on request)
- 68 lead LCCC - E8 - E7
- 68 lead PGA - R8 - R7

The precise case outlines are described in § 9 of this document.

### 3.3 - Electrical requirements

#### 3.3.1 - Absolute maximum ratings

Symbol	Characteristics	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage		-0.3	+7	V
V <sub>I</sub>	Input voltage		-0.3	+7	V
T <sub>stg</sub>	Storage temperature		-65	+150	°C
P <sub>D</sub>	Power dissipation	T <sub>case</sub> = -55°C for 8 - 10 - 12.5 MHz		1.75	W
		T <sub>case</sub> = +125°C for 8 - 10 MHz for 12.5 MHz		1.5 1.7	W W
T <sub>j</sub>	Junction temperature			170	°C
T <sub>leads</sub>	Lead temperature	max soldering 5 seconds		270	°C
T <sub>case</sub>	Operating temperature - see Note	T <sub>case</sub> 8 - 10 - 12.5 MHz	-55	+125	°C

**Note:** T<sub>case</sub> could be -40°C / +85°C or 0°C / +70°C as specified in ordering information § 11.4.

**3.3.2 - Recommended operating conditions**

Symbol	Characteristics and conditions	Operating ranges		
		Min	Max	Unit
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High level input voltage	2		V
V <sub>IL</sub>	Low level input voltage		0.8	V
f	Frequency of operation			
	– 8 MHz part	2	8	MHz
	– 10 MHz part	2	10	MHz
	– 12.5 MHz part	4	12.5	MHz
T <sub>case</sub>	Case operating temperature range - see Note			
	T <sub>case</sub> 8 - 10 - 12.5 MHz part	-55	+125	°C
t <sub>r</sub>	Clock rise time		10	ns
t <sub>f</sub>	Clock fall time		10	ns

**Note :** T<sub>case</sub> could be -40°C / +85°C or 0°C / +70°C as specified in ordering information § 11.4.

**3.3.3 - Electrical performance conditions**

The electrical performance characteristics are specified in tables 1 and are applied over full operating temperature range unless otherwise specified (see § 11).

**3.4 - Mechanical and environment**

The microcircuit shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

**3.5 - Marking**

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following informations as minimum :

**3.5.1 - Thomson logo****3.5.2 - Manufacturer's part number****3.5.3 - Class B identification****3.5.4 - Date-code of inspection lot****3.5.5 - ESD identifier if available****3.5.6 - Country of manufacturing**

## 3.6 - Thermal characteristics

Package	Symbol	Parameter	Value	Unit
DIL 64	$\theta_{J-A}$	Thermal resistance Junction to Ambient	25	$^{\circ}\text{C/W}$
	$\theta_{J-C}$	Thermal resistance Junction to Case	6	$^{\circ}\text{C/W}$
PGA 68	$\theta_{J-A}$	Thermal resistance Junction to Ambient	30	$^{\circ}\text{C/W}$
	$\theta_{J-C}$	Thermal resistance Junction to Case	6	$^{\circ}\text{C/W}$
LCCC 68	$\theta_{J-A}$	Thermal resistance Junction to Ambient	40	$^{\circ}\text{C/W}$
	$\theta_{J-C}$	Thermal resistance Junction to Case	8	$^{\circ}\text{C/W}$
LDCC 68	$\theta_{J-A}$	Thermal resistance Junction to Ambient	50	$^{\circ}\text{C/W}$
	$\theta_{J-C}$	Thermal resistance Junction to Case	10	$^{\circ}\text{C/W}$
CQFP 68	$\theta_{J-A}$	Thermal resistance Junction to Ambient	40	$^{\circ}\text{C/W}$
	$\theta_{J-C}$	Thermal resistance Junction to Case	8	$^{\circ}\text{C/W}$

**Power considerations**

The average chip-junction temperature,  $T_J$ , in  $^{\circ}\text{C}$  can be obtained from :

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

$T_A$  = Ambient Temperature,  $^{\circ}\text{C}$

$\theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient,  $^{\circ}\text{C/W}$

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$ , Watts — Chip Internal Power

$P_{I/O}$  = Power Dissipation on Input and Output Pins — User Determined

For most applications  $P_{I/O} < P_{INT}$  and can be neglected.

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

The total thermal resistance of a package ( $\theta_{JA}$ ) can be separated into two components,  $\theta_{JC}$  and  $\theta_{CA}$ , representing the barrier to heat flow from the semiconductor junction to the package (case), surface ( $\theta_{JC}$ ) and from the case to the outside ambient ( $\theta_{CA}$ ). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

$\theta_{JC}$  is device related and cannot be influenced by the user. However,  $\theta_{CA}$  is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce  $\theta_{CA}$  so that  $\theta_{JA}$  approximately equals  $\theta_{JC}$ . Substitution of  $\theta_{JC}$  for  $\theta_{JA}$  in equation (1) will result in a lower semiconductor junction temperature.

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each inspection lot. Group C and D inspection are performed on a periodic basis in accordance with method 5005 of MIL-STD-883.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each inspection lot as specified in CECC 90110-001. Group C inspection is performed on a periodic basis in accordance with CECC 90110-001.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 1A : Static electrical characteristics for all electrical variants.
- Table 1B : Dynamic electrical characteristics for TS 68000-8 (8 MHz).
- Table 1C : Dynamic electrical characteristics for TS 68000-10 (10 MHz).
- Table 1D : Dynamic electrical characteristics for TS 68000-12 (12.5 MHz).

For static characteristics (table 1A), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to § 5.2 of this specification (tables 1B, 1C and 1D).

Indication of «min.» or «max.» in the column «Test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.3 here above.

5.2 - Test conditions specific to the device

5.2.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of tables 1B, 1C and 1D referring to the loading network number as shown in figures 1A and 1B below.

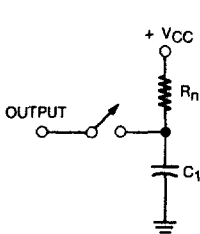


Figure 1A : Passive loads.

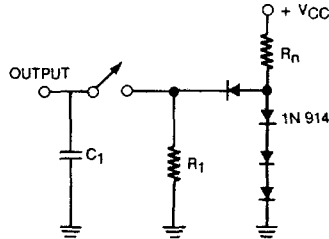


Figure 1B : Active loads.

Load NBR	Figure	R <sub>1</sub>	R <sub>n</sub>	C <sub>1</sub> *	Output application
1	1A	—	910 Ω	130 pF	RESET
2	1A	—	2.9 kΩ	70 pF	HALT
3	1B	6.0 k	1.22 kΩ	130 pF	A1 to A23 $\overline{BG}$ and FC0 to FC2
4	1B	6.0 k	740 Ω	130 pF	All other outputs

\* C<sub>1</sub> includes all parasitic capacitances of test machines.

5.2.2 - Time definitions

The times specified in tables 1B and 1C as dynamic characteristics are defined in figures 2 to 5 below by a reference number given in the column «test number» of the tables together with the relevant «figure number».

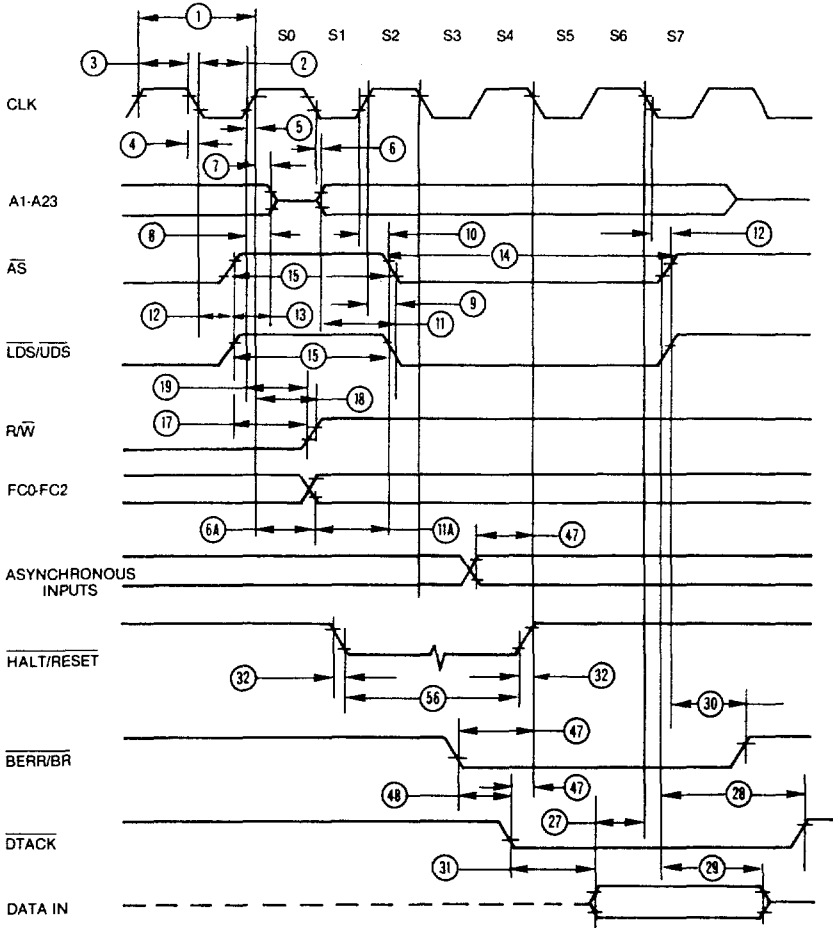


Figure 2 : Read cycle timing.

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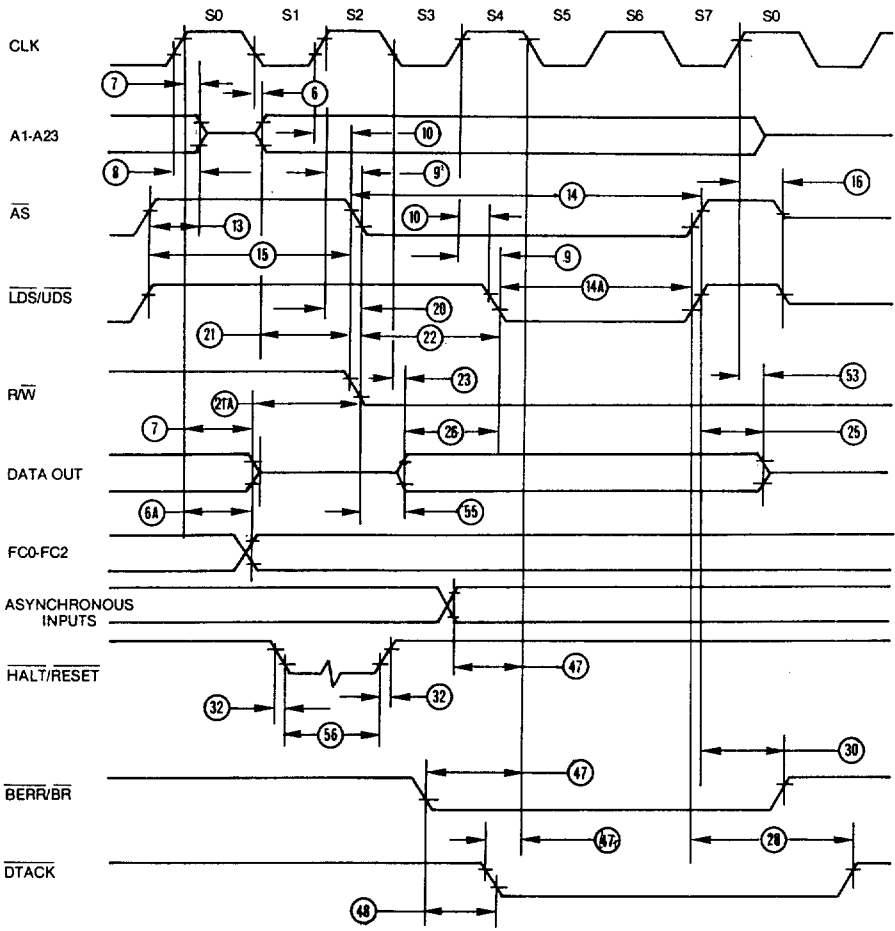


Figure 3 : Write cycle timing.

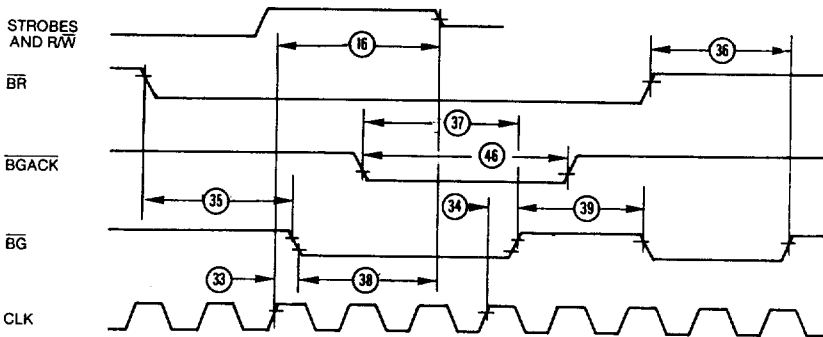


Figure 4 : AC electrical waveforms - bus arbitration.

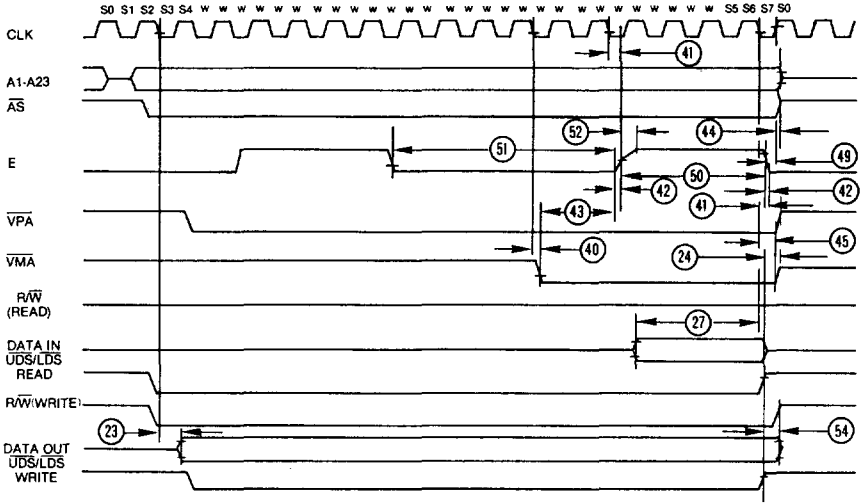


Figure 5: Enable / interface timing.

5.2.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics

Where input pulse generator is loaded by only a 50 Ω resistor, the input pulse characteristics shall be as shown in figure 6.

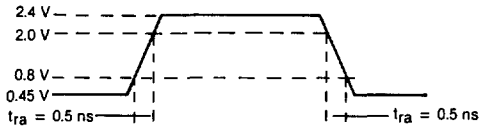


Figure 6: Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be :

$V_{IL} = 0.8 \text{ V}$

$V_{IH} = 2.0 \text{ V}$

c) Time measurement output voltage reference for valid state output

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in figure 7.

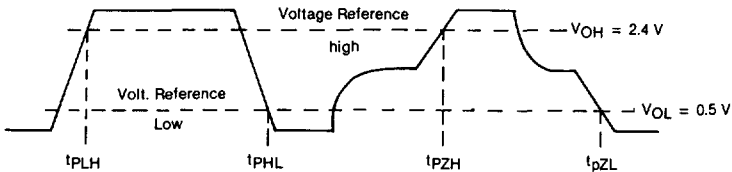


Figure 7: Output voltage references.

5.2.4 - Referred notes to the tables 1x

The following notes shall apply where referred into the tables 1B, 1C and 1D.

**Note 1 :** If the asynchronous setup time (47) requirements are satisfied, the  $\overline{DTACK}$  low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.

**Note 2 :** Where «CLKS» is stated as unit time limit, the reve vant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.

**Note 3 :** For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

**Note 4 :** Actual value depends on actual period.

**Note 5 :** If 47 is satisfied for both  $\overline{DTACK}$  and  $\overline{BERR}$ , 48 may be ignored. In absence of  $\overline{DTACK}$ ,  $\overline{BERR}$  is an asynchronous input using the asynchronous input set up time (47).

**Note 6 :** The processor will negate  $\overline{BG}$  and begin driving the bus again if external arbitration logic negates  $\overline{BR}$  before asserting  $\overline{BGACK}$ .

**Note 7 :** The falling edge of  $\overline{S6}$  triggers both the negation of the strobes ( $\overline{AS}$ , and  $\overline{LDS/UDS}$ ) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

**Note 8 :** When  $\overline{AS}$  and  $\overline{RW}$  are equally loaded ( $\pm 20\%$ ), subtract 10 nanoseconds from the values in these columns.

**Note 9 :** This value should be treated as a minimum for design purpose. For the conformance testing the value shall be regarded as the maximum time.

Table 1A - Static characteristics

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
1	ICC	Supply current	41	VCC = 5.25 V	25°C	—	335	mA
					max			
					min			
2	VOL (1)	Low level output voltage for : A1 to A23 FC0 to FC2 ; $\overline{BG}$	37	VCC = 4.75 V	25°C	—	0.5	V
				IOL = 3.2 mA	max			
				min				
3	VOL (2)	Low level output voltage for : HALT	37	VCC = 4.75 V	25°C	—	0.5	V
				IOL = 1.6 mA	max			
				min				
4	VOL (3)	Low level output voltage for : AS ; RW : D0 to D15 UDS ; LDS ; VMA and E	37	VCC = 4.75 V	25°C	—	0.5	V
				IOL = 5.3 mA	max			
				min				
5	VOL (4)	Low level output voltage for : RESET	37	VCC = 4.75 V	25°C	—	0.5	V
				IOL = 5.0 mA	max			
				min				
6	VOH	High level output voltage for all outputs	37	VCC = 4.75 V	25°C	2.4	—	V
				IOH = -400 $\mu$ A	max			
				min				
7	IIH (1)	High level input current for all inputs excepted HALT and RESET	38	VCC = 5.25 V	25°C	—	2.5	$\mu$ A
				VIN = 5.25 V	max			
				min				
8	IIL (1)	Low level input current for all inputs excepted HALT and RESET	38	VCC = 5.25 V	25°C	- 2.5	—	$\mu$ A
				VIN = 0	max			
				min				
9	IIH (2)	High level input current for : HALT and RESET	38	VCC = 5.25 V	25°C	—	20	$\mu$ A
				VIN = 5.25 V	max			
				min				
10	IIL (2)	Low level input current for : HALT and RESET	38	VCC = 5.25 V	25°C	- 20	—	$\mu$ A
				VIN = 0 V	max			
				min				
11	IOHZ	High level output three-state leakage current for all outputs	—	VCC = 5.25 V	25°C	—	20	$\mu$ A
				VOH = 2.4 V	max			
				min				

(\*) Measurement method : see § 5.1.

Table 1A - Static characteristics (continued)

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
12	I <sub>OLZ</sub>	Low level output three-state leakage current for all outputs	—	V <sub>CC</sub> = 5.25 V V <sub>OL</sub> = 0.4 V	25°C	—	20	μA
					max			
13	V <sub>IH</sub>	High level input voltage for all inputs	—	V <sub>CC</sub> = 4.75 V	25°C	2.0	—	V
					max			
14	V <sub>IL</sub>	Low level input voltage for all inputs	—	V <sub>CC</sub> = 4.75 V	25°C	—	0.8	V
					max			
14A	C <sub>in</sub>	Input capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C	—	25	pF
					max	—	NA	—
					min	—	NA	—
14B	C <sub>out</sub>	Output capacitance (all outputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C	—	20	pF
					max	—	NA	—
					min	—	NA	—
14C	V <sub>test</sub>	Internal protection Transient energy rating		See 5.2 of this DS 5 cycles	25°C	- 500	+ 500	V

(\*) Measurement method : see § 5.1.

Table 1B - Dynamic characteristics - TS 68000-8

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
27	t <sub>SU</sub> (DICL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) f <sub>C</sub> = 8 MHz	25°C	15	—	ns
					max			
					min			
47	t <sub>SU</sub> (SDTCL)	Set-up time DTACK low to clock low (Note 1)	2	Idem test 27	25°C	15	—	ns
					max			
					min			
47	t <sub>SU</sub> (SBRCL)	Set-up time BR low to clock low (Note 1)	2	Idem test 27	25°C	15	—	ns
					max			
					min			
47	t <sub>SU</sub> (SBGCL)	Set-up time BGACK low to clock low (Note 1)	2	Idem test 27	25°C	15	—	ns
					max			
					min			
47	t <sub>SU</sub> (SVPACL)	Set-up time VPA low to clock low (Note 1)	2	Idem test 27	25°C	15	—	ns
					max			
					min			
47	t <sub>SU</sub> (SBERCL)	Set-up time BERR low to clock low (Note 1)	2	Idem test 27	25°C	15	—	ns
					max			
					min			
2	t <sub>w</sub> (CL)	Clock width low	2	Idem test 27	25°C	55	125	ns
					max			
					min			
3	t <sub>w</sub> (CH)	Clock width high	2	Idem test 27	25°C	55	125	ns
					max			
					min			
6A	t <sub>PLH</sub> t <sub>PHL</sub> (CHFCV)	Propagation time clock high to FC valid	2	Idem test 27 Load : 3	25°C	—	70	ns
					max			
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).

Table 1B - Dynamic characteristics - TS 68000-8 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
9	tPHL (CHSLX)	Propagation time clock high to AS low	2	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
9	tPHL (CHSL)	Propagation time CLK high to LDS, UDS low	2	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
12	tPLH (CLSH)	Propagation time CLK low to AS high	2	Idem test 27 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
12	tPLH (CLSH)	Propagation time CLK low to LDS, UDS high	2	Idem test 27 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
18	tPLH (CHRH)	Propagation time CLK high to R/W high	2	Idem test 27 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
20	tPHL (CHRL)	Propagation time CLK high to R/W low	3	Idem test 27 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
23	tPZL tPZH (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
6	tPZL tPZH (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 3	25°C	—	70	ns
					max			
					min			
32	tHRRF	RESET / HALT input transition time	2 - 3	Idem test 27	25°C	—	200	ns
					max			
					min			
33	tPHL (CHGL)	Propagation time CLK high to BG low	4	Idem test 27 Load : 3	25°C	—	70	ns
					max			
					min			
34	tPLH (CHGH)	Propagation time CLK high to BG high	4	Idem test 27 Load : 3	25°C	—	70	ns
					max			
					min			
40	tPHL (CLVM)	Propagation time CLK low to VMA low	5	Idem test 27 Load : 4	25°C	—	70	ns
					max			
					min			
41	tPHL (CLE)	Propagation time CLK low to E low	5	Idem test 27 Load : 4	25°C	—	70	ns
					max			
					min			
8	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C	0	—	ns
					max			
					min			
11	t <sub>su</sub> (AVSL)	Set-up time Address valid to AS, LDS, UDS low	2	Idem test 27 Load : 4	25°C	30 Note 4	—	ns
					max			
					min			
35	tPHL (BRLGL)	Propagation time BR low to BG low	4	Idem test 27 Load : 3	25°C	1.5	3.5 + 90	CLKS Note 2
					max			ns
					min			
37	tPLH (GALEH)	Propagation time BGACK low to BG high	4	Idem test 27 Load : 3	25°C	1.5	3.5 + 90	CLKS Note 2
					max			ns
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).

Table 1B - Dynamic characteristics - TS 68000-8 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
48	$t_{su}$ (BELDAL)	Set-up time BERR low to DTACK low	3	Idem test 27	25°C	20 Note 5	—	ns
					max			
					min			
48	$t_{su}$ (BELDAL)	Set-up time BERR low to DTACK low	2	Idem test 27	25°C	20 Note 5	—	ns
					max			
					min			
26	$t_h$ (DOSL)	Hold time Data-out valid to LDS, UDS low	3	Idem test 27 Load : 4	25°C	30 Note 4	—	ns
					max			
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).

Table 1C - Dynamic characteristics - TS 68000-10

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
27	$t_{su}$ (DICL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) $f_c = 10$ MHz	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{su}$ (SDTCL)	Set-up time DTACK low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{su}$ (SBRCL)	Set-up time BR low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{su}$ (SBGCL)	Set-up time BGACK low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{su}$ (SVPACL)	Set-up time VPA low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{su}$ (SBERCL)	Set-up time BERR low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
2	$t_w$ (CL)	Clock width low	2	Idem test 27	25°C	45	125	ns
					max			
					min			
3	$t_w$ (CH)	Clock width high	2	Idem test 27	25°C	45	125	ns
					max			
					min			
6A	$t_{PLH}$ $t_{PHL}$ (CHFCV)	Propagation time clock high to FC valid	2	Idem test 27 Load : 3	25°C	—	60	ns
					max			
					min			
9	$t_{PHL}$ (CHSLX)	Propagation time clock high to AS low	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
9	$t_{PHL}$ (CHSL)	Propagation time CLK high to LDS, UDS low	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
12	$t_{PLH}$ (CLSH)	Propagation time CLK low to AS high	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).

Table 1C - Dynamic characteristics - TS 68000-10 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
12	t <sub>PLH</sub> (CLSH)	Propagation time CLK low to LDS, UDS high	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
18	t <sub>PLH</sub> (CHRHX)	Propagation time CLK high to R/W high	2	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
20	t <sub>PHL</sub> (CHRL)	Propagation time CLK high to R/W low	3	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
23	t <sub>PZL</sub> t <sub>PZH</sub> (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
6	t <sub>PZL</sub> t <sub>PZH</sub> (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 4	25°C	—	60	ns
					max			
					min			
32	t <sub>HRRF</sub> (CHGL)	RESET / HALT transition time	2 - 3	Idem test 27	25°C	—	200	ns
					max			
					min			
33	t <sub>PHL</sub> (CHGL)	Propagation time CLK high to BG low	4	Idem test 27 Load : 3	25°C	—	60	ns
					max			
					min			
34	t <sub>PLH</sub> (CHGH)	Propagation time CLK high to BG high	4	Idem test 27 Load : 3	25°C	—	60	ns
					max			
					min			
40	t <sub>PHL</sub> (CLVM)	Propagation time CLK low to VMA low	5	Idem test 27 Load : 4	25°C	—	70	ns
					max			
					min			
41	t <sub>PHL</sub> (CLE)	Propagation time CLK low to E low	5	Idem test 27 Load : 4	25°C	—	55	ns
					max			
					min			
8	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C	0	—	ns
					max			
					min			
11	t <sub>su</sub> (AVSL)	Set-up time Address valid to AS, LDS, UDS low	2	Idem test 27 Load : 4	25°C	20 Note 4	—	ns
					max			
					min			
35	t <sub>PHL</sub> (BRLGL)	Propagation time B <sub>R</sub> low to B <sub>G</sub> low	4	Idem test 27 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
37	t <sub>PLH</sub> (GALGH)	Propagation time B <sub>G</sub> ACK low to B <sub>G</sub> high	4	Idem test 27 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
48	t <sub>su</sub> (BELDAL)	Set-up time BERR low to DTACK low	3	Idem test 27	25°C	20 Note 5	—	ns
					max			
					min			
48	t <sub>su</sub> (BELDAL)	Set-up time BERR low to DTACK low	2	Idem test 27	25°C	20 Note 5	—	ns
					max			
					min			
26	t <sub>h</sub> (DOSL)	Hold time Data-out valid to LDS, UDS low	3	Idem test 27 Load : 4	25°C	20 Note 4	—	ns
					max			
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).



Table 1D - Dynamic characteristics - TS 68000-12

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
27	$t_{SU}$ (D1CL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) $f_c = 12$ MHz	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{SU}$ (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{SU}$ (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{SU}$ (SBGCL)	Set-up time BGACK low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{SU}$ (SVPACL)	Set-up time VPA low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
47	$t_{SU}$ (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	2	Idem test 27	25°C	10 Note 9	—	ns
					max			
					min			
2	$t_w$ (CL)	Clock width low	2	Idem test 27	25°C	35	125	ns
					max			
					min			
3	$t_w$ (CH)	Clock width high	2	Idem test 27	25°C	35	125	ns
					max			
					min			
6A	$t_{PLH}$ (CHFCV)	Propagation time clock high to FC valid	2	Idem test 27 Load : 3	25°C	—	55	ns
					max			
					min			
9	$t_{PHL}$ (CHSLX)	Propagation time clock high to $\overline{AS}$ low	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
9	$t_{PHL}$ (CHSL)	Propagation time CLK high to LDS, UDS low	2	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
12	$t_{PLH}$ (CLSH)	Propagation time CLK low to $\overline{AS}$ high	2	Idem test 27 Load : 4	25°C	—	50 Note 3	ns
					max			
					min			
12	$t_{PLH}$ (CLSH)	Propagation time CLK low to LDS, UDS high	2	Idem test 27 Load : 4	25°C	—	50 Note 3	ns
					max			
					min			
18	$t_{PLH}$ (CHRHX)	Propagation time CLK high to R/W high	2	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
20	$t_{PHL}$ (CHRL)	Propagation time CLK high to R/W low	3	Idem test 27 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
23	$t_{PZL}$ (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
6	$t_{PZL}$ (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 4	25°C	—	55	ns
					max			
					min			

(\*) Measurement method : see § 5.1.

Referred notes are given in § 5.2.4 (before Table 1A).

Table 1D - Dynamic characteristics - TS 68000-12 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
32	t <sub>HRRF</sub>	RESET / HALT transition time	2 - 3	Idem test 27	25°C	—	150	ns
					max			
					min			
33	t <sub>PHL</sub> (CHGL)	Propagation time CLK high to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C	—	50	ns
					max			
					min			
34	t <sub>PLH</sub> (CHGH)	Propagation time CLK high to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C	—	50	ns
					max			
					min			
40	t <sub>PHL</sub> (CLVM)	Propagation time CLK low to VMA low	5	Idem test 27 Load : 4	25°C	—	70	ns
					max			
					min			
41	t <sub>PHL</sub> (CLE)	Propagation time CLK low to $\overline{E}$ low	5	Idem test 27 Load : 4	25°C	—	45	ns
					max			
					min			
8	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C	0	—	ns
					max			
					min			
11	t <sub>su</sub> (AVSL)	Set-up time Address valid to $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C	15	—	ns
					max			
					min			
35	t <sub>PHL</sub> (BRLGL)	Propagation time BR low to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
37	t <sub>PLH</sub> (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
48	t <sub>su</sub> (BELDAL)	Set-up time BERR low to DTACK low	3	Idem test 27	25°C	20	—	ns
					max			
					min			
48	t <sub>su</sub> (BELDAL)	Set-up time BERR low to DTACK low	2	Idem test 27	25°C	20	—	ns
					max			
					min			
26	t <sub>h</sub> (DOSL)	Hold time Data-out valid to $\overline{LDS}$ , $\overline{UDS}$ low	3	Idem test 27 Load : 4	25°C	15	—	ns
					max			
					min			

(\*) Measurement method : see § 5.1.  
 Referred notes are given in § 5.2.4 (before Table 1A).

Table 2 - AC electrical specification - clock timing (see Figure 8)

Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f	Frequency of operation	2.0	8.0	2.0	10.0	4.0	12.5	MHz
t <sub>cy</sub>	Cycle time	125	250	100	250	80	250	ns
t <sub>CL</sub> t <sub>CH</sub>	Clock pulse width	55 55	125 125	45 45	125 125	35 35	125 125	ns
t <sub>Cr</sub> t <sub>Cf</sub>	Rise and fall time		10 10		10 10		10 10	ns

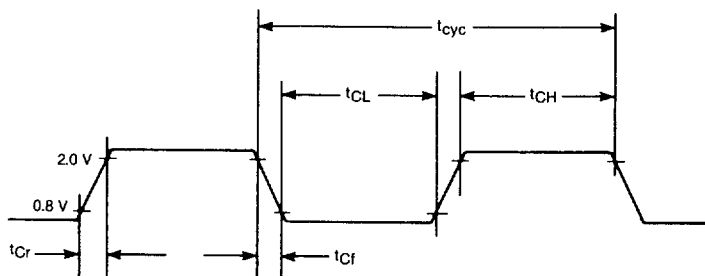


Figure 8 : Clock input timing diagram.

**Note :** Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

## 6 · FUNCTIONAL DESCRIPTION

### 6.1 - General description

The TS 68000 is the first of a family of VLSI microprocessor. It combines state of the art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The TS 68000 is a fully implemented 16-bit microprocessor with 32-bit registers a rich basic instruction set, and versatile addressing modes.

The TS 68000 possesses an asynchronous bus structure with a 24-bit address bus and a 16-bit data bus.

The resources available to the TS 68000 user consist of the following :

- 17 32-bit data and address registers,
- 16 megabyte direct addressing range,
- 56 powerful instruction types,
- operations on five main data types,
- memory mapped I/O,
- 14 addressing modes.

As shown in the programming model (figure 9), the TS 68000 offers seventeen 32-bit registers, a 32-bit program counter, and a 16-bit status register. The first eight registers (D0-D7) are used as data register for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the system stack pointers may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 17 registers may be used as index registers.

The status register (figure 10) contains the interrupt mask (eight levels available) as well as the condition code extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

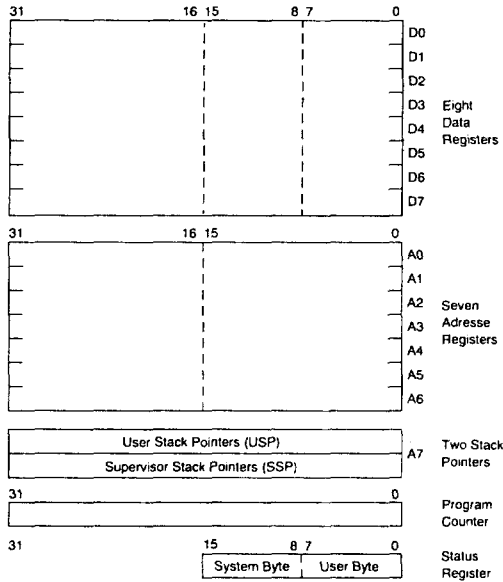


Figure 9 : Programming model.

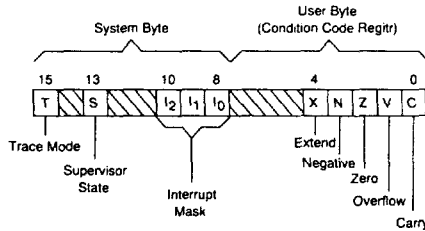


Figure 10 : Status register.

6.2 - Memory organization

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in figure 11. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

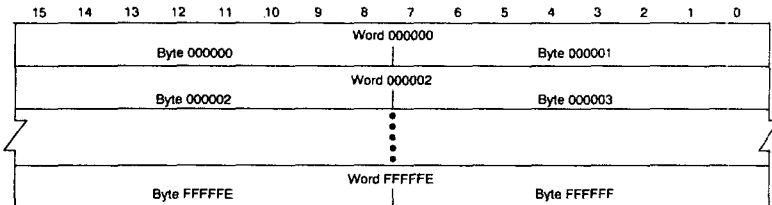
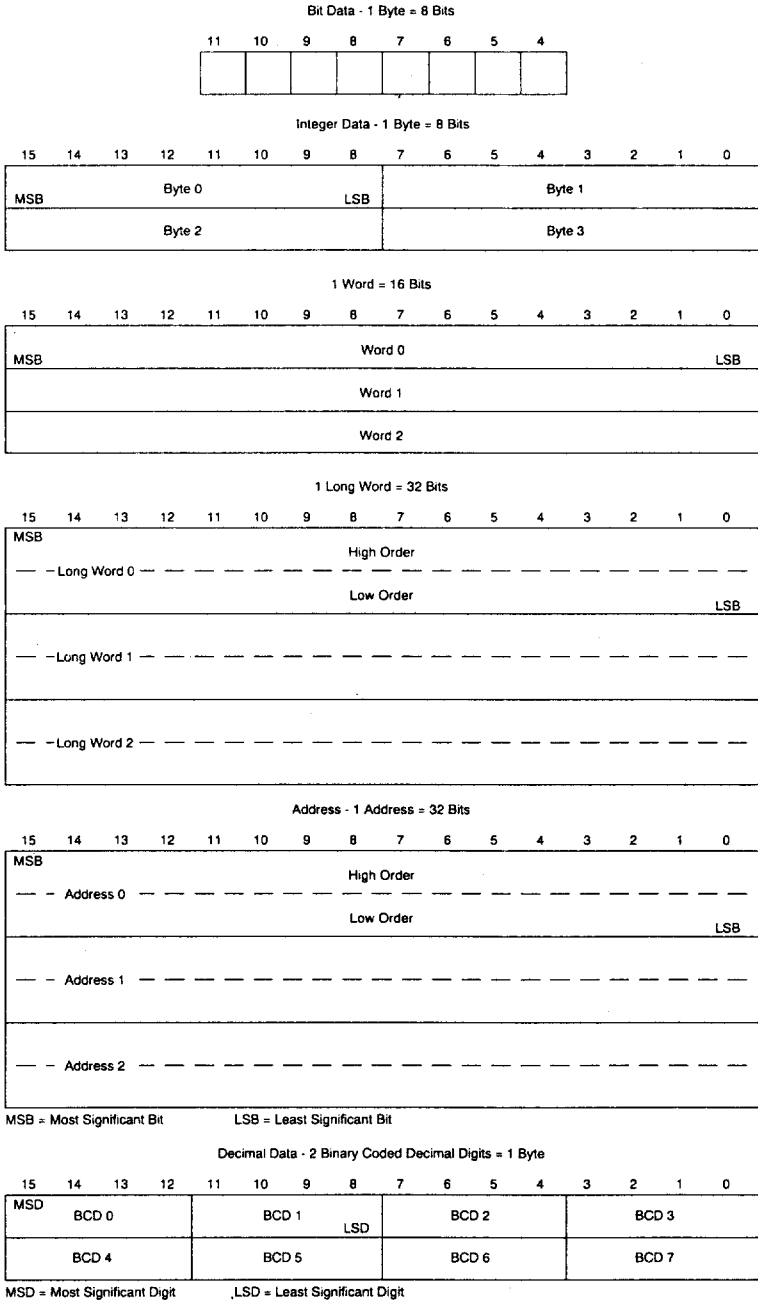


Figure 11 : Word organization in memory.

The data types supported by TS 68000 are : bit data, integer data of 8, 16 or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in figure 12. The numbers indicate the order in which the data would be accessed from the processor.



5

Figure 12: Memory data organization.

**6.3 - Addressing modes and data types**

Five basic data are supported. These data types are :

- Bits,
- BCD Digits (4 bits),
- Bytes (8 bits),
- Words (16 bits),
- Long Words (32 bits).

In addition, operations on other data types such as memory addresses, status word data, etc... are provided in the instruction set.

The 14 address modes, shown in table 3, include six basic types :

- Register Direct,
- Register Indirect,
- Absolute,
- Program Counter Relative,
- Immediate,
- Implied.

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

**Table 3 - Addressing modes**

Mode	Generation
<b>Register direct addressing</b> Data register direct Address register direct	EA = Dn EA = An
<b>Absolute data addressing</b> Absolute short Absolute long	EA = (Next word) EA = (Newt two words)
<b>Program counter relative addressing</b> Relative with offset Relative with index and offset	EA = (PC) + d <sub>16</sub> EA = (PC) + (Xn) + dg
<b>Register indirect addressing</b> Register indirect Postincrement register indirect Predecrement register indirect Register indirect with offset Indexed register indirect with offset	EA = (An) EA = (An), An ← An + N An ← An - N, EA = (An) EA = (An) + d <sub>16</sub> EA = (An) + (Xn) + dg
<b>Immediate data addressing</b> Immediate Quick immediate	DATA = Next word(s) Inherent data
<b>Implied addressing</b> Implied register	EA = SR, USP, SP, PC
<b>Notes :</b> EA : Effective Address. An : Address Register. Dn : Data Register. Xn : Address or Data Register Used as Index Register. SR : Status Register. PC : Program Counter. ( ) : Contents of. dg : 8-Bit Offset (Displacement). d <sub>16</sub> : 16-Bit Offset (Displacement). N : 1 for byte, 2 for word, and 4 for long word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundary. ← : Replaces.	

## 6.4 - Instruction set overview

The TS 68000 instruction set is shown in table 4. Some additional instructions are variations, or subsets, of these and they appear in table 5. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can be used any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, «quick» arithmetic operations, BCD arithmetic, and expanded operation (through traps).

Table 4 - Instruction set summary

Mnemonic	Description
ABCD ADD AND ASL ASR	Add Decimal With Extend Add Logical And Arithmetic Shift Left Arithmetic Shift Right
Bcc BCHG BCLR BRA BSET BSR BTST	Branch Conditionally Bit Test and Change Bit Test and Clear Branch Always Bit Test and Set Branch to Subroutine Bit Test
CHK CLR CMP	Check Register Against Bounds Clear Operand Compare
DBcc DIVS DIVU	Test Condition, Decrement and Branch Signed Divide Unsigned Divide
EOR EXG EXT	Exclusive Or Exchange Registers Sign Extend
JMP JSR	Jump Jump to Subroutine
LEA LINK LSL LSR	Load Effective Address Link Stack Logical Shift Left Logical Shift Right

Mnemonic	Description
MOVE MULS MULU	Move Signed Multiply Unsigned Multiply
NBCD NEG NOP NOT	Negate Decimal with Extend Negate No Operation One's Complement
OR	Logical Or
PEA	Push Effective Address
RESET ROL ROR ROXL ROXR RTE RTR RTS	Reset External Devices Rotate Left without Extend Rotate Right without Extend Rotate Left with Extend Rotate Right with Extend Return from Exception Return and Restore Return from Subroutine
SBCD Scc STOP SUB SWAP	Subtract Decimal with Extend Set Conditional Stop Subtract Swap Data Register Halves
TAS TRAP TRAPV TST	Test and Set Operand Trap Trap on Overflow Test
UNLK	Unlink

Table 5 - Variation of instruction types

Instruction type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR  ANDI to SR	Logical And And Immediate And Immediate to Condition Codes And Immediate to Status Register
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR  EORI to SR	Exclusive Or Exclusive Or Immediate Exclusive Or Immediate to Condition Codes Exclusive Or Immediate to Status Register

Instruction type	Variation	Description
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVEA to CCR MOVE USP	Move Move Address Move Multiple Registers Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR  ORI to SR	Logical Or Or Immediate Or Immediate to Condition Codes Or Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

### 6.5 - Designation of the terminals

The function, category and relevant symbol of each terminal of the device are given in the following table 6.

Table 6

Symbol	Function	Category
VCC	Power supply (2 terminals)	Supply terminals
VGND	Power supply (2 terminals)	
FC0 to FC2	Processor status	Outputs
IPL0 to IPL2	Interrupt control	Inputs
A1 to A23	Address Bus	Outputs
AS	Asynchronous Bus Control	Outputs
R / W		
UDS		
LDS		
DTACK		Input
BR	Bus arbitration Control	Inputs
BGACK		Output
BERR	System control	Input
RESET		Input / Output
HALT		
VPA	6800 peripheral control	Input
VMA		Output
E		Output
CLK	Clock	Input
D0 to D15	Data Bus	Input / Output
(*) VSS is the reference terminal for the voltages.		

### 6.6 - Initialisation of the device

#### 6.6.1 - Power supply sequencing

VCC and VGND have to be connected before power supply VCC increases to the full operational value.

In addition, for power up, the microprocessor TS 68000 shall be held with low level to the RESET for at least 100 milliseconds to allow stabilisation of the die circuitry.

#### 6.6.2 - Initialisation procedure after power up

The microprocessor TS 68000 is initialised by only application of low level to the RESET input during at least 10 clock periods after VCC has reached its operating value.

### 6.7 - Detailed block diagram

The functional block diagram is given in figure 13 below.

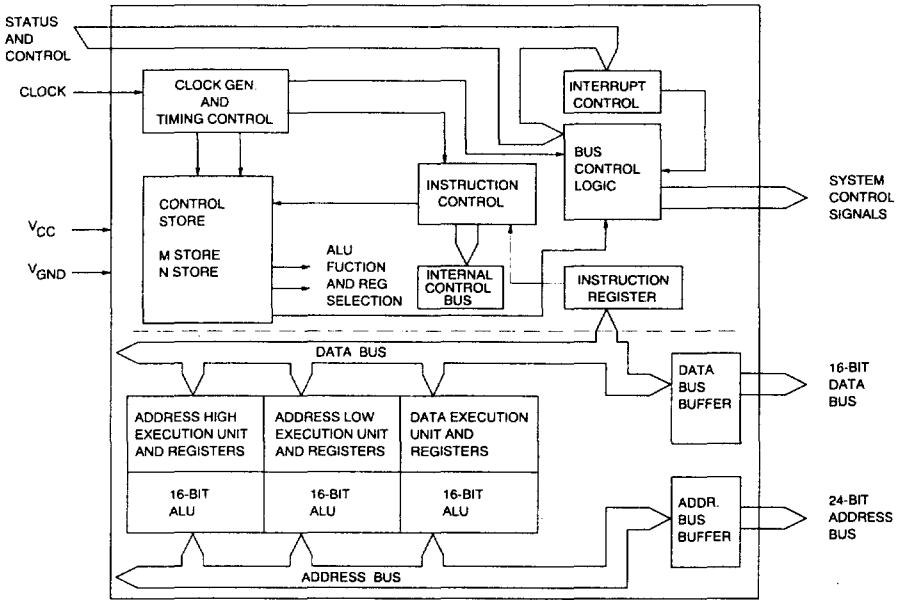


Figure 13 : Block diagram.

6.8 - Signal description

The input and output signals can be functionally organized into the groups shown in figure 14.

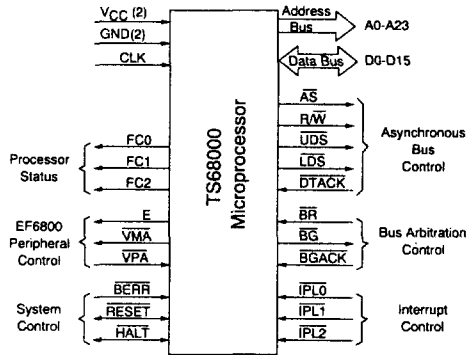


Figure 14 : Input and output signals.

6.9 - Interface with 6800 peripherals

Extensive line of 6800 peripherals are directly compatible with the TS 68000.

**Note :** It is the own user's responsibility to verify the actual 6800 peripheral performances to be compatible to the actual used TS 68000 microprocessor performances.

Some of 6800 peripherals that are particularly useful are :

- 6821 Peripheral interface adapter,
- 6840 Programmable timer module,
- 6850 Asynchronous communications interface adapter,
- 6852 Synchronous serial data adapter,
- 6854 Advanced data link controller.

To interface the synchronous 6800 peripherals with the asynchronous TS 68000, the processor modifies its bus cycle to meet the 6800 cycle requirements whenever an 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 15 is a flowchart of the interface operation between the processor and 6800 devices.

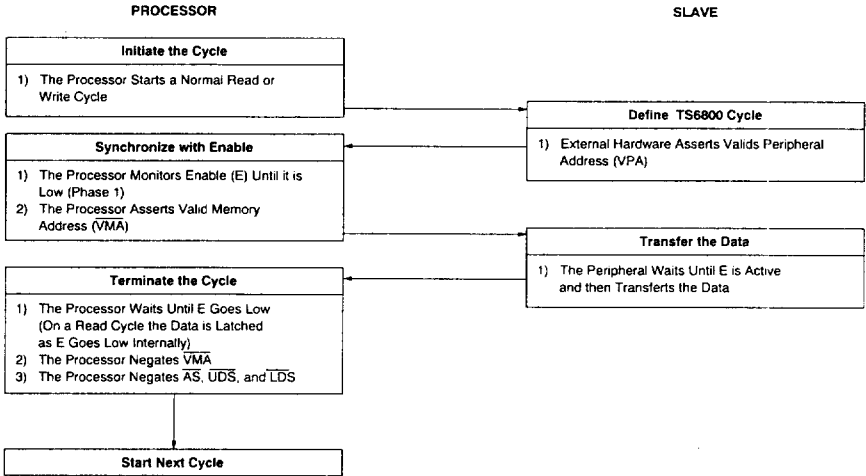


Figure 15 : 6800 interfacing flowchart.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

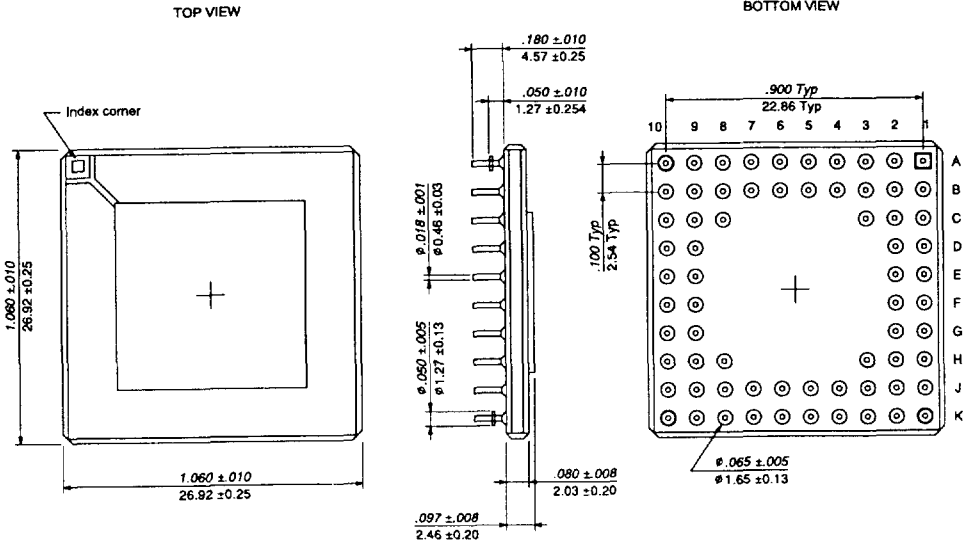
8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

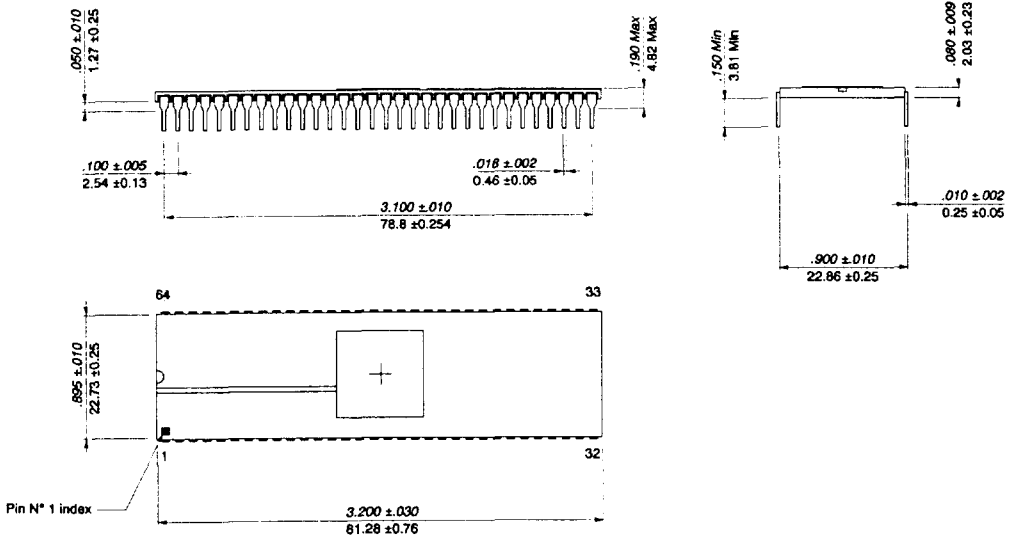
- a) Device should be handled on benches with conductive and grounded surface.
- b) Ground test equipment, tools and operator.
- c) Do not handle devices by the leads.
- d) Store devices in conductive foam or carriers.
- e) Avoid use of plastic, rubber, or silk in MOS areas.
- f) Maintain relative humidity above 50 %, if practical.

9 - PACKAGE MECHANICAL DATA

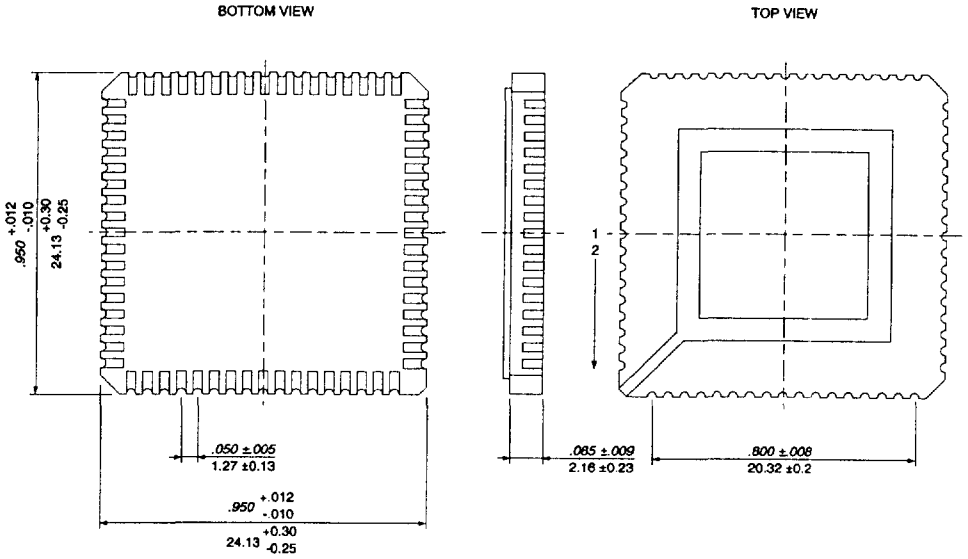
9.1 - 68 pins - Pin Grid Array



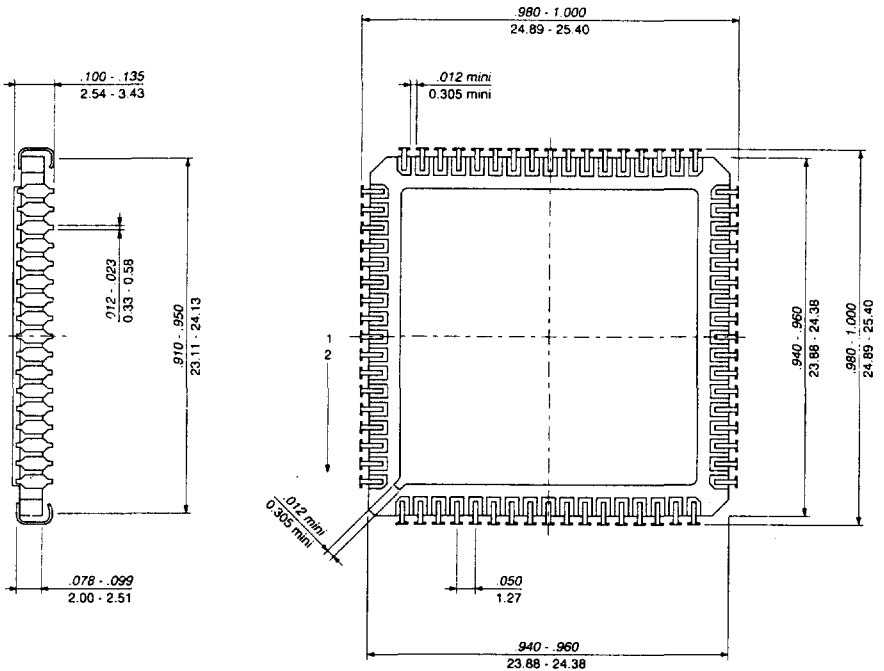
9.2 - 64 pins - Ceramic Side Brazed Package



9.3 - 68 pins - Leadless Ceramic Chip Carrier

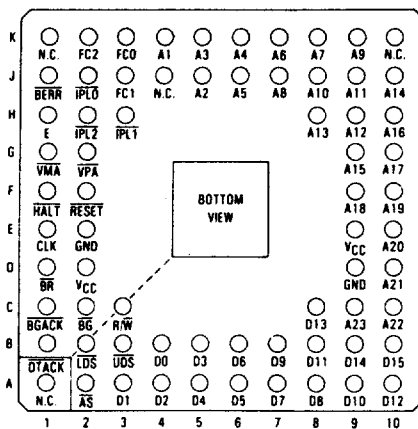


9.4 - 68 pins - Leaded Ceramic Chip Carrier (on request only)

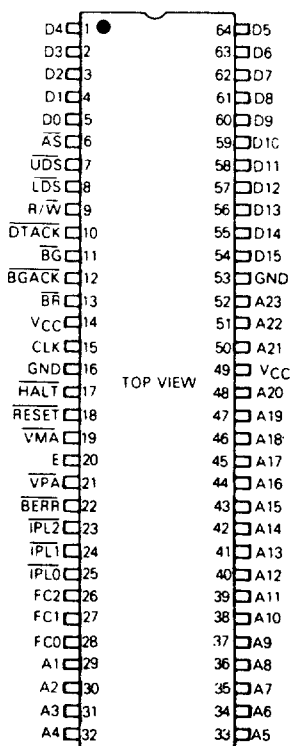


10 - TERMINAL CONNECTIONS

10.1 - 68 pins - Pin Grid Array

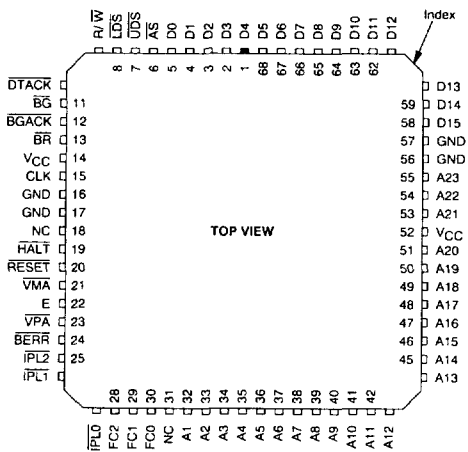


10.2 - 64 pins - Ceramic DIL



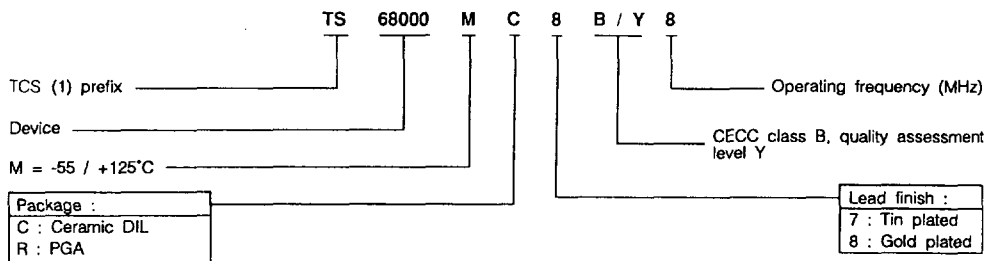
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10.3 · 68 pins · Leaded and Leadless Ceramic Chip Carrier

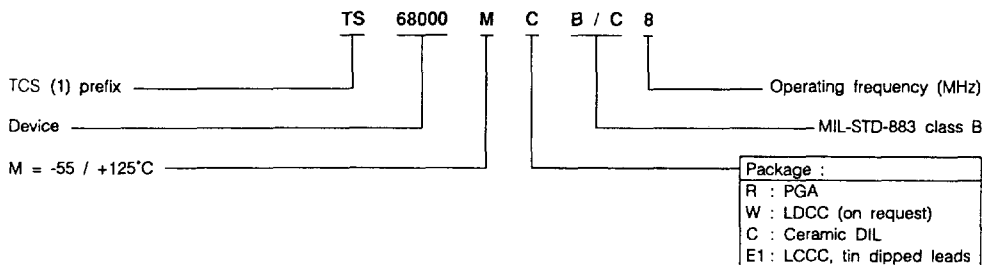


11 - ORDERING INFORMATION

11.1 - CECC (CECC spec number is 90110-001)

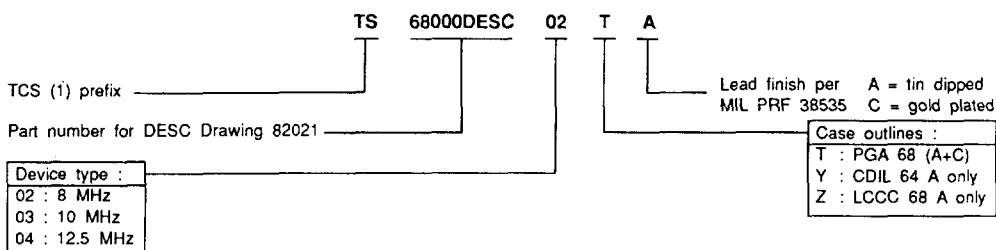


11.2 - MIL-STD-883

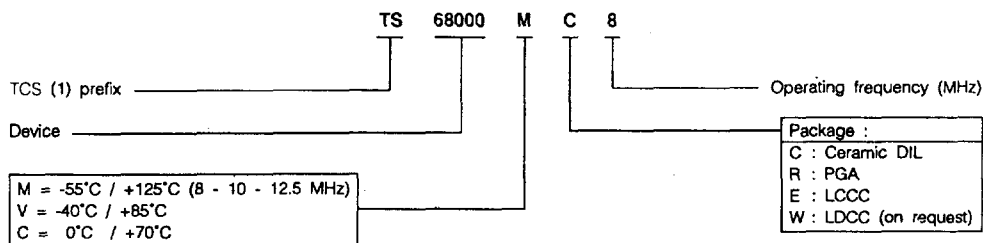


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11.3 - DESC



11.4 - Standard product



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES