

# 54F/74F784

## 8-Bit Serial-Parallel Multiplier With Adder/Subtractor

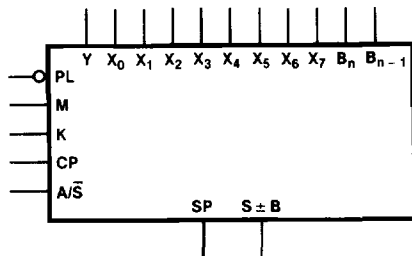
### Description

The 'F784 is a serial (nx8)-bit multiplier with a final stage adder/subtractor for optional use in adding a B bit to obtain  $S \pm B$ . A ( $B_{n-1}$ )-bit can also be added via an internal flip-flop to achieve a 1-bit delay. The x word is parallel loaded (eight bits wide) into latches and the y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in Fast Fourier Transforms.

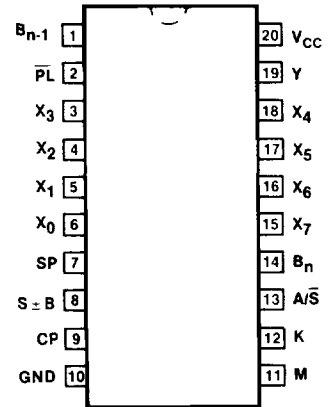
- **Twos Complement Multiplication**
- **Cascadable for any Number of Bits**
- **Full Adder and B-1 Input Included for Maximum Flexibility**
- **Maximum Clock Frequency 50 MHz Guaranteed**
- **Supply Current 100 mA Max**

**Ordering Code:** See Section 5

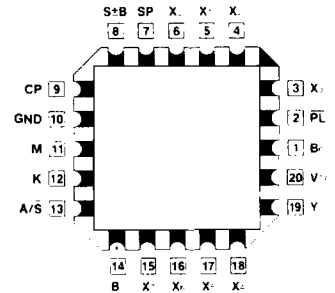
### Logic Symbol



### Connection Diagrams



**Pin Assignment for DIP and SOIC**



**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
X <sub>0</sub> -X <sub>7</sub>	Multiplicand Data Inputs	0.5/0.375
Y	Serial Multiplier Input	0.5/0.375
CP	Clock Pulse Input	0.5/0.375
K	Serial Expansion Input	0.5/0.375
M	Mode Control Input	0.5/0.375
PL	Parallel Load Input	0.5/0.75
A/S	Add/Subtract	0.5/0.375
SP	Serial X•Y Product Output	25/12.5
S ± B	Serial X•Y ± B Output	25/12.5
B <sub>n</sub>	Serial B Input	0.5/0.375
B <sub>n-1</sub>	Delayed Serial B Input	0.5/0.375

## Functional Description

The 'F784 is a serial-parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

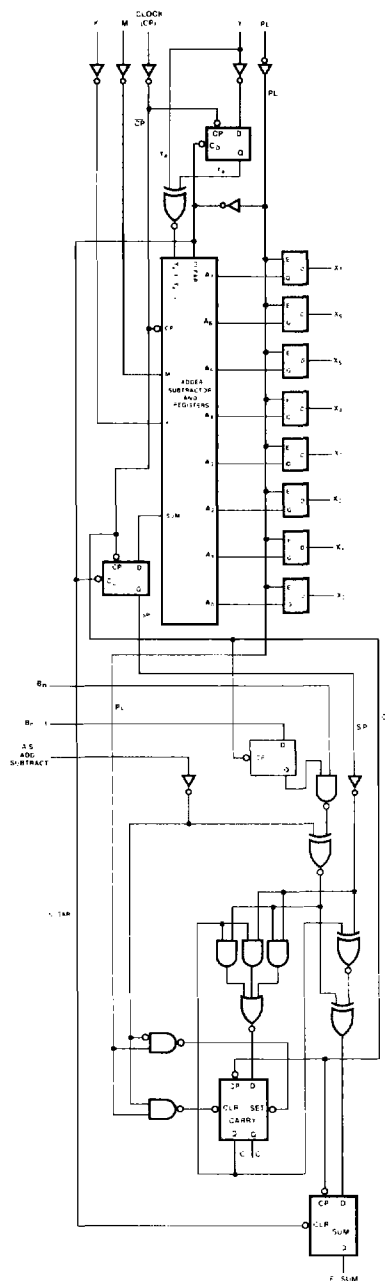
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the  $S_0$  output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product  $XY$  and the product  $XY \pm B$ . Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a  $B_{n-1}$  input is provided which delays the B data by one clock cycle. Thus, a valid output results.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**DC Characteristics over Operating Temperature Range** (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
$I_{CC}$	Power Supply Current		67	100	mA	$V_{CC} = \text{Max}$

**AC Characteristics:** See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	50	65			50		MHz	3-1	
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{PL}}$ to SP	6.0	10.0	13.0		5.0	14.5	ns	3-1 3-11	
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{PL}}$ to $S \pm B$	5.5	9.5	12.0		4.5	13.5	ns	3-1 3-11	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to SP	4.0	6.5	9.0		3.5	10.0	ns	3-1 3-7	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $S \pm B$	4.0	7.0	9.0		3.5	10.0	ns	3-1 3-7	

## AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$	$T_A, V_{CC} =$ Mil	$T_A, V_{CC} =$ Com		
		Min Typ Max	Min Max	Min Max		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW K to CP	13.0 9.0		14.0 10.0	ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW K to CP	0 1.0		0 1.0		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW Y to CP	15.0 15.0		16.0 16.0	ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW Y to CP	1.5 1.5		1.5 1.5		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW X to $\overline{\text{PL}}$	5.0 5.0		6.0 6.0	ns	3-14
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW X to $\overline{\text{PL}}$	2.0 2.0		2.0 2.0		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW $B_n$ to CP	7.0 7.0		8.0 8.0	ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $B_n$ to CP	0 0		0 0		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW $A/\overline{\text{S}}$ to CP	12.0 12.0		13.0 13.0	ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $A/\overline{\text{S}}$ to CP	1.5 1.5		1.5 1.5		
$t_s(\text{H})$ $t_s(\text{L})$	Set up Time, HIGH or LOW $B_{n-1}$ to CP	4.0 4.0		5.0 5.0	ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $B_{n-1}$ to CP	0 0		1.0 1.0		
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	5.0		6.0	ns	3-11
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	5.0 5.0		6.0 6.0	ns	3-7
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to CP	6.5		7.5	ns	3-11