National Semiconductor

Electronic Data Processing

MM5303 Universal Fully Asynchronous Receiver/Transmitter

General Description

The MM5303 is a fully asynchronous receiver/transmitter, fabricated with National's metal-gate, depletion load, PMOS technology. All inputs and outputs are fully TTL compatible, requiring no external resistors or level shifting.

This device is a programmable interface between an asynchronous serial data channel and a parallel data channel. The transmitter section converts parallel data into a serial word which includes: start bit, data, parity bit (if selected), and stop bit(s). The receiver converts a serial word of the same format into a parallel one and automatically checks start bit, parity (if selected), and stop bit(s).

Both transmitter and receiver are doubly buffered; in addition, received data out and status words may be TRI-STATED, facilitating bus configurations.

Status conditions are: transmission complete, Tx buffer register empty, Rx data available, parity error, framing error, and over-run error.

The MM5303 is fully programmable. It can operate full or half duplex, transmitting and receiving simultaneously at different baud rates; word length may be 5, 6, 7 or 8 bits; parity generation/checking may be even, odd or inhibited; the number of stop bits may be either 1 or 2, with 1 1/2 bits when transmitting a 5 bit code.

Features

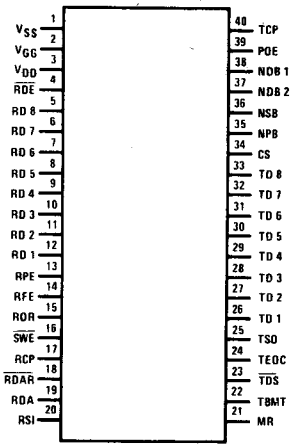
- Low power
- High speed
- Fully externally programmable:
  - Word length
  - Parity mode
  - Number of stop bits
- Fully double buffered eliminating need for precise synchronization
- Full or half duplex operation
- Direct TTL/DTL compatibility
- Automatic data received/transmitted status generation
- TRI-STATE outputs
- Automatic start bit generation/verification
- Internal pull-ups on all inputs

Applications

- Peripherals
- Terminals
- Mini computers
- Facsimile transmission
- Modems
- Concentrators
- Asynchronous data multiplexers
- Card and tape readers
- Printers
- Data sets
- Controllers
- Keyboard encoders
- Remote data acquisition systems
- Asynchronous data cassettes

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5303N
See Package 24

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	V_{SS} − 25V/V_{SS} + 0.3V*
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Outputs should not have more than V_{SS} − 15V

DC Electrical Characteristics

T_A within operating temperature range, V_{SS} = 5V ±5%, V_{DD} = 0V, V_{GG} = −12V ±5% unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Input Voltage Levels	(Note 3)	V_{SS}−1.5		V_{SS}+0.3	V
V_{IL}	Low Input Voltage Levels		V_{DD}		0.8	V
V_{OH}	High Output Voltage Levels	I_{OH} = −100μA	2.4			V
V_{OL}	Low Output Voltage Levels	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High Level Input Current Levels	V_{IN} = V_{SS}			10	μA
I_{IL}	Low Level Input Current Levels	V_{IN} = 0.4V, V_{SS} = 5.25V			1.6	mA
I_{OL}	Output Leakage Current Level	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, $0 \leq V_{OUT} \leq 5V$			−1	μA
I_{OS}	Output Short Circuit Current Level	V_{OUT} = 0V, (Note 4)			25	mA
C_{IN}	Input Capacitance	(Note 2)				
	All Inputs	V_{IN} = V_{SS}, f = 1 MHz		5	10	pF
C_{OUT}	Output Capacitance					
	All Outputs	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, f = 1 MHz		10	20	pF
I_{SS}	Power Supply Current	All Inputs at V_{SS}		13	25	mA
I_{GG}	Power Supply Current	All Inputs at V_{SS}		6	15	mA

AC Electrical Characteristics at 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Clock Frequency	RCP, TCP	dc		500	kHz
t_{PW}	Pulse Width					
	Clock	RCP, TCP	1			μs
	Master Reset	MR	5			μs
	Control Strobe	CS	1			μs
	Tx Data Strobe	$\overline{TDS}$	300			ns
	Rx Data Available Reset	$\overline{RDAR}$, (Note 5)	200			ns
t_C	Coincidence Time	$\overline{TDS}$	300			ns
		CS	1			μs
t_{SET}	Input Set-Up Time	TD1–TD8	0			ns
		NPB, NSB, NDB, POE	0			ns
t_{HOLD}	Input Hold Time	TD1–TD8	300			ns
		NPB, NSB, NDB, POE	0			ns
t_{pd0}	Output Propagation Delay to Low State	$\overline{RDE}$, $\overline{SWE}$ Enable to Outputs Low			500	ns
t_{pd1}	Output Propagation Delay to High State	$\overline{RDE}$, $\overline{SWE}$ Enable to Outputs High			500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

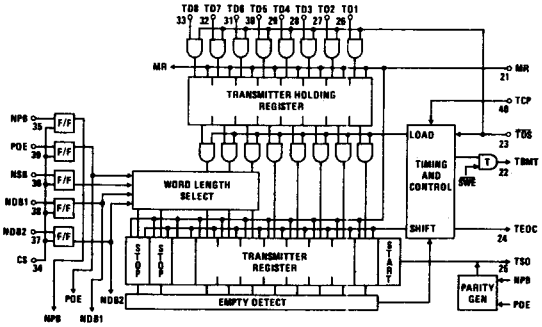
Note 2: Capacitance is guaranteed by periodic testing.

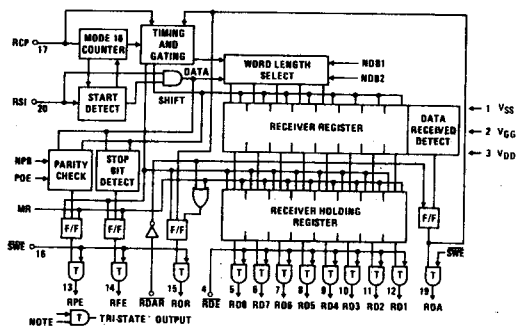
Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: Only one output should be shorted at a time.

Note 5: Refer to Receiver Timing diagram for detail.

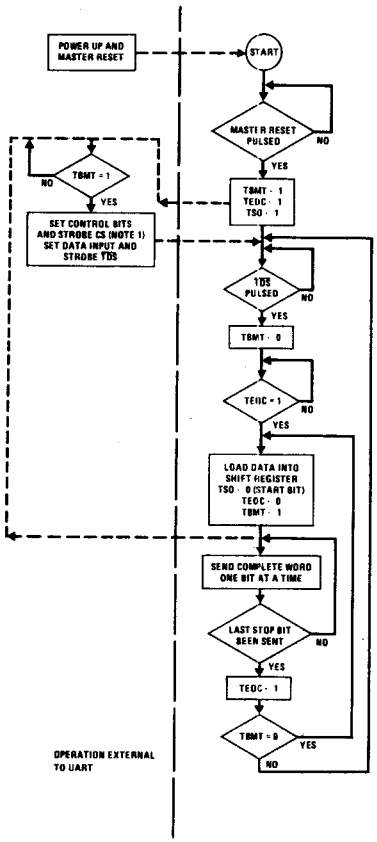
Functional Block Diagrams



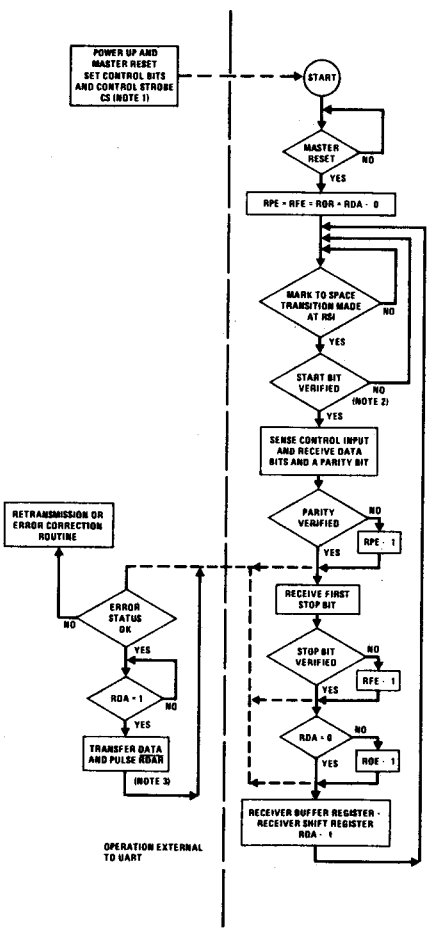


Flow Charts

Transmitting Sequence



Receiving Sequence



Note 1: Control Strobe should be made only at the beginning of transmission and remain inactive during transmission. It may be tied high if no change is necessary.

Note 2: The line must stay low for 8 RCP pulses to be verified.

Note 3: $\overline{\text{RDAR}} \leftarrow 0$ will cause RDA $\leftarrow$ 0, refer to receiver timing for detail.

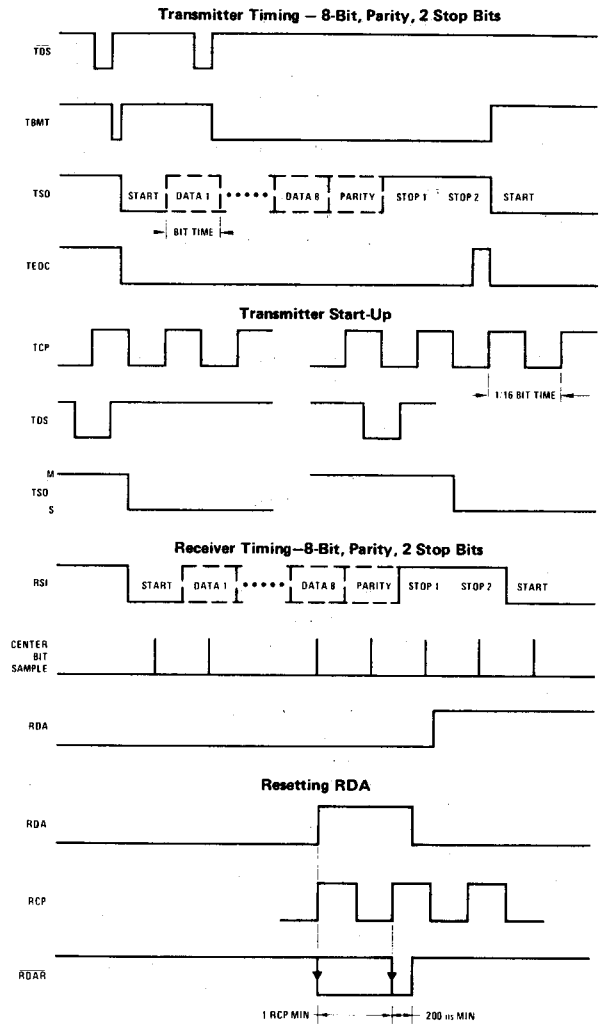
Pin Functions

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{SS}	Power Supply	+5V supply
2	V_{GG}	Power Supply	−12V supply
3	V_{DD}	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8–RD1) of the receiver buffer register.
5–12	RD8–RD1	Receiver Data Outputs	These are the 8 TRI-STATE data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e., the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.
15	ROR	Receiver Over Run Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable Input	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset Input	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register is empty and may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe Input	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character Output	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one full TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26–33	TD1–TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines,as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe Input	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.
36	NSB	Number of Stop Bits	This input selects the number of stop bits, 1, 1 1/2, or 2 to be transmitted. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits, except when 5-bit data is selected, then 1 1/2 stop bits will occur.

Pin Functions (cont'd)

PIN NO.	SYMBOL	NAME	FUNCTION
37–38	NDB2, NDB1	Number of Data Bits/ Character	These 2 inputs are internally decoded to select either 5, 6, 7 or 8 data bits/ character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

Timing Diagrams

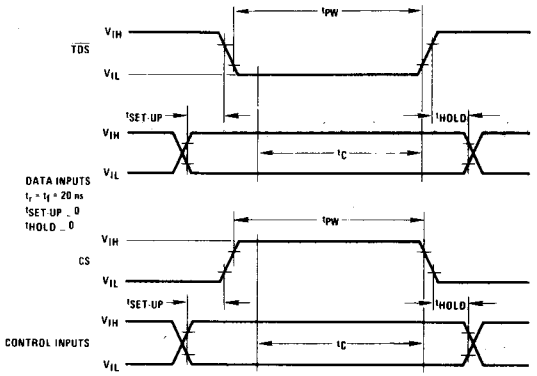


Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of $\overline{TDS}$.

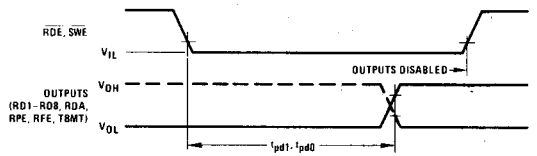
$\overline{RDAR}$ may go low any time after the RDA comes up but must stay low for at least 200 ns after the first clock pulse period. $\overline{RDAR}$ may be hard wired low, in which case RDA will go high and remain high for the duration of the positive clock pulse.

Timing Diagrams (cont'd)

Data/Control Timing Diagram

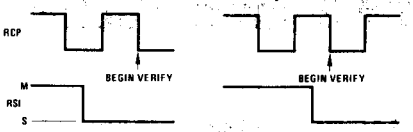


Output Timing Diagram



Note: Waveform drawings not to scale for clarity.

Start Bit Detect/Verify



If the RSI line remains spacing for 1/2 a bit time, a genuine start bit is verified. Should the line return to a marking condition prior to 1/2 a bit time, the start bit verification process begins again.