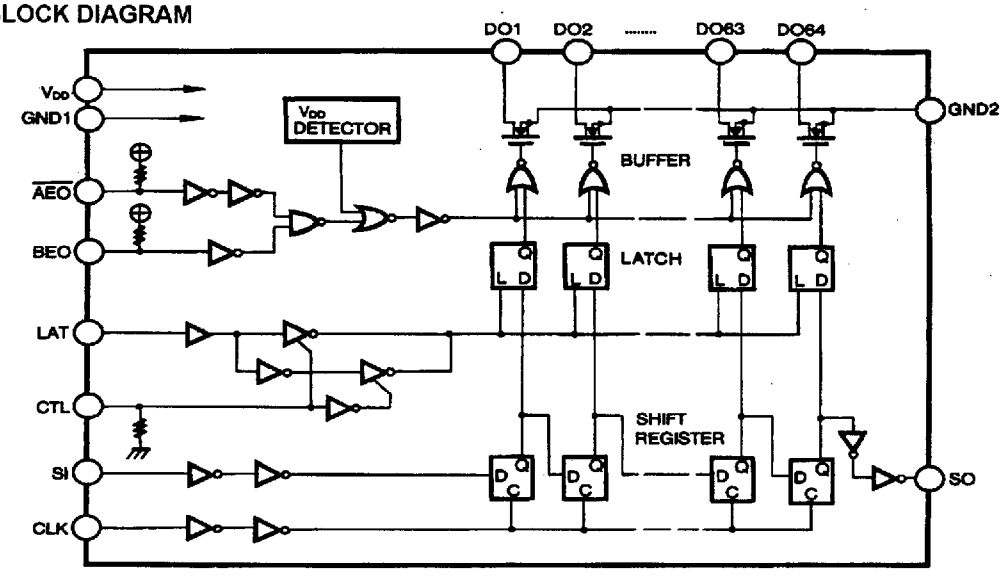
INTRODUCTION

The KS0054C is a low power CMOS 64-Bit Thermal Printer Head Driver. It contains a 64-Bit high speed shift register, 64-Bit latches output control circuit and 64-Bit drivers with a driver capability of 30V/10mA. Allowing direct connection with Thermal Printer Heads.

FEATURES

- **Built in 64-Bit Static Shift Register**
- **Built in 64-Bit Latches**
- **Built in Output Control Circuit and 64-Bit Latches**
- **Output Off Function when Detect Low Supply Voltage**
- **High Supply Voltage for Driver ..... 30V (max)**
- **Low Operating Current ..... 10mA (max)**
- **High Speed Operation ..... 0.3mA / 2MHz (typ)**
- **High Speed Operation ..... 5MHz (max)**
- **Si-Gate CMOS Process**

BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	I/O	Description
CLK	I	Clock input for Static Shift Register
SI	I	Serial Data Input (H : Blank, L : White)
SO	O	Serial Data Output from Shift Register
CTL	I	Change the Polarity of the Latch Signal
LATCH	I	Data Latch Input —CTL is L State L : Parallel Data Input, H : Latch —CTL is H State L : Latch, H : Parallel Data Input
$\overline{AEO}$	I	Data Output Disable Input H : DO_n Terminals are in the High Impedance State
BEO	I	Data Output Disable Input L : DO_n Terminals are in the High Impedance State
DO_n	O	Parallel Data Output Terminals
V_{DD}	—	Logic Power (+ 5V)
GND1	—	Logic GND (0V)
GND2	—	Output (DO_n) GND(0V)

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.5 ~ 7.0	V
Input Voltage	V_{IH}	- 0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	-20 ~ 20	mA
Output Voltage(SO)	V_{OSO}	- 0.5 ~ V_{DD}+ 0.5	V
Output Voltage (DO_n)	V_{ODOn}	30	V
Output Current(DO_n)	I_{ODOn}	12	mA
Operating Temperature	T_{OPR}	- 10 ~ 80	℃
Junction Temperature	T_J	125	℃

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Input Voltage	V_{IH}	—	0	—	—	V
Output High Voltage(DO_n)	V_{OH}	I_{OH} = 20μA	—	24	26	V
Output Low Current(DO_n)	I_{OL}	—	8	10	—	mA
Clock Frequency	f_{CLK}	—	—	2	5	MHz
Clock Pulse Width	$t_{W(CLK)}$	Refer to Timing Chart	70	—	—	ns
Set-up Time(CLK-SI)	$t_{ST(CLK-SI)}$		50	—	—	ns
Set-up Time(CLK-LAT)	$t_{ST(CLK-LAT)}$		100	—	—	ns
Latch Pulse Width	$t_{W(LAT)}$		100	—	—	ns
Hold Time(CLK-SI)	$t_{H(CLK-SI)}$		10	—	—	ns
Hold Time(CLK-LAT)	$t_{H(CLK-LAT)}$		50	—	—	ns
Operating Temperature	T_{ORP}	—	-10	—	80	℃

DC ELECTRICAL CHARACTERISTICS

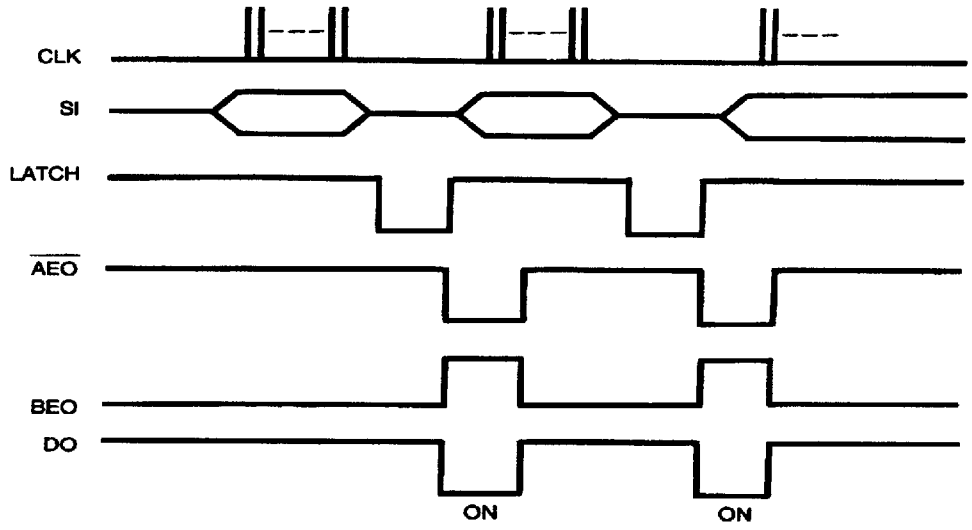
(V_{DD} = 5V, Ta = 25℃)

Characteristic	Symbol	Pad Name	Test Conditions	Min	Typ	Max	Unit
High Input Voltage	V_{IH}	CLK,CTL,LAT $\overline{AEO}$,BEO,SI	—	3.5	—	5.0	V
Low Input Voltage	V_{IL}	CLK,CTL,LAT $\overline{AEO}$,BEO,SI	—	0	—	1.5	V
High Input Current	I_{IH1}	CLK,LAT,SI $\overline{AEO}$,BEO	V_{IH} = 5.0V	—	—	0.5	μA
	I_{IH2}	CTL		8	17	35	μA
Low Input Current	I_{IL1}	CLK,CTL,LAT,SI	V_{IL} = 0V	-0.5	—	—	μA
	I_{IL2}	$\overline{AEO}$,BEO		-35	-17	-8	μA
High Output Voltage	$V_{OH(SO)}$	SO	V_{DD} = 4.5V	4.45	—	—	V
Low Output Voltage	$V_{OL(SO)}$	SO	Output Open	—	—	0.05	V
High Output Current	$I_{OH(SO)}$	SO	V_{OH} = V_{DD} - 0.4V	0.5	1.0	—	mA
Low Output Current	$I_{OL(SO)}$	SO	V_{OL} = 0.4V	0.5	1.0	—	mA
Low Output Voltage	$V_{OL(DO)}$	DO_n	$I_{OL(DO)}$ = 10mA	—	1.0	1.5	V
Low Output Current	$I_{OL(DO)}$	DO_n	$V_{OL(DO)}$	8	10	—	mA
Supply Current	I_{DD1}	V_{DD}	f_{CLK} = 5MHz SI = FIX	—	0.3	1.0	mA
	I_{DD2}		f_{CLK} = 5MHz SI = FIX	—	1.0	3.0	mA
	I_{DD3}		f_{CLK} = 5MHz f_{SI} = 1/2f_{CLK}	—	3.0	7.0	mA
Low Voltage	$V_{L(DET)}$	V_{DD}	V_{DD} = 5V→0V	3.0	—	4.2	V
Output Leakage Current	$I_{O(LKG)}$	V_{DD}	V_{DD} = 4.5V V_{OH} = 28V	—	—	10	μA

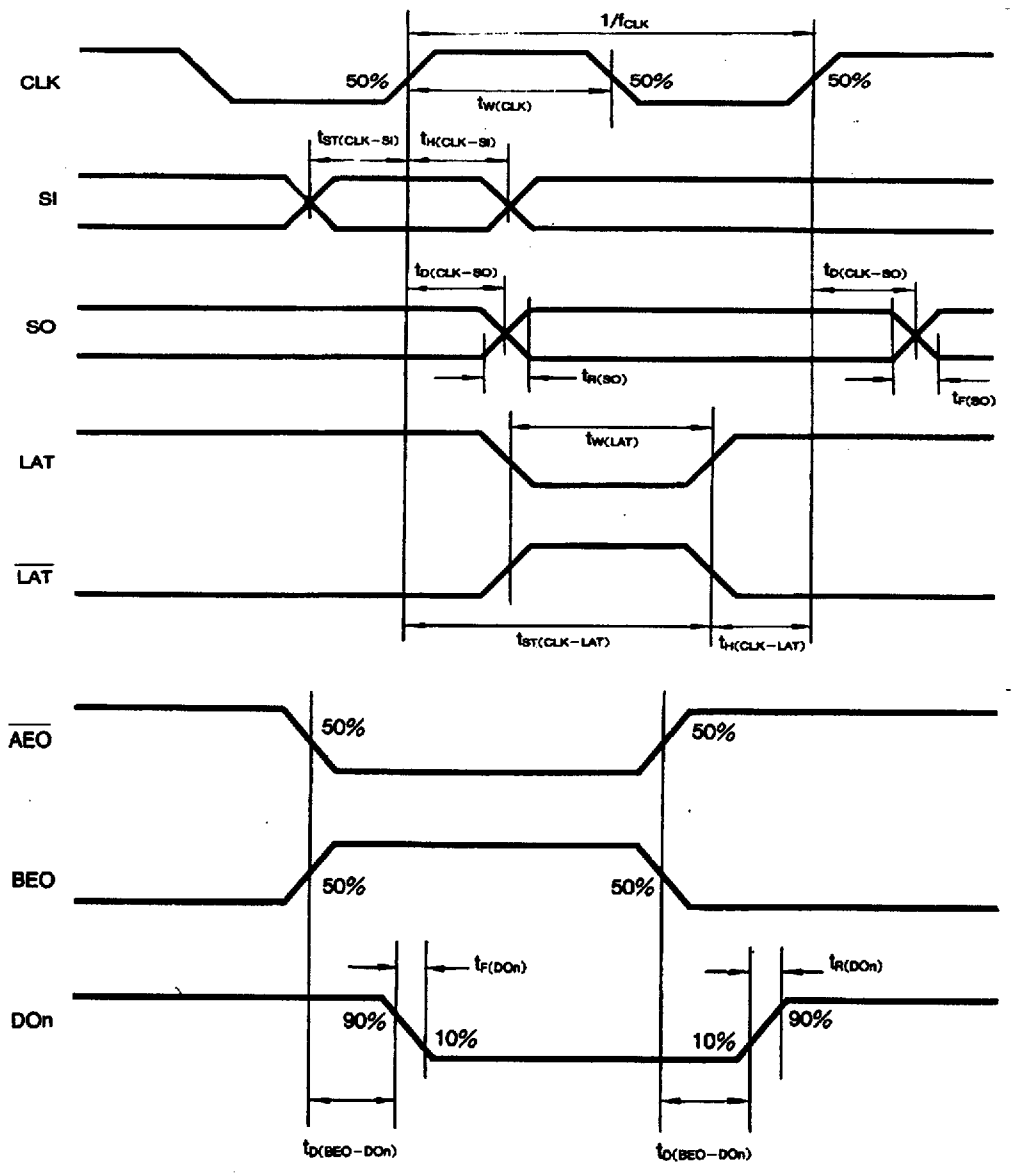
AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pad Name	Signal Conditions	Min	Typ	Max	Unit
Output Rising Time 1	$t_{R(SO)}$	SO	1. Input Signal	—	20	35	ns
Output Falling Time 1	$t_{F(SO)}$	SO	— Amplitude : 0-5V_{P-P}	—	20	35	ns
Output Rising Time 2	$t_{R(DOn)}$	DO_n	— Rising, Falling Time	—	0.8	3.0	μs
Output Falling Time 2	$t_{F(DOn)}$	DO_n	≤15ns	—	0.8	3.0	μs
Output Delay Time 1	$t_{D(CLK-SO)}$	CLK—SO	2. Output Signal	—	70	120	μs
Output Delay Time 2	$t_{D(BEO-DOn)}$	BEO—DOn	— Standard Load :1.6K ohm	—	1.0	3.0	μs

SIGNAL SEQUENCE

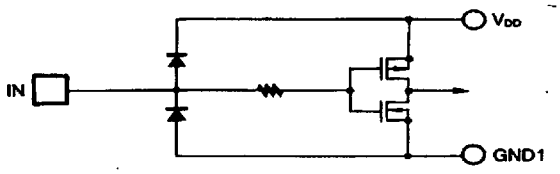


TIMING DIAGRAM

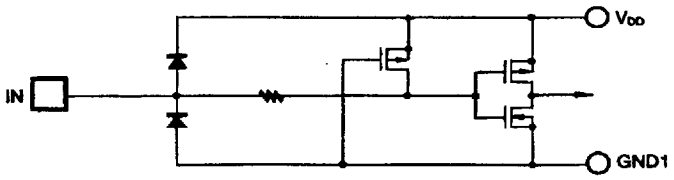


Input/Output stage Structure

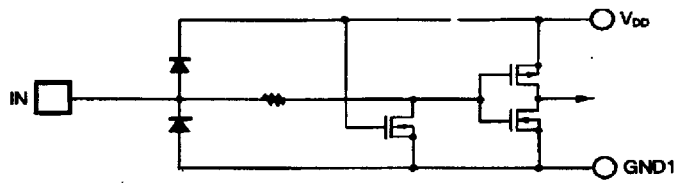
1. IN BUFFER 1 (CLK,SI,LAT)



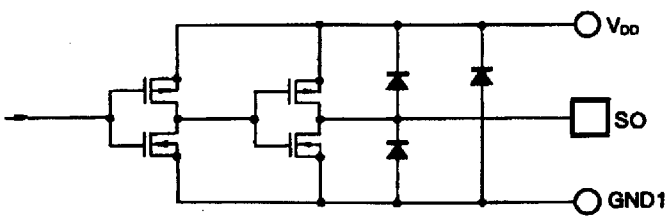
2. IN BUFFER 2($\overline{AEO}$,BEO)



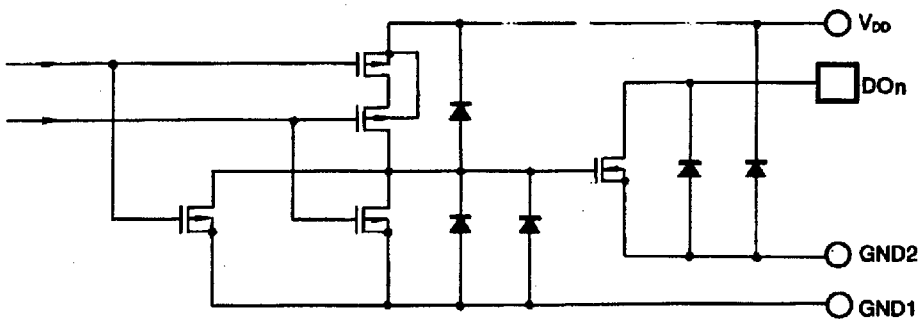
3. IN BUFFER 3(CTL)



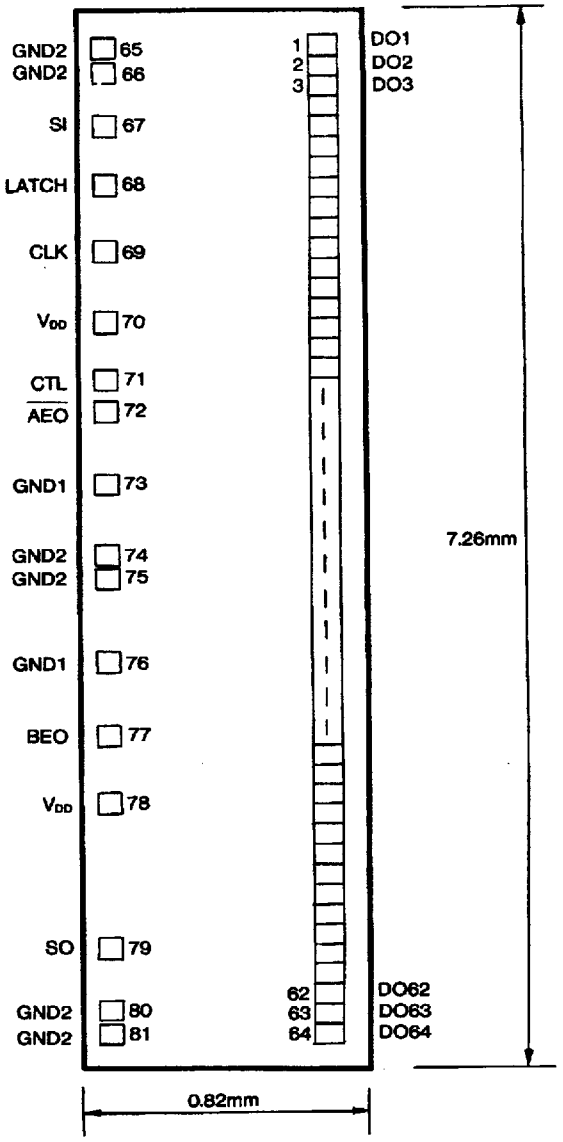
4. OUT BUFFER 1(SO)



5. OUT BUFFER2 (DOn)



PAD LAYOUT



CHIP SIZE
: 7.32 mm × 0.82mm
CHIP THICKNESS
: 0.35 ± 0.03mm
PAD SIZE
: 0.08 × 0.08mm
PAD PITCH
: 0.11mm

PAD CO—ORDINATED

NO.	NAME	X	Y	NO.	NAME	X	Y	NO.	NAME	X	Y
1	DO1	-3465	260	28	DO28	-495	260	55	DO55	2475	260
2	DO1	-3355	260	29	DO29	-385	260	56	DO56	2585	260
3	DO3	-3245	260	30	DO30	-275	260	57	DO57	2695	260
4	DO4	-3135	260	31	DO31	-165	260	58	DO58	2805	260
5	DO5	-3025	260	32	DO32	-55	260	59	DO59	2915	260
6	DO6	-2915	260	33	DO33	55	260	60	DO60	3025	260
7	DO7	-2805	260	34	DO34	165	260	61	DO61	3135	260
8	DO8	-2695	260	35	DO35	275	260	62	DO62	3245	260
9	DO9	-2585	260	36	DO36	385	260	63	DO63	3355	260
10	DO10	-2475	260	37	DO37	495	260	64	DO64	3465	260
11	DO11	-2365	260	38	DO38	605	260	65	GND2	-3465	-215
12	DO12	-2255	260	39	DO39	715	260	66	GND2	-3285	-215
13	DO13	-2145	260	40	DO40	825	260	67	SI	-3000	-215
14	DO14	-2035	260	41	DO41	935	260	68	LATCH	-2500	-215
15	DO15	-1925	260	42	DO42	1045	260	69	CLK	-2000	-215
16	DO16	-1815	260	43	DO43	1155	260	70	VDD	-1500	-215
17	DO17	-1705	260	44	DO44	1265	260	71	CTL	-1250	-215
18	DO18	-1595	260	45	DO45	1375	260	72	AEO	-1000	-215
19	DO19	-1485	260	46	DO46	1485	260	73	GND1	-500	-215
20	DO20	-1375	260	47	DO47	1595	260	74	GND2	0	-215
21	DO21	-1265	260	48	DO48	1705	260	75	GND2	180	-215
22	DO22	-1155	260	49	DO49	1815	260	76	GND1	520	-215
23	DO23	-1045	260	50	DO50	1925	260	77	BEO	1160	-215
24	DO24	-935	260	51	DO51	2035	260	78	VDD	1695	-215
25	DO25	-825	260	52	DO52	2145	260	79	SO	2955	-215
26	DO26	-715	260	53	DO53	2255	260	80	GND2	3286	-215
27	DO27	-605	260	54	DO54	2365	260	81	GND2	3466	-215

(0,0) : CHIP CENTER