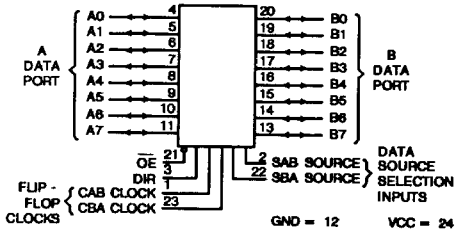
CD54/74FCT647, CD54/74FCT647AT
CD54/74FCT649, CD54/74FCT649AT

July 1990



FUNCTIONAL DIAGRAM

Octal Bus Transceivers/Registers, with Open Drain

CD54/74FCT647, CD54/74FCT647AT - Non-Inverting
CD54/74FCT649, CD54/74FCT649AT - Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 6.8ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT647, FCT649)*

The CD54/74FCT647, 647AT, 649 and 649AT open-drain, octal-bus tranceivers/registers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

Family Features:
- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX - Speed of bipolar FAST*/AS/S; FCTXXXAT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

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The CD54/74FCT647, 647AT, 649 and 649AT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0 to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT647 and 649 are also available in chip form (H suffix). These unpackaged device are operable over the -55°C to +125°C temperature range.

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT647, 647AT	CD54/74FCT649, 649AT
X	X	↓	X	X	X	Input	Not Specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not Specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs. To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10kΩ resistors.

File Number **2402**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

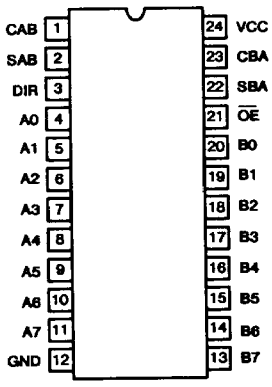
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

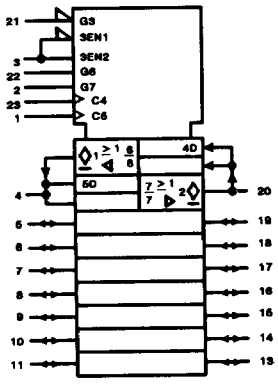
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		40	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT647, CD54/74FCT647AT TYPES

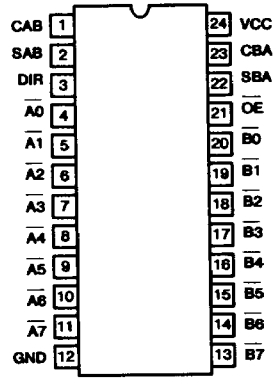


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT649, CD54/74FCT649AT TYPES



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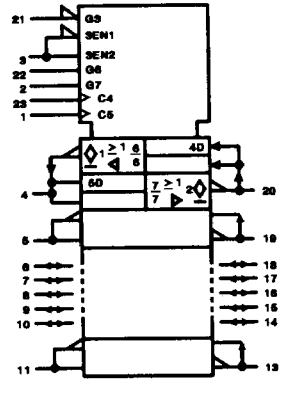


IEC LOGIC SYMBOL

4 TECHNICAL DATA

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, −55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		VCC (V)	AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		−55°C to +125°C		
		VI (V)	IO (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	–	2	–	2	–	V
Low-Level Input Voltage	VIL			4.5 to 5.5	–	0.8	–	0.8	–	0.8	V
High-Level Output Voltage	VOH	VIH or VIL	−15	MIN	2.4	–	2.4	–	–	–	V
			−12	MIN	2.4	–	–	–	2.4	–	V
Low-Level Output Voltage	VOL	VIH or VIL	64	MIN	–	0.55	–	0.55	–	–	V
			48	MIN	–	0.55	–	–	–	0.55	V
High-Level Input Current	IIH	VCC		MAX	–	0.1	–	1	–	1	µA
Low-Level Input Current	IIL	GND		MAX	–	−0.1	–	−1	–	−1	µA
3-State Leakage Current	IOZH	VCC		MAX	–	0.5	–	10	–	10	µA
	IOZL	GND		MAX	–	−0.5	–	−10	–	−10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	−60	–	−60	–	−60	–	mA
Input Clamp Voltage	VIK	VCC or GND	−18	MIN	–	−1.2	–	−1.2	–	−1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	–	8	–	80	–	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	–	1.6	–	1.6	–	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT647, 649 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT647AT, 649AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Data to Clock Setup Time	tSU	5†		4	-	4.5	-		CONTACT LOCAL SALES OFFICE FOR AVAILABILITY			-	ns
Data to Clock Hold Time	tH	5		2	-	2	-					-	ns
Clock Pulse Width	tW	5		6	-	6	-					-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

SWITCHING CHARACTERISTICS

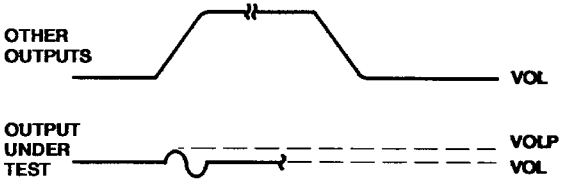
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT647, 649 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT647AT, 649AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Store An → Bn FCT647/AT; Store Bn → An	tPZL	5†	6.8	2	9	2	10		CONTACT LOCAL SALES OFFICE FOR AVAILABILITY				ns
	tPLZ	5	6.8	2	9	2	11						ns
Store $\overline{An}$ → Bn FCT649/AT; Store $\overline{Bn}$ → An	tPZL	5	6.8	2	9	2	10						ns
	tPLZ	5	6.8	2	9	2	11						ns
An → Bn FCT647/AT; Bn → An	tPZL	5	6.8	2	9	2	11						ns
	tPLZ	5	6.8	2	9	2	11						ns
$\overline{An}$ → Bn FCT649/AT; $\overline{Bn}$ → An	tPZL	5	6	2	8	2	9						ns
	tPLZ	5	6.8	2	9	2	11						ns
Select to Data FCT647/AT, FCT649/AT	tPZL	5	8.3	2	11	2							ns
	tPLZ	5	6.8	2	9	2	11						ns
Enabling Times, Bus to Output or Register to Output FCT647/AT	tPZL	5	10.5	2	14	2	15						ns
Enabling Times, Bus to Output or Register to Output FCT649/AT	tPZL	5	11.3	2	15	2	18						ns
Disabling Times, Bus to Output or Register to Output FCT647/AT, FCT649/AT	tPLZ	5	6.8	2	9	2							ns
Power Dissipation Capacitance	CPD§	-											pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical @ +25°C										V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical @ +25°C										V
Input Capacitance	CI	-	-	-	10	-	10	-	-	10	-	10	pF
Off-State Output Capac.	CO	-	-	-	15	-	15	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

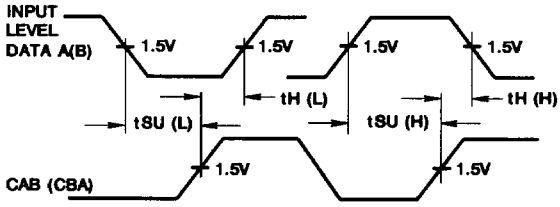


Figure 2 - Data setup and hold times.

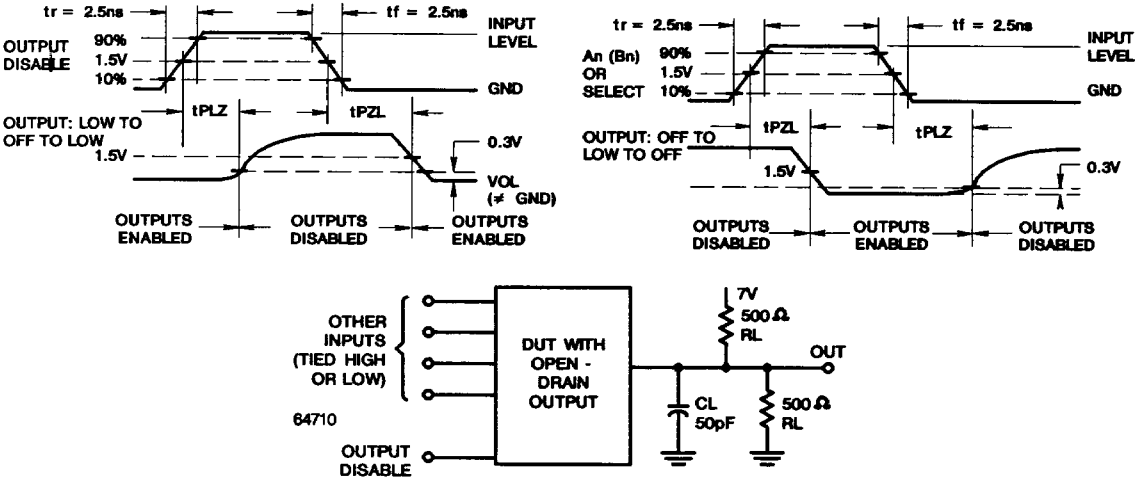


Figure 3 - Open-drain propagation delay times and test circuit.