ABRIDGED VERSION

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A TDK Group Company

SSI 32P4915A

PRML Read Channel with PR4, 8/9 ENDEC, 4-burst Servo

Target Specification

February 1996

DESCRIPTION

The SSI 32P4915A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 53 to 160 Mbit/s. Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and 4-burst servo. Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V power supply. The SSI 32P4915A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- Register programmable data rates from 53 to 160 Mbit/s
- Sampled data read channel with Viterbi qualification
- Programmable filter for PR4 equalization
- Five tap transversal filter with adaptive PR4 equalization
- 8/9 GCR ENDEC
- Data Scrambler/Descrambler
- Presettable precoder state
- Programmable write precompensation
- Low operating power (1.15W typical at 5V)
- Register programmable power management (<5 mW power down mode)
- 4-bit nibble and byte wide bi-directional NRZ data interfaces
- 8-bit direct write mode automatically configured for RCLK = VCO/8
- Serial interface port for access to internal program storage registers
- Single power supply (5V ± 10%)
- Small footprint 80-lead PTQFP, 100-lead TQFP and 100-lead QFP packages
- Power Management under register bit control

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The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

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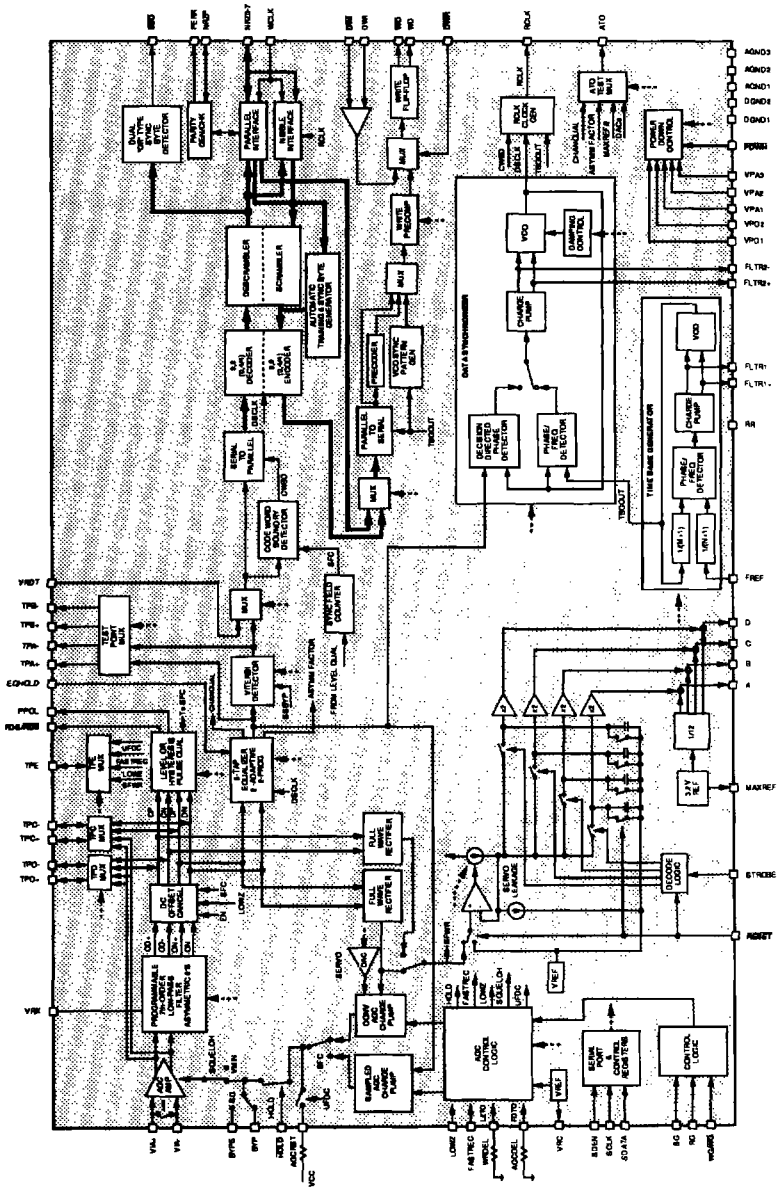
BLOCK DIAGRAM



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FEATURES (continued)

AUTOMATIC GAIN CONTROL

- Dual mode AGC, analog during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery (analog)
- Programmable, symmetric, charge pump currents for data reads (sampled)
- Charge pump currents track programmable data rate during data reads (sampled)
- Low drift AGC hold circuitry
- Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery
- AGC Amplifier squelch during Low-Z
- Wide bandwidth, precision full-wave rectifier
- Programmable AGC controls
  - Separate external input pins for AGC hold, fast recovery, and Low-Z control

  or

  - Internal Low-Z and fast decay timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor. AGC input impedance vs LOWZ = 5:1.
- 2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4V

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 6 to 50 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable "zeros" equalization provides time asymmetry compensation
  - ±0.5 ns group delay variation from 0.3 fc to fc, with fc = 50 MHz
  - Minimizes size and power
  - Low-Z switch at filter output for fast offset recovery
  - No external coupling capacitors required
  - DC offset compensation provided at filter output
  - Five tap transversal filter for fine equalization to PR4
  - Self adapting inner taps (symmetric)
  - Programmable outer taps (symmetric, 4 bits)
  - Equalization hold input
  - "Zeros" channel quality output
  - Amplitude asymmetry factor output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register programmable window or hysteresis pulse qualifier for servo reads
- Selectable RDS pulse width and polarity for servo gray code reads

TIME BASE GENERATOR

- Less than 1% frequency resolution
- Up to 180 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

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FEATURES (continued)

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 160 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 4-bit nibble and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection, single byte or dual ("or" type)
- Semi-auto training and sync byte generation available for single sync byte operation
- Surface defect scan mode

SERVO

- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- "Soft Landing" charge pump architecture
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Programmable charge pump current
- Wide bandwidth, precision full-wave rectifier
- Programmable selection of normal or differentiated filter output to servo capture block
- Programmable AGC gain in servo mode (2 bits)
- Full wave rectifier observation point

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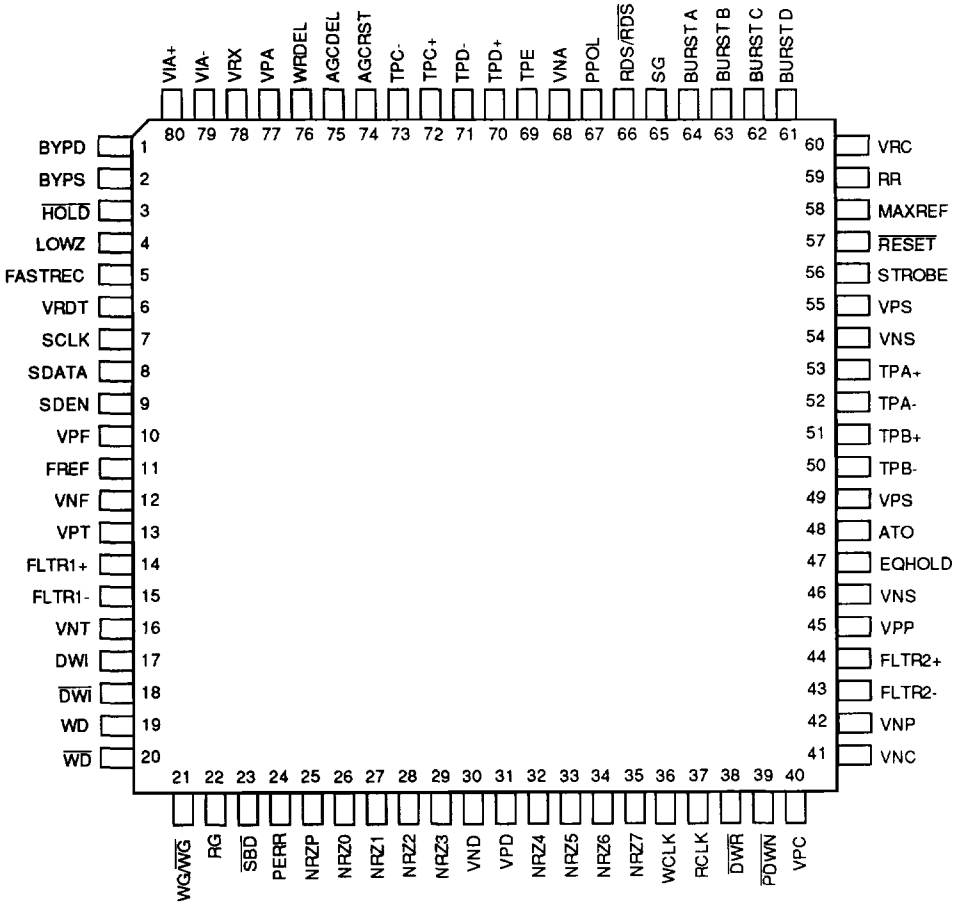
PACKAGE PIN DESIGNATIONS

(Top View)



80-Lead PTQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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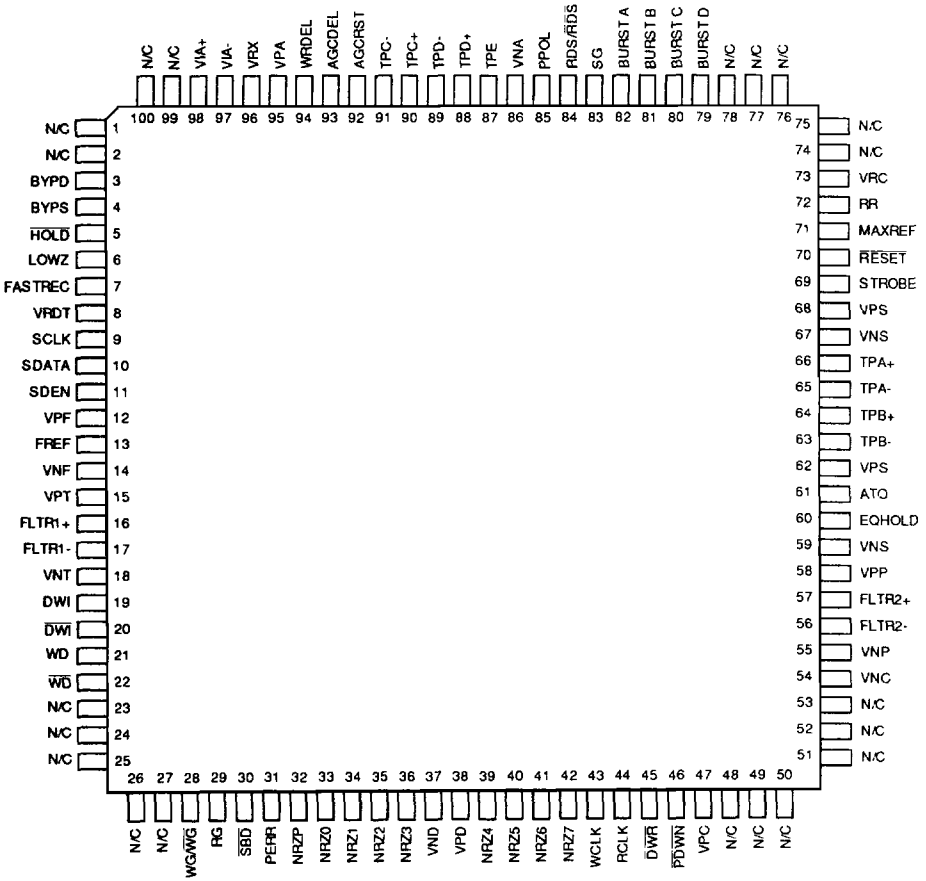

100-Lead TQFP, PTQFP

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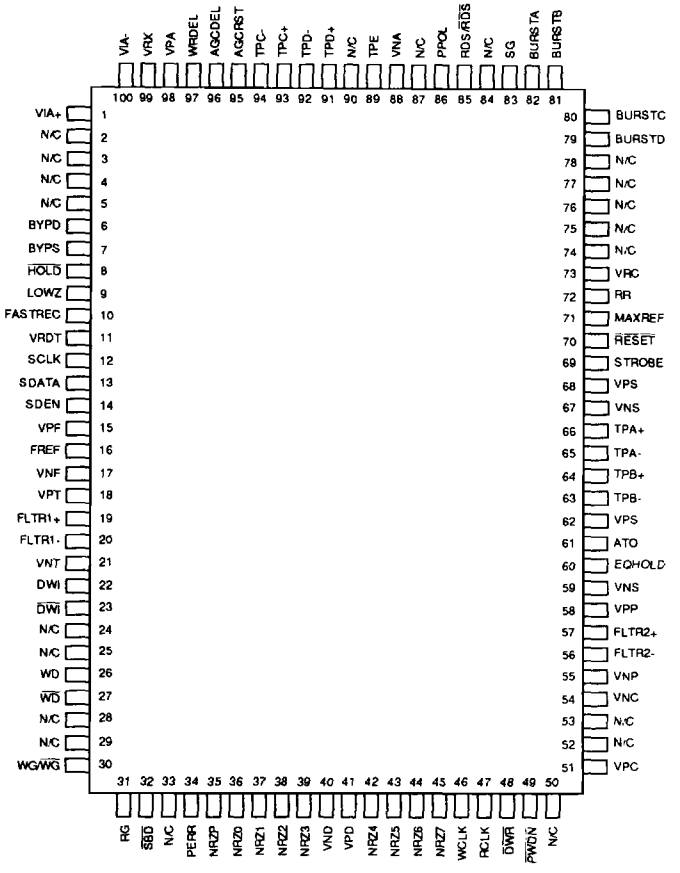

100-Lead QFP

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