

Planar Tunnel (Back) Diode Chips

Series A1S

Features

- Rugged Planar Design
- Low Temperature Variation
- Zero Bias Operation
- Excellent RF Match
- Low 1/f Noise

Applications

DC Coupled Detectors
 Detector Log Video Amplifiers
 Doppler Mixers

Environmental Ratings (Maximum)

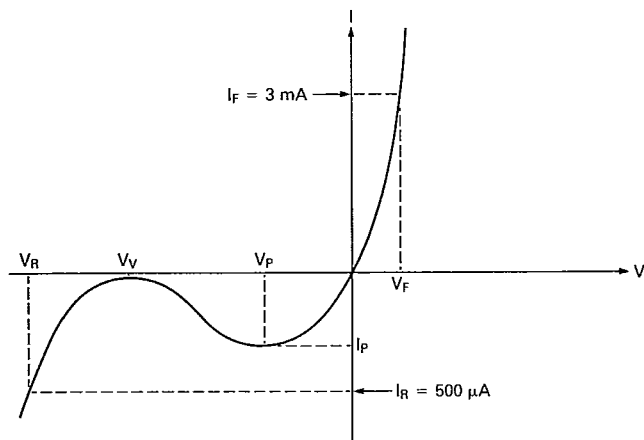
Storage Temperature - 55°C to + 125°C
 Operating Temperature - 55°C to + 115°C

Electrical Specifications @ 25°C

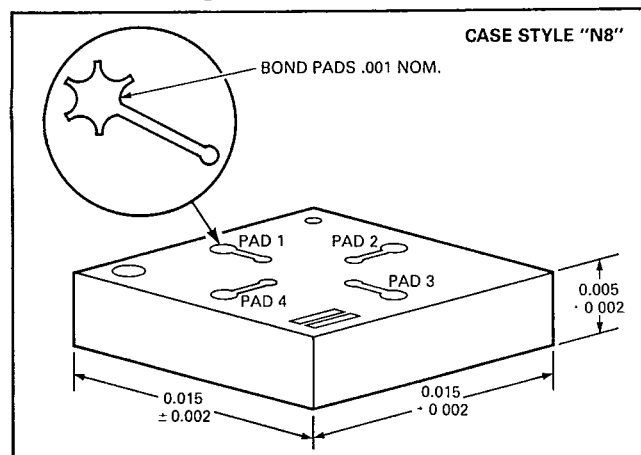
Part Number	I_p (μ A) Range	I_p/I_V (Min.)	V_R (mV) @ 500 μ A (Min.)	V_F (mV) @ 3 mA (Max.)	C_j^* (pF) (Max.)	R_S (Ohms) (Max.)
A1S020	100-200	3	450	130	.20	10
A1S021	100-200	3	450	125	.25	10
A1S022	100-200	3	450	120	.30	10
A1S030	200-300	3	440	125	.20	10
A1S031	200-300	3	440	120	.25	10
A1S032	200-300	3	440	115	.30	10
A1S040	300-450	3	430	120	.20	10
A1S041	300-450	3	430	115	.25	10
A1S042	300-450	3	430	110	.30	10
A1S050	450-600	4	420	115	.20	10
A1S051	450-600	4	420	110	.25	10
A1S052	450-600	4	420	105	.30	10
A1S060	600-750	4	410	115	.20	10
A1S061	600-750	4	410	110	.25	10
A1S062	600-750	4	410	105	.30	10

*@ V_V
 Note: Specifications subject to change without notice.

V & I Characteristics



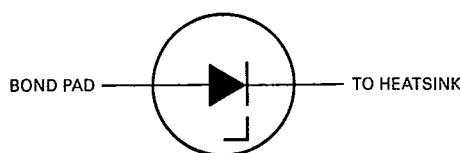
Outline Drawing



Handling Procedures

- Die Attach Silver Epoxy with cure temperature of 125°C maximum
- Wire Bonding 0.7 mil gold wire thermocompression bond
 Tip temperature = 180°C maximum
 Stage temperature = 160°C maximum

Bond Pad to Heatsink diagram

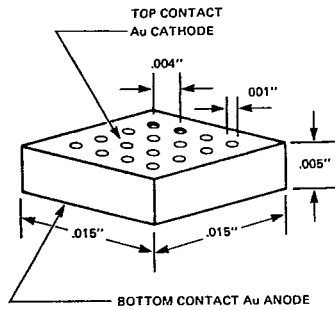


CAUTION: Static Sensitive Device

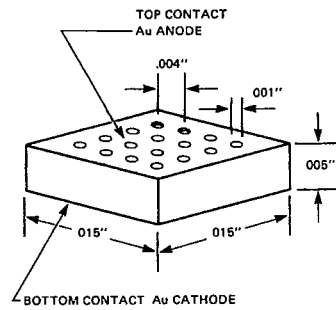
T-91-20

Diode Outline Dimensions

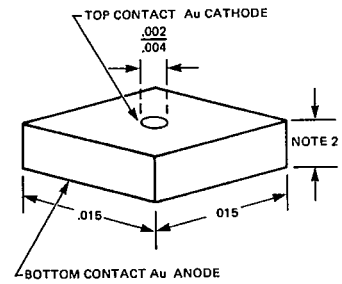
CASE STYLE "N1" *



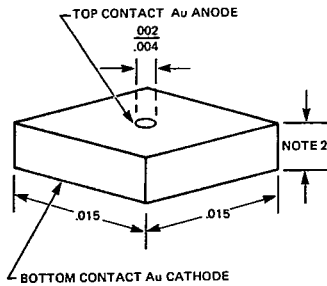
CASE STYLE "N2" *



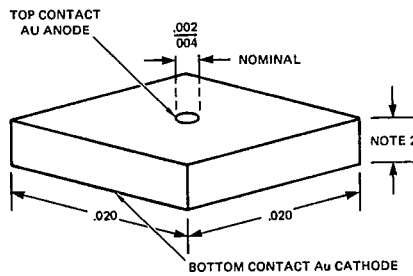
CASE STYLE "N3"



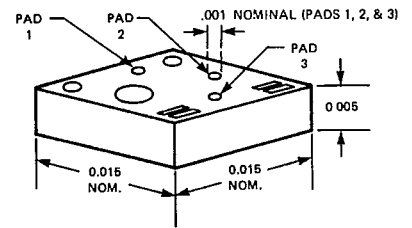
CASE STYLE "N4"



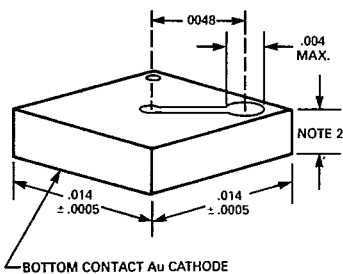
CASE STYLE "N5"



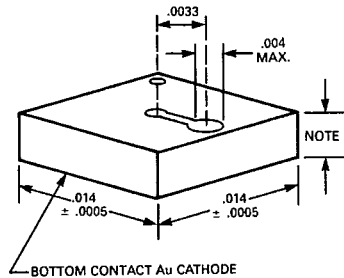
CASE STYLE "N6" *4



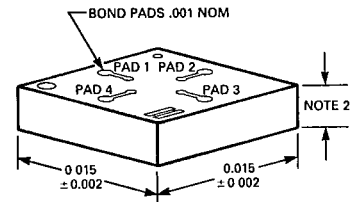
CASE STYLE "70N7"



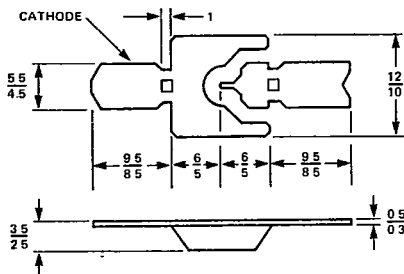
CASE STYLE "18N7"



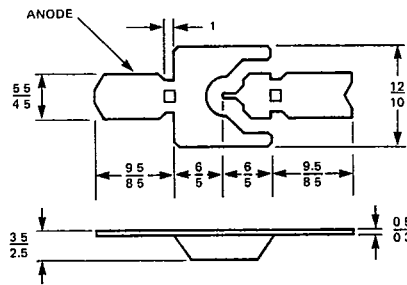
CASE STYLE "N8"



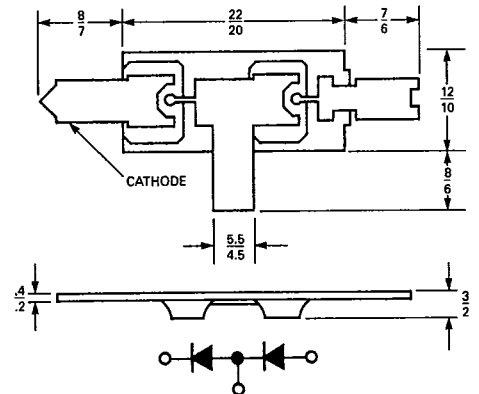
CASE STYLE "B1"6



CASE STYLE "B2"6



CASE STYLE "B3"6

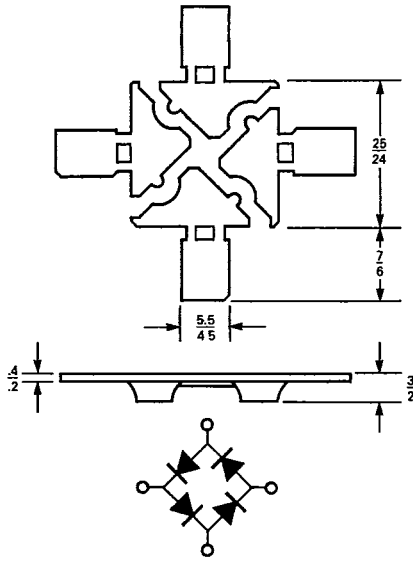


*Some die may have test pattern contacts in addition to the active junction. Always bond to the junction closest to the geometric center of the chip or the specified junction.

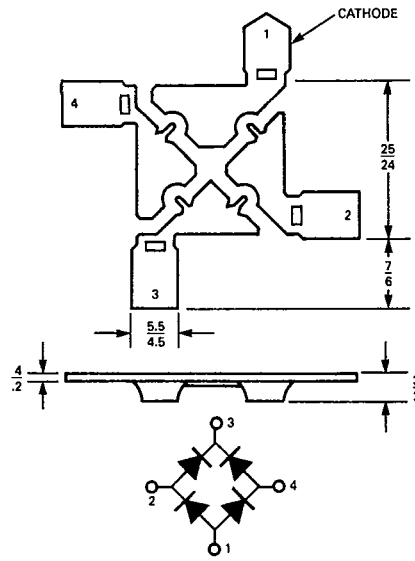
Notes:

1. All dimensions are nominal.
2. Chip thicknesses vary from .003" to .008" dependent upon specific product.
3. Chips N1 & N2 may have from 9 to 16 contacts. Always bond to the junction closest to the geometric center of the chip.
4. Contact to be used on chip N6 will be specified with each shipment.
5. Packages are not necessarily drawn to the same scale.
6. All "Bx" package dimensions are in thousandths of an inch.

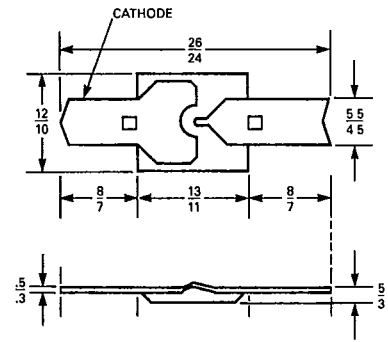
CASE STYLE "B4"6



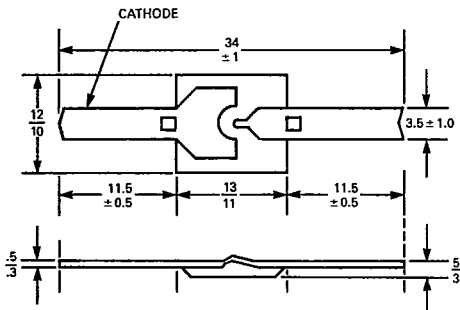
CASE STYLE "B5"6



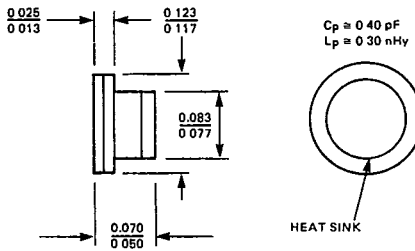
CASE STYLE "B7S"6



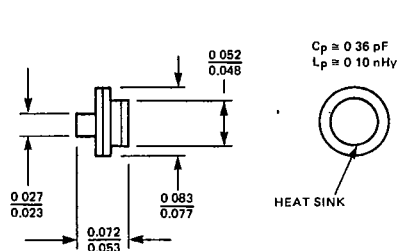
CASE STYLE "B7L"6



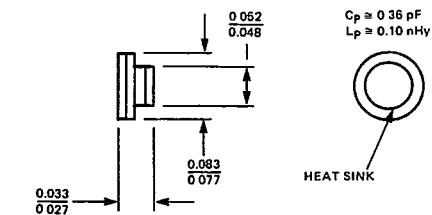
CASE STYLE "A"



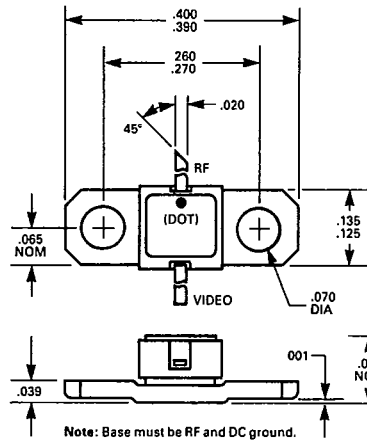
CASE STYLE "C"



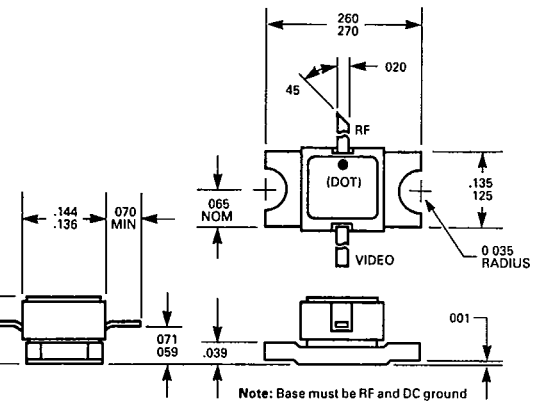
CASE STYLE "D"



CASE STYLE "F"



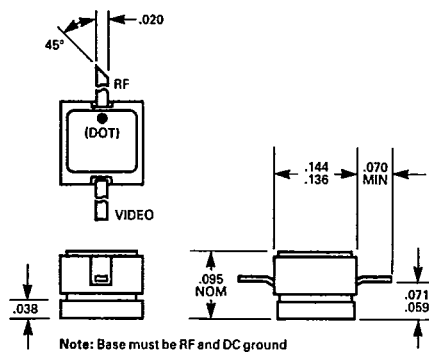
CASE STYLE "F1"



Note: Base must be RF and DC ground.

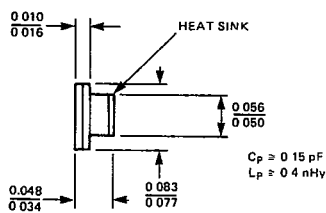
Note: Base must be RF and DC ground.

CASE STYLE "F2"

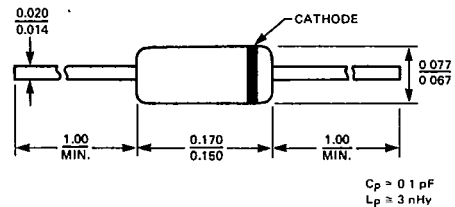


Note: Base must be RF and DC ground.

CASE STYLE "G"



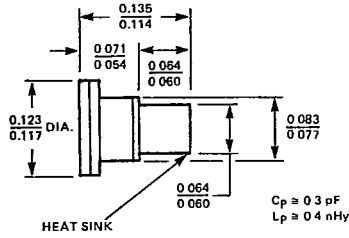
CASE STYLE "H"
(Glass axial lead—similar to D034)



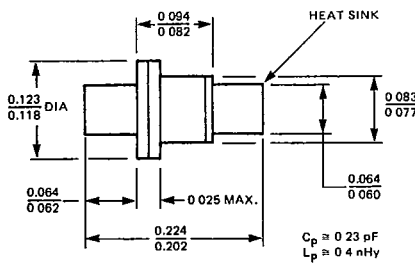
Cp ≈ 0.1 pF
Lp ≈ 3 nHy

Diode Outline Dimensions

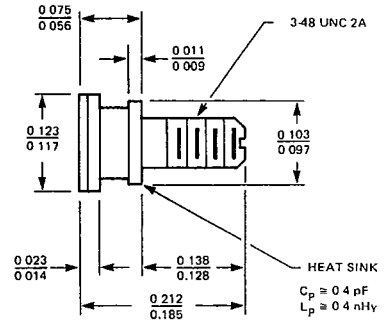
CASE STYLE "I"



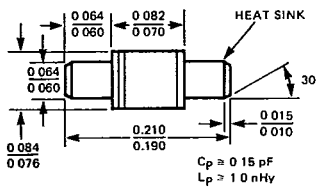
CASE STYLE "J"



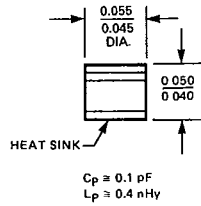
CASE STYLE "K"



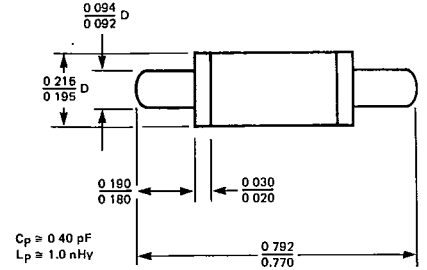
CASE STYLE "L"



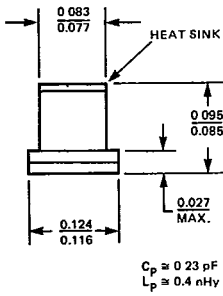
CASE STYLE "P"



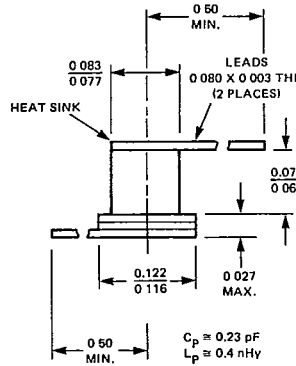
CASE STYLE "S2"



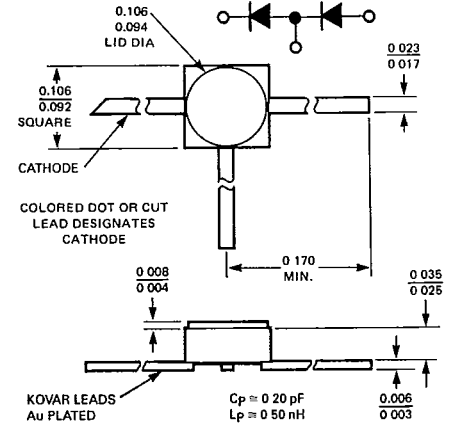
CASE STYLE "S3"



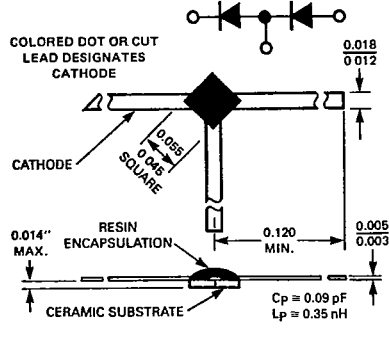
CASE STYLE "S4"



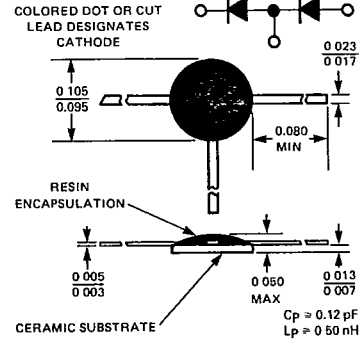
CASE STYLE "T2"



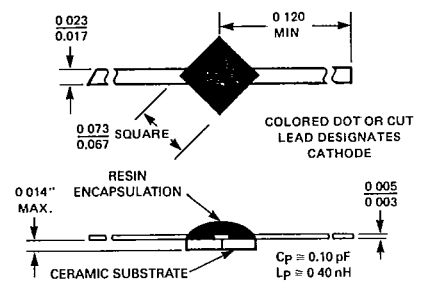
CASE STYLE "T3"



CASE STYLE "T4"

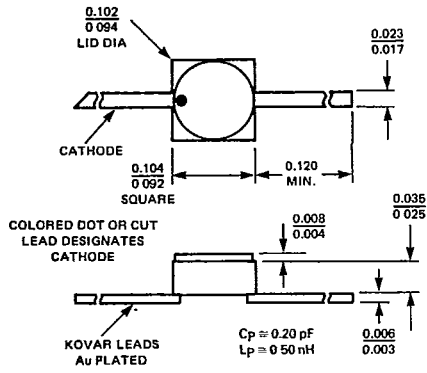


CASE STYLE "U1"

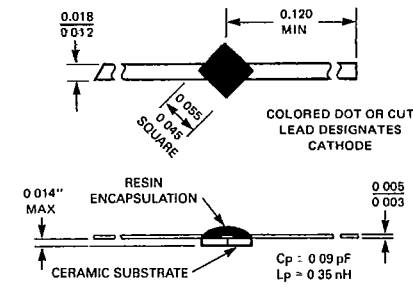


Note: Packages are not necessarily drawn to the same scale.

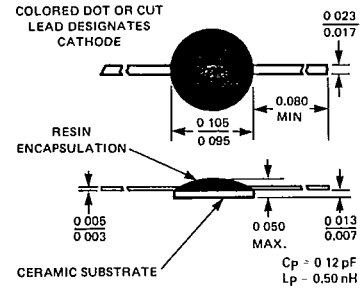
CASE STYLE "U2"



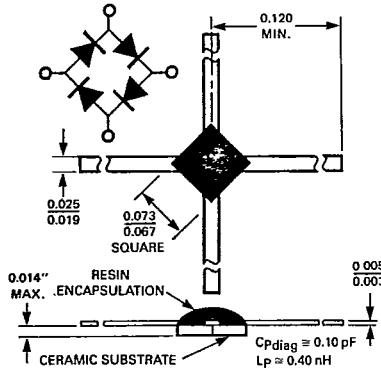
CASE STYLE "U3"



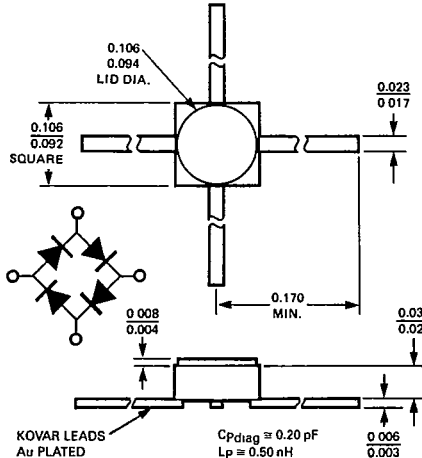
CASE STYLE "U4"



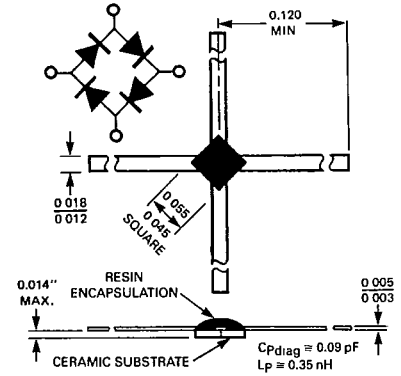
CASE STYLE "W1"



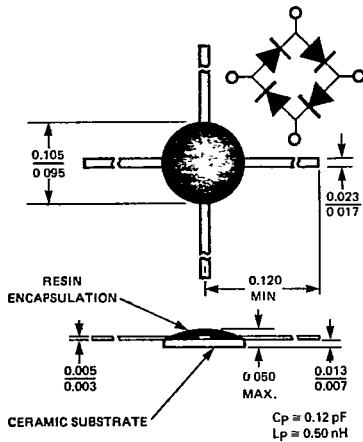
CASE STYLE "W2"



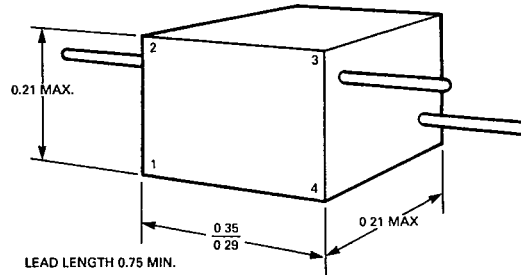
CASE STYLE "W3"



CASE STYLE "W4"



CASE STYLE "Z"



CONNECTION DIAGRAMS FOR "Z"

