



# 77 GHz MPA for Car Radar Systems

Preliminary Data Sheet

# T626\_MPA2\_W

- Operating Frequency: 76 - 77 GHz
- Output Power: + 13 dBm
- Input and Output matched to 50  $\Omega$
- Application in Car Radar Systems

**ESD:** Electrostatic discharge sensitive device, observe handling precautions!

Type	Marking	Ordering Code	Package
T626_MPA2_W	–	Q62702-G173	Chip

The T626\_MPA2\_W is a millimeter wave, medium power amplifier, suitable for signal amplification in modern, MMIC-based car radar systems. It might be used as small signal amplifier or as output stage.

The MMIC will be delivered with wirebond compatible pads. To ease substrate design, the MMIC's layout can be provided in dxf- or gds2-format.

## Circuit Description

The T626\_MPA2\_W incorporates a two-stage, PHEMT - based millimeter wave amplifier. Both input and output are matched to 50  $\Omega$ .

The T626\_MPA2\_W is optimized for mounting on a metal plate, different performance might be expected using flip-chip mounting.

The MPA delivers at least 13 dBm of RF output power with 3 dB compression. The small-signal gain is 8 dB.

Over a temperature range of  $T_{amb} = -40$  to  $+95$  °C, the output power variation is less than 3 dB without DC bias compensation.

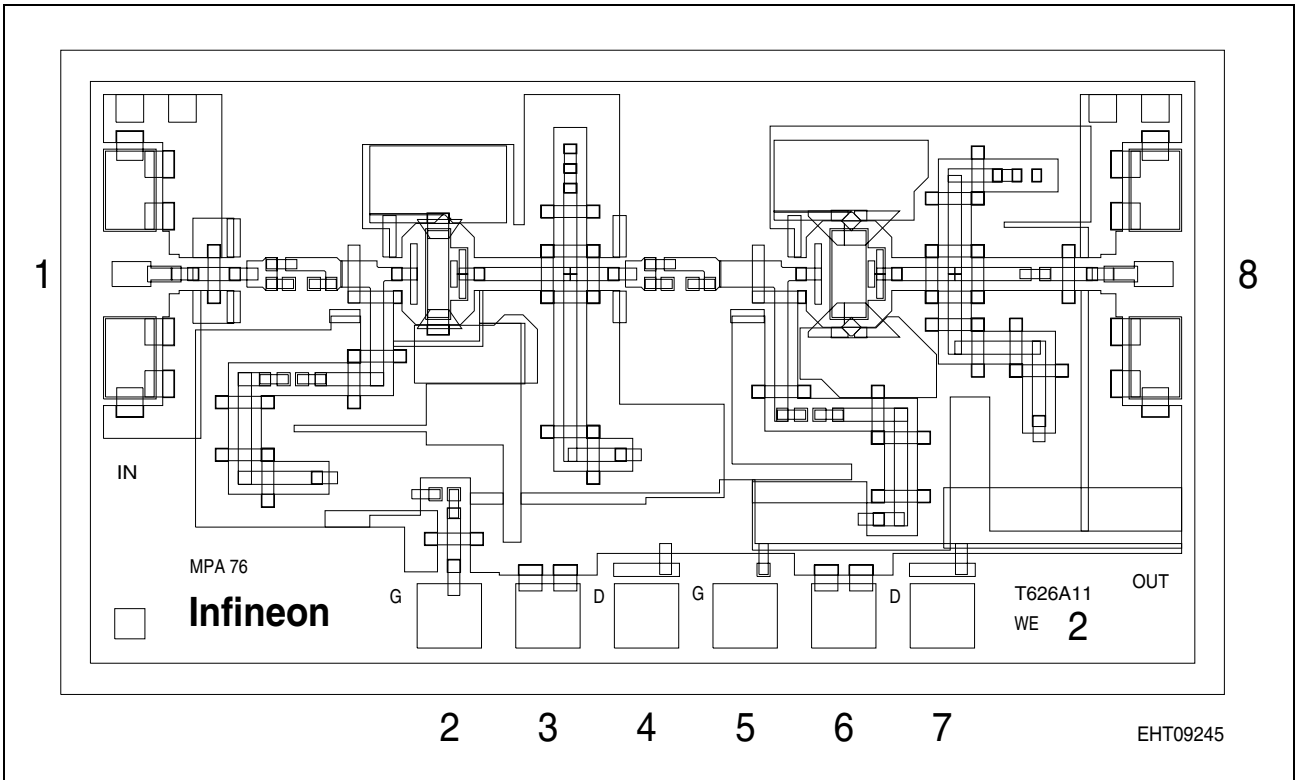


Figure 1 Pin Configuration

Pin Configuration

Pad	Symbol	Function
1	RF IN	Coplanar RF Input, Matched to 50 Ω Typically 46 μm RF Signal Pad Width, 37 μm Gap to GND Pads RF Probing: Use 100 to 120 μm Ground – Signal – Ground Pitch
2	$V_{G1}$	Gate Voltage 1 <sup>st</sup> PHEMT Amplifier Stage
3	GND	Chip DC Ground
4	$V_{D1}$	Drain Voltage 1 <sup>st</sup> PHEMT Amplifier Stage
5	$V_{G2}$	Gate Voltage 2 <sup>nd</sup> PHEMT Amplifier Stage
6	GND	Chip DC Ground
7	$V_{D2}$	Drain Voltage 2 <sup>nd</sup> PHEMT Amplifier Stage
8	RF OUT	Coplanar RF Output, Matched to 50 Ω Typically 46 μm RF Signal Pad Width, 37 μm Gap to GND Pads RF Probing: Use 100 to 120 μm Ground – Signal – Ground Pitch

The bias pads (2 - 7) have 150 μm pitch.

**Characteristic - General and DC**

Parameter	Symbol	Typ. Value	Unit
Ambient Temperature <sup>1)</sup>	$T_{amb}$	- 40 to + 105	°C
Drain Supply Voltage, 1 <sup>st</sup> Stage	$V_{D1}$	3.4	V
Gate Supply Voltage, 1 <sup>st</sup> Stage	$V_{G1}$	0.2	V
Drain Supply Current, 1 <sup>st</sup> Stage	$I_{D1}$	40	mA
Drain Supply Voltage, 2 <sup>nd</sup> Stage	$V_{D2}$	3.6	V
Gate Supply Voltage, 2 <sup>nd</sup> Stage	$V_{G2}$	0.2	V
Drain Supply Current, 2 <sup>nd</sup> Stage	$I_{D2}$	60	mA

<sup>1)</sup> Chip's backside mounted on a metal heatsink.

**Characteristic - RF**

Parameter <sup>1)</sup>	Symbol	Typ. Value	Unit
Operation frequency	$f_0$	76 to 77	GHz
RF Output Power, 1 dB compression	$P_{OUT-1dB}$	11	dBm
RF Output Power, 3 dB compression	$P_{OUT-3dB}$	13	dBm
RF Output Power, saturation	$P_{SAT}$	13.5	dBm
Small Signal Gain ( $P_{IN} = - 10$ dBm)	$G_S$	8	dB
Large Signal Gain ( $P_{IN} = + 6$ dBm)	$G_S$	6.5	dB
Isolation with both stages $V_D = 0$	$A_i$	> 30	dB

<sup>1)</sup> The given parameters assume 50  $\Omega$  RF load impedance and an ambient temperature of  $T_{amb} = 25$  °C. The chip's backside is mounted on a metal plate. Chip thickness is 100  $\mu$ m. The T626\_MPA2\_W is intended for wire bonding only. Flip chip mounting with stud bumps might lead to different performance.

**Geometry**

Parameter	Symbol	Typ. Value	Unit
Chip Thickness	$d_{\text{Chip}}$	100	$\mu\text{m}$
Chip Outline	$A_{\text{Chip}}$	$1.68 \times 0.89$	$\text{mm}^2$
Bond Pad Size DC	$A_{\text{BondpadDC}}$	$100 \times 100$	$\mu\text{m}^2$
Bond Pad Pitch DC	<i>DC Pitch</i>	150	$\mu\text{m}$
Bond Pad Size RF	$A_{\text{BondpadRF}}$	$50 \times 50$	$\mu\text{m}^2$
Bond Pad Pitch RF <sup>1)</sup>	<i>CPW Pitch</i>	120	$\mu\text{m}$

<sup>1)</sup> RF Probing: Use G-S-G Probes with 100 to 120  $\mu\text{m}$  Pitch.

**Recommended Bonding Conditions**

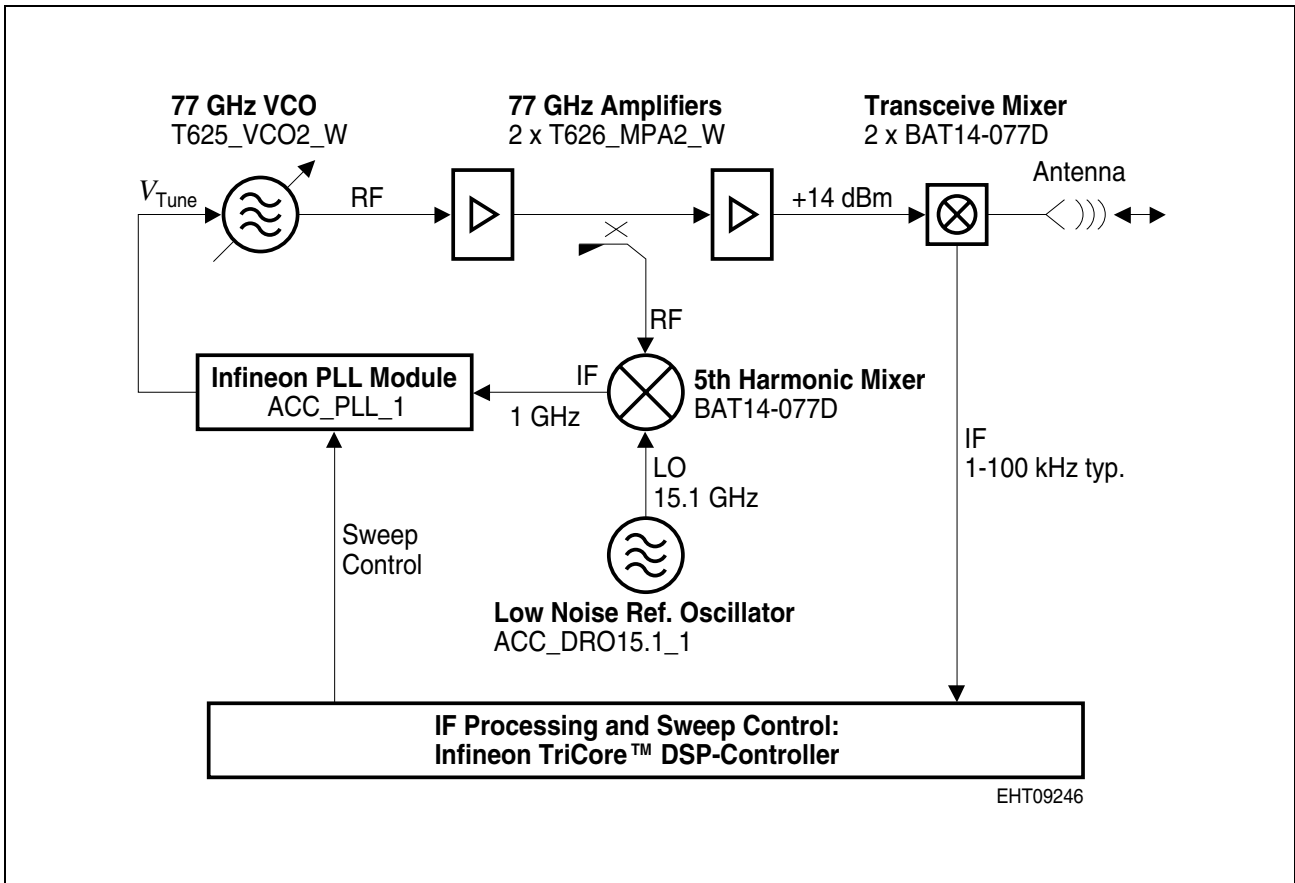
Parameter	Thermal Compression <sup>1)</sup>	Wedge Bonding	Unit
Chuck Temp.	250	250	$^{\circ}\text{C}$
Tool Temp.	180	150	$^{\circ}\text{C}$
Scrub	100	–	Hz
Bond Force	50	25	g
Wire Diameter	25	17	$\mu\text{m}$
Bond Pull Test (1)	2.5 <sup>2)</sup>		g
Bond Pull Test (2)	3.1 <sup>2)</sup>		g
Bond Pull Test (3)	3.2 <sup>2)</sup>		g
Bond Pull Test (4)	3.0 <sup>2)</sup>		g
Bond Pull Test (5)	2.8 <sup>2)</sup>		g

<sup>1)</sup> Nailhead, no ultrasonic

<sup>2)</sup> See Mil 883, > 2 g

**Application Note: Infineon Semiconductors in Modern ACC Radar Systems**

Infineon provides a variety of car radar products to simplify the design of modern, MMIC-based car radar systems:



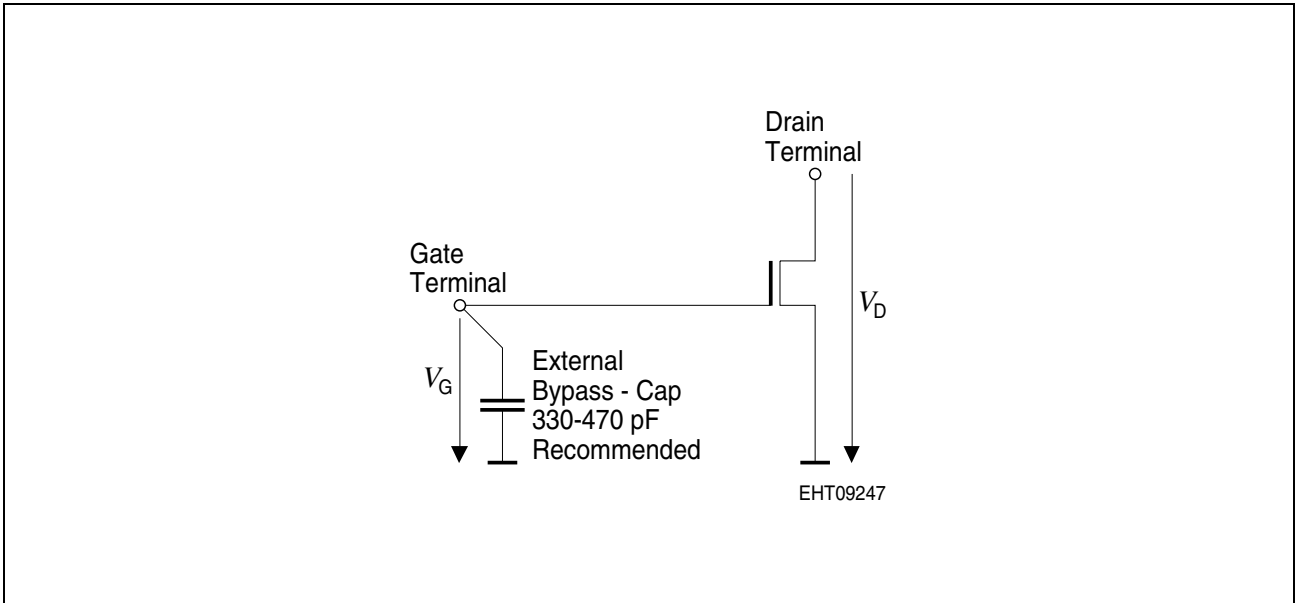
**Figure 2 Principle of a Modern one-beam, MMIC-based FMCW Radar System**

T625_VCO2_W	PHEMT-based 76 - 77 GHz, two-stage voltage controlled oscillator (VCO) GaAs MMIC with + 5 dBm output power.
T626_MPA2_W	PHEMT-based 76 - 77 GHz, two-stage medium power amplifier (MPA) with max. + 13.5 dBm RF output power and 10 dB small-signal gain at 76.5 GHz.
BAT14-077D	Silicon-based dual Schottky diode for millimeter wave receive mixer applications, 12 dB conversion loss, low $1/f$ corner frequency, very low noise.
ACC_DRO15.1_1 <sup>1)</sup>	Ultra-low phase noise ( $-108$ dB/Hz @ 100 kHz) dielectric resonator oscillator (DRO) module as stable frequency reference with excellent short-term and long-term stability. Pre-tuned to 15.1 GHz.
ACC_PLL_1 <sup>1)</sup>	Phase locked loop (PLL) module for the generation of ultra-linear frequency sweeps in FMCW radar systems. Typical deviation from a 200 MHz RF sweep at 76.5 GHz is less than 20 kHz. Maximum sweep bandwidth: 450 MHz, modulation rate 500 GHz/s. User control by simple digital interface or by an external data generator.
TriCore <sup>1)</sup>	TriCore™ microcontroller with two fast, synchronous A/D converters. Especially suited for signal processing and sweep control.

<sup>1)</sup> Contact Infineon for more information and design support.

**Application Note: Biasing of Infineon PHEMT-Based Car Radar MMICs**

Infineon car radar MMICs provide on-chip blocking capacitors, capable to reduce bias oscillations down to 1 GHz. For save operation below 1 GHz, a bypass capacitor of 470 to 330 pF should be connected from each MMIC gate terminal to an on-chip ground pad. The capacitor should have low ESR up to 1.5 GHz. Keep leads as short as possible.



**Figure 3**

DC-Blocking of drain terminals is normally not necessary and might lead to bias oscillations induced by feedback via common ground lead inductance. Combination of drain and gate terminals should be done by series resistors of 5 to 10 Ω.

To compensate for temperature effects, an active bias controller with positive temperature coefficient (e.g. Infineon BCR 400W) can be used.