CMOS Digital Integrated Circuits   Silicon Monolithic

TC7MP3125FK

1. Functional Description

- Low-Voltage, Low-Power 2-Bit × 2 Dual-Supply Bus Transceiver

2. General

The TC7MP3215FK is an advanced high-speed CMOS 4-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.
All inputs and outputs have tolerant function, and can be applied up to 3.6 V at power down mode.
The input consists of two same 2-bit configuration and it can be used as dual 2-bit configurations or single 4-bit configuration.
When the DIR input that changes transmission direction is H level, A-bus works as input and B-bus works as output, and when the DIR is L level, A-bus works as output and B-bus works as input.
When the Enable input $\overline{OE}$ is H level, both A-bus and B-bus become to floating state (high-impedance).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

(1) Operating voltage: 1.2 V to 1.8 V / 1.2 V to 2.5 V / 1.2 V to 3.3 V / 1.5 V to 2.5 V
1.5 V to 3.3 V / 1.8 V to 2.5 V / 1.8 V to 3.3 V / 2.5 V to 3.3 V
bidirectional interface

(2) High-speed operation: t_{pd} = 6.8 ns (max) (V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 8.9 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 10.3 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 61 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 9.5 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 10.8 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 60 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 58 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V)

(3) Output current: $|I_{OH}|/I_{OL}$ = 12 mA (min) (V_{CC} = 3.0 V)
$|I_{OH}|/I_{OL}$ = 9 mA (min) (V_{CC} = 2.3 V)
$|I_{OH}|/I_{OL}$ = 3 mA (min) (V_{CC} = 1.65 V)
$|I_{OH}|/I_{OL}$ = 1 mA (min) (V_{CC} = 1.4 V)

(4) Ultra-small package: VSSOP (US16)

(5) Low power dissipation: By using the new circuit, the power consumption is reduced significantly when $\overline{OE}$ = "H".
Suitable for battery-driven applications such as PDAs and cellular phones.

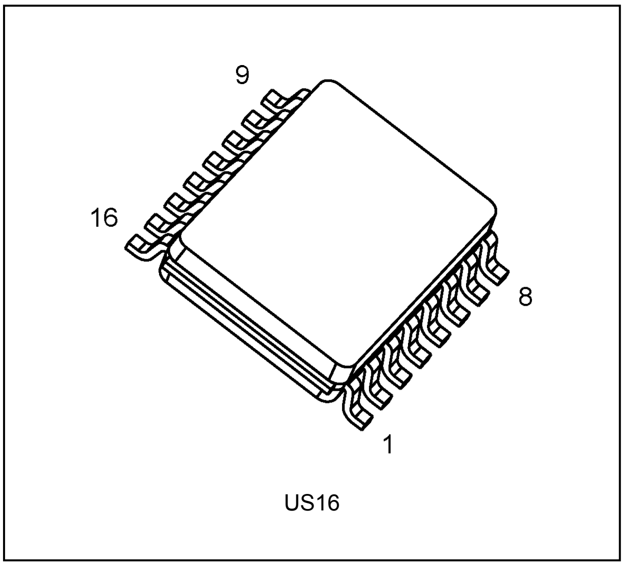
(6) Floating of A-bus and B-bus is permitted (when $\overline{OE}$ = "H").

(7) 3.6 V tolerance and power-down protection are provided to all inputs and outputs.

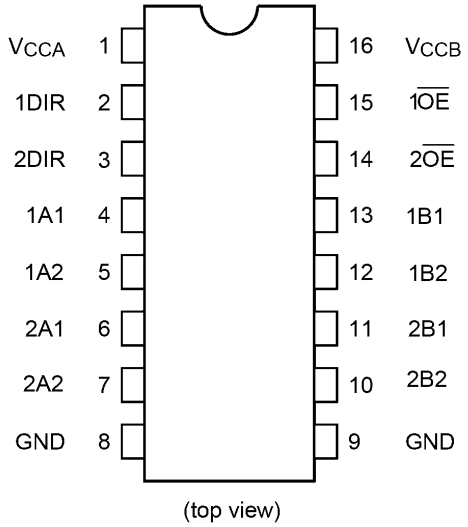
Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

Start of commercial production
2019-03

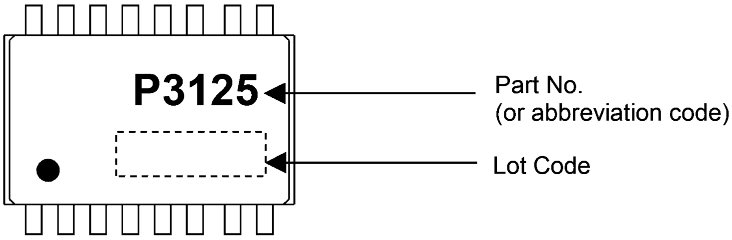
4. Packaging



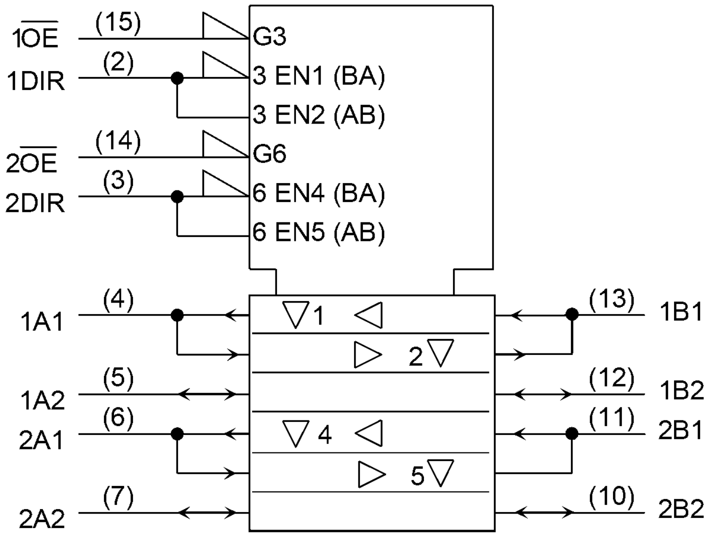
5. Pin Assignment



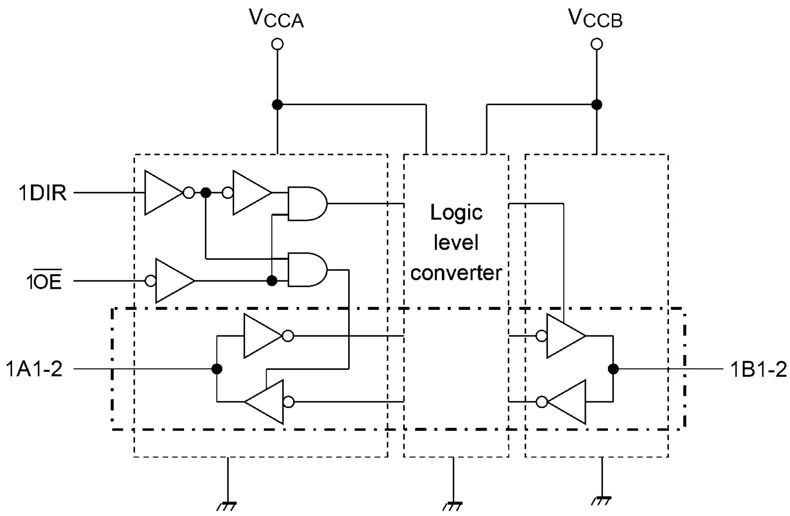
6. Marking

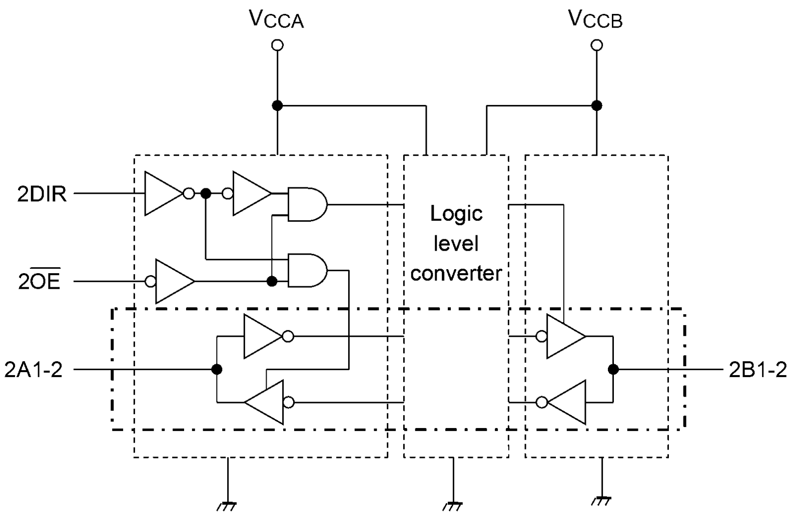


7. IEC Logic Symbol



8. Block Diagram





9. Truth Table

Input $1\overline{OE}$	Input 1DIR	Function Bus 1A1-1A2	Function Bus 1B1-1B2	Outputs
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

Input $2\overline{OE}$	Input 2DIR	Function Bus 2A1-2A2	Function Bus 2B1-2B2	Outputs
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

X: Don't care
Z: High impedance

10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	-0.5 to 4.6	V
	V_{CCB}		-0.5 to 4.6	
Input voltage (DIR, $\overline{OE}$)	V_{IN}		-0.5 to 4.6	V
Bus I/O voltage	$V_{I/OA}$	(Note 2)	-0.5 to 4.6	V
		(Note 3)	-0.5 to V_{CCA} + 0.5	
	$V_{I/OB}$	(Note 2)	-0.5 to 4.6	
		(Note 3)	-0.5 to V_{CCB} + 0.5	
Input diode current	I_{IK}		-50	mA
I/O diode current	$I_{I/OK}$	(Note 4)	±50	mA
Output current	I_{OUTA}		±25	mA
	I_{OUTB}		±25	
V_{CC}/ground current per supply pin	I_{CCA}		±50	mA
	I_{CCB}		±50	
Power dissipation	P_D		180	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.
Note 2: Output in OFF state.
Note 3: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.
Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

11. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	—	1.1 to 2.7	V
	V_{CCB}			1.65 to 3.6	
Input voltage(DIR, $\overline{OE}$)	V_{IN}		—	0 to 3.6	V
Bus I/O voltage	$V_{I/OA}$	(Note 2)	—	0 to 3.6	V
		(Note 3)		0 to V_{CCA}	
	$V_{I/OB}$	(Note 2)		0 to 3.6	
		(Note 3)		0 to V_{CCB}	
Output current	I_{OUTA}		V_{CCA} = 2.3 to 2.7 V	±9	mA
			V_{CCA} = 1.65 to 1.95 V	±3	
			V_{CCA} = 1.4 to 1.6 V	±1	
	I_{OUTB}		V_{CCB} = 3.0 to 3.6 V	±12	
			V_{CCB} = 2.3 to 2.7 V	±9	
			V_{CCB} = 1.65 to 1.95 V	±3	
Operating temperature	T_{opr}		—	-40 to 85	°C
Input rise and fall times	dt/dv		V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

Note 1: Don't use at $V_{CCA} > V_{CCB}$.

Note 2: Output in OFF state.

Note 3: High (H) or Low (L) state.

12. Electrical Characteristics

12.1. DC Characteristics

12.1.1. 2.3 V ≤ V_{CCA} ≤ 2.7 V, 2.7 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 85 ℃)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		2.3 to 2.7	2.7 to 3.6	1.6	—	V
	V_{IHB}	Bn		2.3 to 2.7	2.7 to 3.6	2.0	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		2.3 to 2.7	2.7 to 3.6	—	0.7	V
	V_{ILB}	Bn		2.3 to 2.7	2.7 to 3.6	—	0.8	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	2.3 to 2.7	2.7 to 3.6	V_{CCA} -0.2	—	V
			I_{OHA} = -9 mA	2.3	2.7 to 3.6	1.7	—	
	V_{OHB}		I_{OHB} = -100 μA	2.3 to 2.7	2.7 to 3.6	V_{CCB} -0.2	—	
			I_{OHB} = -12 mA	2.3 to 2.7	3.0	2.2	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	2.3 to 2.7	2.7 to 3.6	—	0.2	V
			I_{OLA} = 9 mA	2.3	2.7 to 3.6	—	0.6	
	V_{OLB}		I_{OLB} = 100 μA	2.3 to 2.7	2.7 to 3.6	—	0.2	
			I_{OLB} = 12 mA	2.3 to 2.7	3.0	—	0.55	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.3 to 2.7	2.7 to 3.6	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.3 to 2.7	2.7 to 3.6	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		2.3 to 2.7	2.7 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		2.3 to 2.7	0	—	2.0	
	I_{OFF3}			2.3 to 2.7	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		2.3 to 2.7	2.7 to 3.6	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		2.3 to 2.7	2.7 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		2.3 to 2.7	2.7 to 3.6	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		2.3 to 2.7	2.7 to 3.6	—	±2.0	
	I_{CCTB}	V_{INB} = V_{CCB} - 0.6 V per input		2.3 to 2.7	2.7 to 3.6	—	750.0	

12.1.2. 1.65 V ≤ V_{CCA} < 2.3 V, 2.7 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.65 to 2.3	2.7 to 3.6	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.65 to 2.3	2.7 to 3.6	2.0	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.65 to 2.3	2.7 to 3.6	—	0.35× V_{CCA}	V
	V_{ILB}	Bn		1.65 to 2.3	2.7 to 3.6	—	0.8	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.65 to 2.3	2.7 to 3.6	V_{CCA} -0.2	—	V
			I_{OHA} = -3 mA	1.65	2.7 to 3.6	1.25	—	
	V_{OHB}		I_{OHB} = -100 μA	1.65 to 2.3	2.7 to 3.6	V_{CCB} -0.2	—	
			I_{OHB} = -12 mA	1.65 to 2.3	3.0	2.2	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.65 to 2.3	2.7 to 3.6	—	0.2	V
			I_{OLA} = 3 mA	1.65	2.7 to 3.6	—	0.3	
	V_{OLB}		I_{OLB} = 100 μA	1.65 to 2.3	2.7 to 3.6	—	0.2	
			I_{OLB} = 12 mA	1.65 to 2.3	3.0	—	0.55	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 2.3	2.7 to 3.6	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 2.3	2.7 to 3.6	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.65 to 2.3	2.7 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.65 to 2.3	0	—	2.0	
	I_{OFF3}			1.65 to 2.3	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 2.3	2.7 to 3.6	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 2.3	2.7 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.65 to 2.3	2.7 to 3.6	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.65 to 2.3	2.7 to 3.6	—	±2.0	
	I_{CCTB}	V_{INB} = V_{CCB} - 0.6 V per input		1.65 to 2.3	2.7 to 3.6	—	750.0	

12.1.3. 1.4 V ≤ V_{CCA} < 1.65 V, 2.7 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.4 to 1.65	2.7 to 3.6	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.4 to 1.65	2.7 to 3.6	2.0	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.4 to 1.65	2.7 to 3.6	—	0.30× V_{CCA}	V
	V_{ILB}	Bn		1.4 to 1.65	2.7 to 3.6	—	0.8	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.4 to 1.65	2.7 to 3.6	V_{CCA} -0.2	—	V
			I_{OHA} = -1 mA	1.4	2.7 to 3.6	1.05	—	
	V_{OHB}		I_{OHB} = -100 μA	1.4 to 1.65	2.7 to 3.6	V_{CCB} -0.2	—	
			I_{OHB} = -12 mA	1.4 to 1.65	3.0	2.2	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.4 to 1.65	2.7 to 3.6	—	0.2	V
			I_{OLA} = 1 mA	1.4	2.7 to 3.6	—	0.35	
	V_{OLB}		I_{OLB} = 100 μA	1.4 to 1.65	2.7 to 3.6	—	0.2	
			I_{OLB} = 12 mA	1.4 to 1.65	3.0	—	0.55	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.4 to 1.65	2.7 to 3.6	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.4 to 1.65	2.7 to 3.6	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.4 to 1.65	2.7 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.4 to 1.65	0	—	2.0	
	I_{OFF3}			1.4 to 1.65	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.4 to 1.65	2.7 to 3.6	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.4 to 1.65	2.7 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.4 to 1.65	2.7 to 3.6	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.4 to 1.65	2.7 to 3.6	—	±2.0	
	I_{CCTB}	V_{INB} = V_{CCB} - 0.6 V per input		1.4 to 1.65	2.7 to 3.6	—	750.0	

12.1.4. 1.1 V ≤ V_{CCA} < 1.4 V, 2.7 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.1 to 1.4	2.7 to 3.6	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.1 to 1.4	2.7 to 3.6	2.0	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.1 to 1.4	2.7 to 3.6	—	0.30× V_{CCA}	V
	V_{ILB}	Bn		1.1 to 1.4	2.7 to 3.6	—	0.8	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.1 to 1.4	2.7 to 3.6	V_{CCA} -0.2	—	V
	V_{OHB}		I_{OHB} = -100 μA	1.1 to 1.4	2.7 to 3.6	V_{CCB} -0.2	—	
			I_{OHB} = -12 mA	1.1 to 1.4	3.0	2.2	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.1 to 1.4	2.7 to 3.6	—	0.2	V
	V_{OLB}		I_{OLB} = 100 μA	1.1 to 1.4	2.7 to 3.6	—	0.2	
			I_{OLB} = 12 mA	1.1 to 1.4	3.0	—	0.55	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	2.7 to 3.6	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	2.7 to 3.6	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.1 to 1.4	2.7 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.1 to 1.4	0	—	2.0	
	I_{OFF3}			1.1 to 1.4	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	2.7 to 3.6	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	2.7 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	2.7 to 3.6	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	2.7 to 3.6	—	±2.0	
	I_{CCTB}	V_{INB} = V_{CCB} - 0.6 V per input		1.1 to 1.4	2.7 to 3.6	—	750.0	

12.1.5. 1.65 V ≤ V_{CCA} < 2.3 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.65 to 2.3	2.3 to 2.7	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.65 to 2.3	2.3 to 2.7	1.6	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.65 to 2.3	2.3 to 2.7	—	0.35× V_{CCA}	V
	V_{ILB}	Bn		1.65 to 2.3	2.3 to 2.7	—	0.7	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.65 to 2.3	2.3 to 2.7	V_{CCA} -0.2	—	V
			I_{OHA} = -3 mA	1.65	2.3 to 2.7	1.25	—	
	V_{OHB}		I_{OHB} = -100 μA	1.65 to 2.3	2.3 to 2.7	V_{CCB} -0.2	—	
			I_{OHB} = -9 mA	1.65 to 2.3	2.3	1.7	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.65 to 2.3	2.3 to 2.7	—	0.2	V
			I_{OLA} = 3 mA	1.65	2.3 to 2.7	—	0.3	
	V_{OLB}		I_{OLB} = 100 μA	1.65 to 2.3	2.3 to 2.7	—	0.2	
			I_{OLB} = 9 mA	1.65 to 2.3	2.3	—	0.6	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 2.3	2.3 to 2.7	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 2.3	2.3 to 2.7	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.65 to 2.3	2.3 to 2.7	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.65 to 2.3	0	—	2.0	
	I_{OFF3}			1.65 to 2.3	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 2.3	2.3 to 2.7	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 2.3	2.3 to 2.7	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.65 to 2.3	2.3 to 2.7	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.65 to 2.3	2.3 to 2.7	—	±2.0	

12.1.6. 1.4 V ≤ V_{CCA} < 1.65 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.4 to 1.65	2.3 to 2.7	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.4 to 1.65	2.3 to 2.7	1.6	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.4 to 1.65	2.3 to 2.7	—	0.30× V_{CCA}	V
	V_{ILB}	Bn		1.4 to 1.65	2.3 to 2.7	—	0.7	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.4 to 1.65	2.3 to 2.7	V_{CCA} -0.2	—	V
			I_{OHA} = -1 mA	1.4	2.3 to 2.7	1.05	—	
	V_{OHB}		I_{OHB} = -100 μA	1.4 to 1.65	2.3 to 2.7	V_{CCB} -0.2	—	
			I_{OHB} = -9 mA	1.4 to 1.65	2.3	1.7	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.4 to 1.65	2.3 to 2.7	—	0.2	V
			I_{OLA} = 1 mA	1.4	2.3 to 2.7	—	0.35	
	V_{OLB}		I_{OLB} = 100 μA	1.4 to 1.65	2.3 to 2.7	—	0.2	
			I_{OLB} = 9 mA	1.4 to 1.65	2.3	—	0.6	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.4 to 1.65	2.3 to 2.7	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.4 to 1.65	2.3 to 2.7	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.4 to 1.65	2.3 to 2.7	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.4 to 1.65	0	—	2.0	
	I_{OFF3}			1.4 to 1.65	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.4 to 1.65	2.3 to 2.7	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.4 to 1.65	2.3 to 2.7	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.4 to 1.65	2.3 to 2.7	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.4 to 1.65	2.3 to 2.7	—	±2.0	

12.1.7. 1.1 V ≤ V_{CCA} < 1.4 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.1 to 1.4	2.3 to 2.7	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.1 to 1.4	2.3 to 2.7	1.6	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.1 to 1.4	2.3 to 2.7	—	0.30× V_{CCA}	V
	V_{ILB}	Bn		1.1 to 1.4	2.3 to 2.7	—	0.7	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.1 to 1.4	2.3 to 2.7	V_{CCA} -0.2	—	V
	V_{OHB}		I_{OHB} = -100 μA	1.1 to 1.4	2.3 to 2.7	V_{CCB} -0.2	—	
			I_{OHB} = -9 mA	1.1 to 1.4	2.3	1.7	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.1 to 1.4	2.3 to 2.7	—	0.2	V
	V_{OLB}		I_{OLB} = 100 μA	1.1 to 1.4	2.3 to 2.7	—	0.2	
			I_{OLB} = 9 mA	1.1 to 1.4	2.3	—	0.6	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	2.3 to 2.7	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	2.3 to 2.7	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.1 to 1.4	2.3 to 2.7	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.1 to 1.4	0	—	2.0	
	I_{OFF3}			1.1 to 1.4	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	2.3 to 2.7	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	2.3 to 2.7	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	2.3 to 2.7	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	2.3 to 2.7	—	±2.0	

12.1.8. 1.1 V ≤ V_{CCA} < 1.4 V, 1.65 V ≤ V_{CCB} < 2.3 V (Unless otherwise specified, T_a = -40 to 85 ℃)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	DIR, $\overline{OE}$, An		1.1 to 1.4	1.65 to 2.3	0.65× V_{CCA}	—	V
	V_{IHB}	Bn		1.1 to 1.4	1.65 to 2.3	0.65× V_{CCB}	—	
Low-level input voltage	V_{ILA}	DIR, $\overline{OE}$, An		1.1 to 1.4	1.65 to 2.3	—	0.30× V_{CCA}	V
	V_{ILB}	Bn		1.1 to 1.4	1.65 to 2.3	—	0.35× V_{CCB}	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = -100 μA	1.1 to 1.4	1.65 to 2.3	V_{CCA} -0.2	—	V
	V_{OHB}		I_{OHB} = -100 μA	1.1 to 1.4	1.65 to 2.3	V_{CCB} -0.2	—	
			I_{OHB} = -3 mA	1.1 to 1.4	1.65	1.25	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.1 to 1.4	1.65 to 2.3	—	0.2	V
	V_{OLB}		I_{OLB} = 100 μA	1.1 to 1.4	1.65 to 2.3	—	0.2	
			I_{OLB} = 3 mA	1.1 to 1.4	1.65	—	0.3	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	1.65 to 2.3	—	±2.0	μA
	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.1 to 1.4	1.65 to 2.3	—	±2.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		1.1 to 1.4	1.65 to 2.3	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} V_{IN}, V_{OUT} = 0 to 3.6 V		1.1 to 1.4	0	—	2.0	
	I_{OFF3}			1.1 to 1.4	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	1.65 to 2.3	—	2.0	μA
	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.1 to 1.4	1.65 to 2.3	—	2.0	
	I_{CCA}	V_{CCA} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	1.65 to 2.3	—	±2.0	
	I_{CCB}	V_{CCB} ≤ (V_{IN}, V_{OUT}) ≤ 3.6 V		1.1 to 1.4	1.65 to 2.3	—	±2.0	

12.2. AC Characteristics

12.2.1. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	5.4	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	8.4	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	6.7	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	6.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	8.7	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	3.9	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.2. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	8.9	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	13.4	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	10.9	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	7.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	10.7	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	5.2	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.3. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	10.3	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	18.5	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	13.0	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	8.6	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	14.3	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	6.6	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.4. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	61	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	95	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	44	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	22	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	52	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	18	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.5. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	9.1	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	13.5	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	11.8	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	9.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	12.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	5.1	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.6. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	10.8	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	18.3	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	14.2	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	10.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	15.4	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	6.4	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

12.2.7. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	60	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	95	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	45	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	23	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	54	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	17	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

12.2.8. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	58	ns
3-state output enable time ($\overline{OE}$ → An)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	92	
3-state output disable time ($\overline{OE}$ → An)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	47	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 13.1, 14.1 Table 13.1.1, 13.1.2, 14.1.1	1.0	30	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	55	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 13.1, 14.2 Table 13.1.1, 13.1.2, 14.1.1	1.0	17	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

12.3. Dynamic Switching Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF)

Characteristics		Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	A → B	V_{OLP}	(Note 1)	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	3.3	0.8	V
					1.8	3.3	0.8	
					1.8	2.5	0.6	
	B → A				2.5	3.3	0.6	
					1.8	3.3	0.25	
					1.8	2.5	0.25	
Quiet output minimum dynamic V_{OL}	A → B	V_{OLV}	(Note 1)	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	3.3	-0.8	V
					1.8	3.3	-0.8	
					1.8	2.5	-0.6	
	B → A				2.5	3.3	-0.6	
					1.8	3.3	-0.25	
					1.8	2.5	-0.25	
Quiet output maximum dynamic V_{OH}	A → B	V_{OHP}	(Note 1)	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	3.3	4.6	V
					1.8	3.3	4.6	
					1.8	2.5	3.3	
	B → A				2.5	3.3	3.3	
					1.8	3.3	2.3	
					1.8	2.5	2.3	
Quiet output minimum dynamic V_{OH}	A → B	V_{OHV}	(Note 1)	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	3.3	2.0	V
					1.8	3.3	2.0	
					1.8	2.5	1.7	
	B → A				2.5	3.3	1.7	
					1.8	3.3	1.3	
					1.8	2.5	1.3	

Note 1: Parameter guaranteed by design.

12.4. Capacitive Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance	C_{IN}		DIR, $\overline{OE}$		2.5	3.3	7	pF
Bus I/O capacitance	$C_{I/O}$		An, Bn		2.5	3.3	8	pF
Power dissipation capacitance	C_{PDA}	(Note 1)	$\overline{OE}$ = L	A → B (DIR = H)	2.5	3.3	3	pF
				B → A (DIR = L)	2.5	3.3	16	
			$\overline{OE}$ = H	A → B (DIR = H)	2.5	3.3	0	
				B → A (DIR = L)	2.5	3.3	0	
	C_{PDB}	(Note 1)	$\overline{OE}$ = L	A → B (DIR = H)	2.5	3.3	16	
				B → A (DIR = L)	2.5	3.3	5	
			$\overline{OE}$ = H	A → B (DIR = H)	2.5	3.3	0	
				B → A (DIR = L)	2.5	3.3	0	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per bit)

13. AC Test Circuit

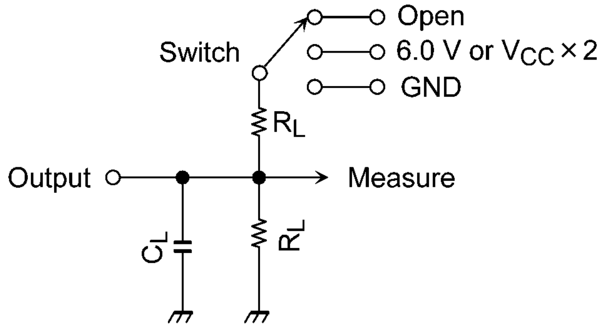


Fig. 13.1 AC Test Circuit

Table 13.1.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
t_{PLH}, t_{PHL}	Open	—
t_{PLZ}, t_{PZL}	6.0 V	V_{CC} = 3.3 ± 0.3 V
	V_{CC} × 2	V_{CC} = 2.5 ± 0.2 V
		V_{CC} = 1.8 ± 0.15 V
		V_{CC} = 1.5 ± 0.1 V
		V_{CC} = 1.2 ± 0.1 V
t_{PHZ}, t_{PZH}	GND	—

Table 13.1.2 Parameter for AC Test Circuit

Symbol	V_{CC} = 3.3 ± 0.3 V V_{CC} = 2.5 ± 0.2 V	V_{CC} = 1.8 ± 0.15 V	V_{CC} = 1.5 ± 0.1 V	V_{CC} = 1.2 ± 0.1 V
R_L	500 Ω	1 kΩ	2 kΩ	10 kΩ
C_L	30 pF	30 pF	15 pF	15 pF

14. AC Waveform

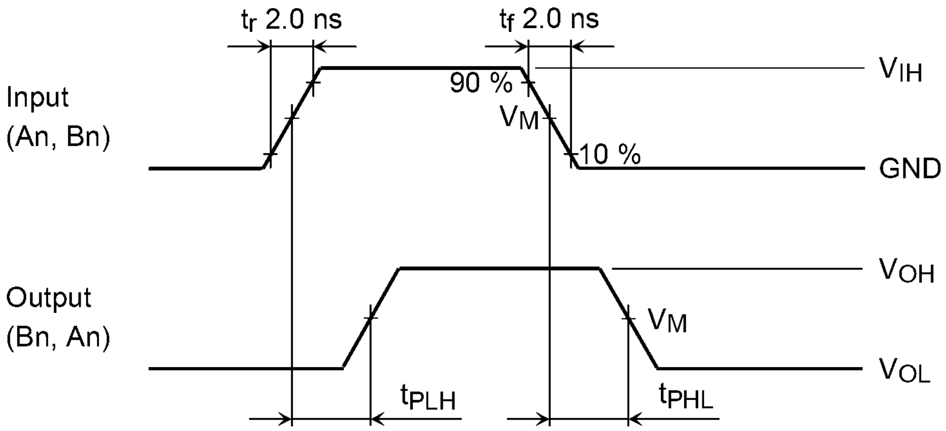


Fig. 14.1 t_{PLH}, t_{PHL}

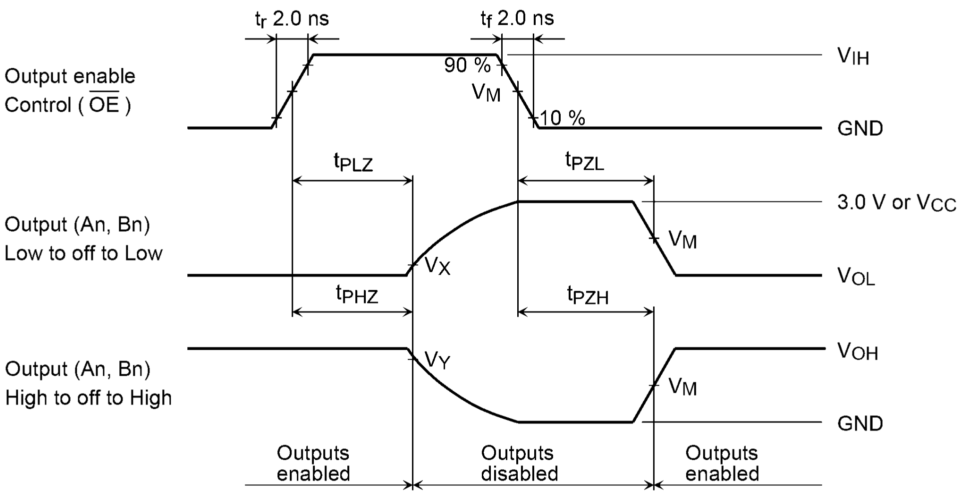


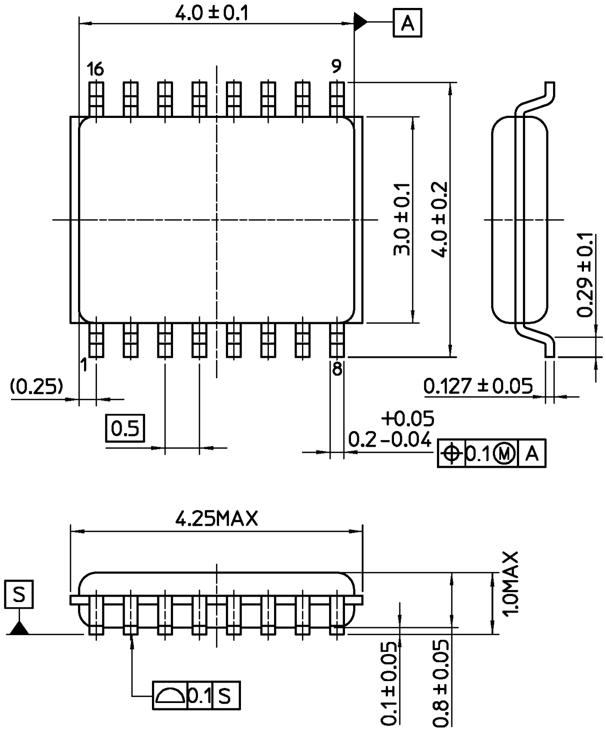
Fig. 14.2 t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Table 14.1.1 AC Waveform Symbols

Symbol	V_{CC} = 3.3 ± 0.3 V	V_{CC} = 2.5 ± 0.2 V V_{CC} = 1.8 ± 0.15 V	V_{CC} = 1.5 ± 0.1 V V_{CC} = 1.2 ± 0.1 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.1 V
V_Y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	V_{OH} - 0.1 V

Package Dimensions

Unit: mm



Weight: 0.02 g (typ.)

Package Name(s)
Nickname: US16

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