PRELIMINARY

4-BIT SINGLE-CHIP MICROPROCESSOR WITH VOICE SYNTHESIZER

■ GENERAL DESCRIPTION

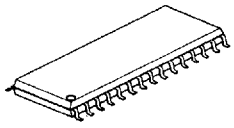
The NJU3811 is a C-MOS 4-bit single-chip microprocessor with 6-bit PCM voice synthesizer,operated 2.4V minimum.

The microprocessor contains 1k-word ROM, 64-nibble RAM, four input ports, eight output ports, two I/O ports and a hardware-interrupt and perfroms system and voice synthesis control.

The voice synthsizer incorporates 4 seconds of a dedicated ROM whcih can be divided into individual memory sections and output the voice under microprocessor control.

It is used in a wide field for many applications such as toys and home electronic appliances free from problems of interface and space, because the microprocessor and voice synthesizer are combined in single-chip.

■ PACKAGE OUTLINE



NJU3811M-XX

■ FEATURES

<MICROPROCESSOR BLOCK>

- Built-in ROM : 1k words x 8-bit
- Built-in RAM : 64 words x 4-bit
- Instruction : 59 instructions
- Output Port : 8 ports
- Input Port : 4 ports
- I/O Port : 2 I/O ports
- Timer Interrupt : 1 port (8-bit Timer/Counter)
- External Interrupt : 1 port
- Min. Instruction Cycle : 3.9 us

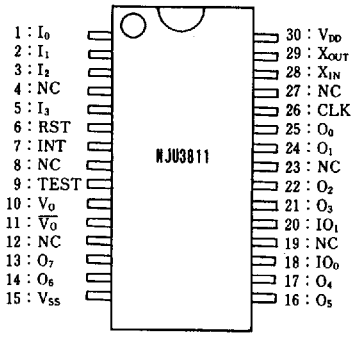
<VOICE SYNTHESIS BLOCK>

- 6-bit PWM Method
- Dedicated Voice ROM : 24k words x 6-bit
- Synthesis Time : 4 seconds Max.(Internal ROM)
- Piezo Buzzer Direct Driving

<COMMON FEATURES>

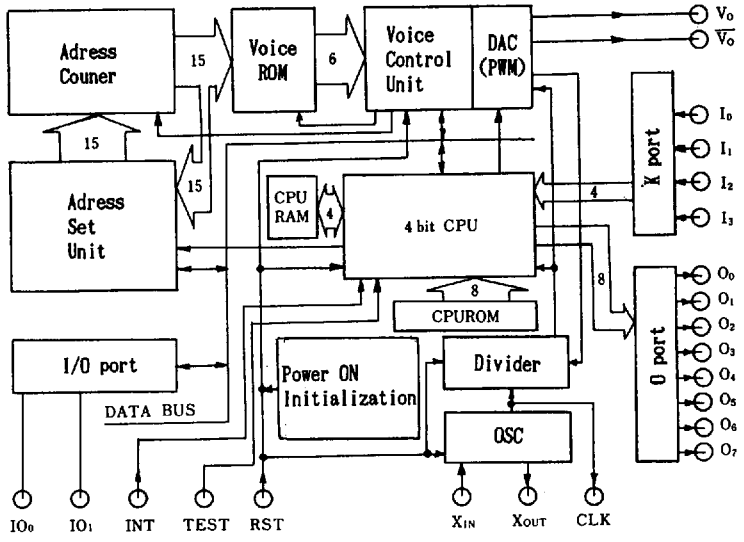
- Operating Voltage : 2.4-5.4V
- Built-in Power-On-Initialization Circuits
- External Reset Input Terminal
- Built-in CR Oscillation Circuits
- Package Outline : DMP30
- C-MOS Technology

■ PIN CONFIGURATION



8

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1,2,3,5	$I_0 \sim I_4$	4 bit input terminals (with Pull-down resistance)
25,24,22 21,17,16 14,13	$O_0 \sim O_7$	8 bit output terminals
18,20	IO_0, IO_1	2 bit input/output terminals
6	RST	External reset input terminal
7	INT	External interrupt input terminal
9	TEST	Test terminal (Normally Open)
10,11	$V_O, \overline{V_O}$	Voice synthsizer output terminals
26	CLK	Clock monitor terminal
28,29	X_{IN}, X_{OUT}	Oscillation terminals (External R connect to these terminals)
30,15	V_{DD}, V_{SS}	Voltage Supply terminals
4,8,12 19,23,27	NC	Non connection

■ FUNCTIONAL DESCRIPTION

(1) BUILT-IN CPU

The 4-bit CPU of the NJU3811 combines four dedicated Input ports(K port), eight dedicated Output ports, two programable Input/Output ports(I/O port), an internal Timer/Counter(of 8-bit) interrupt, an external hardware interrupt, 1k-byte ROM (as the real programing area) and 64-nibble RAM.

This system control program coding can be written-in using the same MASK for voice ROM data.

(2) VOICE SYNTHESIZER

The 6-bit voice synthesis block can be sectioned and mapped as desired as the start and end address are pointed to by the user programing. (Real Voice ROM Address is 0080h-5DFFh: Maximum synthesis 4 seconds in total.)

The form of the voice data for output may be either a polarity bit plus 5-bit PWM D/A conversion output (for direct Piezo driving: Terminal V_O, $\overline{V_O}$) or a 6-bit PWM type D/A conversion output (Terminal V_O only is used for output; $\overline{V_O}$ = high impedance).

This selection is an option which can be coded using the same MASK for the CPU and voice ROMs.

(3) VOICE SYNTHESIZER OUTPUT

Two output forms of the voice data on the terminal V_O and $\overline{V_O}$ are available, either in the Single mode or the Double mode which are options coded on the same MASK for the CPU ROM and the Voice ROM.

The voice date are Pulse-Width-Modulation using the 6KHz sampling rate.

- SINGLE MODE

The single mode is a form of an output composed of a polarity bit and 5-bit PWM voice data. This mode suits for direct driving of a Piezo(piezo buzzer) using both output terminals V_O and $\overline{V_O}$.

The data is output in the form of pulse-strings, each pulse cycling in aproximately 0.65us (1/768KHz/2).

- DOUBLE MODE

The double mode is a form of an output composed of 6-bit PWM convered voice data. In this mode the V_O terminal only is used as output terminal and $\overline{V_O}$ terminal becomes high impedance state because the polarity bit is not output.

The data are output in the form of pulse-strings, each pulse cycling in aproximately 0.325us (1/1.536MHz/2).

In an output, Low-Pass-Filter using is recommended to prevend the noise appearing on the output, shown in the application circuits diagram.

(4) CR OSCILLATION CIRCUITS

The CR oscillation circuits requires an external resistor connect to the X_{IN} and X_{OUT} terminal. When the external clock operation, use the X_{IN} termainal as a clock-input terminal. (X_{OUT} terminal is open in that case.)

Supply Voltage	Resistance Value	Oscillation Frequency
3V	29KΩ	1.536MHz
5V	31KΩ	1.536MHz

(5) POWER-ON-INITIALIZATION

When the power on, the NJU3811 is initialized by builted in power-on-initialization circuits. The external reset can also be instructed by rising the RST terminal to H state.

Initialized CPU status / Program Counter: 0
Stack pointer : 0
Staus : 1
Interrupt : disabled

■ INSTRUCTION SET FOR CPU BLOCK 1

	OP Code	Object	Function	Status (ST=1)	Cycle	Note
DATA TRANSMISSION	TAY	04	Y←AC		1	PRC=0
			Y'←AC		1	PRC=1
	TYA	14	AC←Y		1	PRC=0
			AC←Y'		1	PRC=1
	XAX	1B	AC↔X		1	PRC=0
			AC↔X'		1	PRC=1
	TAP	26	PH(Y')←AC		1	
	TPA	16	AC←PH(Y')		1	
	TAPICY	17	PH(Y')←AC, Y←Y+1	CY=1	1	
	TAPDCY	27	PH(Y')←AC, Y←Y−1	BW≠1	1	
	TMA	0D	AC←M(X, Y)		1	
	TAM	1D	M(X, Y)←AC		1	
	TAMICY	0A	M(X, Y)←AC, Y←Y+1	CY=1	1	
	TAMDCY	1A	M(X, Y)←AC, Y←Y−1	BW≠1	1	
	TMY	05	Y←M(X, Y)		1	RPC=0
			Y'←M(X, Y)		1	RPC=1
	XMA	0B	M(X, Y)↔AC		1	
	TPMICY	03	M(X, Y)←PH(Y'), Y←Y+1	CY=1	1	
	TMPICY	13	PH(Y')←M(X, Y), Y←Y+1	BW≠1	1	
	TRM	23	M(X, Y)←ROM[PH(Y'=13, 14), X', A]		1	YLSB=0: **Lower data** YLSB=1: **Upper data**
	CLA	80	AC←0		1	
	LDI A, #K	80−8F	AC←#K, #K=0−15		1	
	LDI Y, #K	90−9F	Y←#K, #K=0−15		1	RPC=0
			Y'←#K, #K=0−15		1	RPC=1
	LDI X, #K	A0−AF	X←#K, #K=0−15		1	RPC=0
			X'←#K, #K=0−15		1	RPC=1
BIT OPERATION	SBIT b	30−33	$M(X, Y)_b$←1, b=0−3		1	
	RBIT b	34−37	$M(X, Y)_b$←0, b=0−3		1	
	TBIT b	38−38	Test $M(X, Y)_b$, b=0−3	M(X,Y) b=1	1	
	TBA b	3C−3F	Test AC_b, b=0−3	(AC) b=1	1	
	RAR	21	Rotate Right Accumulator	CY=1	1	
	RAL	22	Rotate Left Accumulator	CY=1	1	
	RYR	24	Rotate Right Yreg	CY=1	1	RPC=0
			Rotate Right Y'reg	CY=1	1	RPC=1
	RYL	25	Rotate Left Yreg	CY=1	1	RPC=0
			Rotate Left Y'reg	CY=1	1	RPC=1
	RXR	28	Rotate Right Xreg	CY=1	1	RPC=0
			Rotate Right X'reg	CY=1	1	RPC=1
	RXL	29	Rotate Left Xreg	CY=1	1	RPC=0
			Rotate Left X'reg	CY=1	1	RPC=1
	SEC	0C	Set Carry	1	1	
	CLC	1C	Clear Carry	0	1	

8

■ INSTRUCTION SET FOR CPU BLOCK 2

	OP Code	Object	Function	Status(ST=1)	Cycle	Note
	ADD A, M	0E	AC←M(X, Y)+AC	CY=1	1	
	INC A	71	AC←AC+1	CY=1	1	
	DEC A	7F	AC←AC−1	BW≠1	1	
	ADD A, #K	70−7F	AC←AC+K, K=0−15	CY=1	1	
	AND A, M	0F	AC←AC∧M(X, Y)	AC≠0	1	
	CMP A, M	2E	M(X, Y)$\stackrel{?}{=}$AC	M(X, Y)≠AC	1	
	CMP Y, #K	B0−BF	Y$\stackrel{?}{=}$#K, #K=0−15	Y≠#K	1	
	INC Y	08	Y←Y+1	CY=1	1	RPC=0
			Y'←Y'+1	CY=1	1	RPC=1
	DEC Y	18	Y←Y−1	BW≠1	1	RPC=0
			Y'←Y'−1	BW≠1	1	RPC=1
	INC M	09	AC←M(X, Y)+1	CY=1	1	
	DEC M	19	AC←M(X, Y)−1	BW≠1	1	
	YNEA	01	Y≠A	Y≠A	1	
	OR A, M	1F	AC←AC∨M(X, Y)	AC≠0	1	
	XOR A, M	2F	AC←AC⊕M(X, Y)	AC≠0	1	
	NEG	2D	AC←0−AC		1	
	SUB A, M	1E	AC←M(X, Y)−AC	AC≠0	1	
	AND A, #K	40−4F	AC←AC∧#K, #K=0−15	AC≠0	1	
	OR A, #K	50−5F	AC←AC∨#K, #K=0−15	AC≠0	1	
	OUTR	02	O−REG←ROM[PH(Y'=13, 14), X', A]		2	
			AC←AC+1	CY=1		
	INK	12	AC←(K port)		1	
	JPL addr	68−6F	ST=1:Branch ST=0:Non Branch		2	2 byte Instruction
	JMP addr	C0−FF	ST=1:Branch ST=0:Non Branch		1	
	CALL add	60−67	ST=1:Subroutine call , ST=0:Non Subroutine call		2	2 byte Instruction
	RET	2B	Return from Subroutine		1	
	RETI	2C	Return from Interrupt Routine		1	
	NOP	00	No Operation		1	
	SRPC	10	RPC←1		1	
	RRPC	20	RPC←0		1	
	MDT	06	Memory Dump Testing			

8

* Expranation of mark

←: Tran direction	AC: Accumulator	PC: Program Counter	
∧: Logic AND	X: X Register	SPC: Stock Pointer	
∨: Logic OR	X': X' Register	KP: K Port	
⊕: EXCRUSIVE OR	Y: Y Register	OP: O Port	
+: Add	Y': Y' Register	#K: Immediate data	
−: Subtraction	PH: Peripheral Register	( ): Addressed by the address in the parenthesis	
$\stackrel{?}{=}$: Compare	M: Data Memory		
	ROM: Read only memory		
	ST: Status Flag	addr: Execute Address	
	RPC: Instruction table change	b, b: n bit , n=1 ~ 3	

After execute the instruction

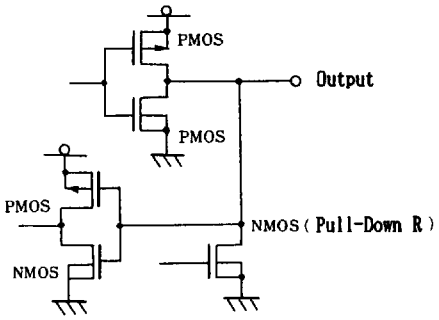
Meet the condition ; 1 , Not meet the condition ; 0

CY ; Carry BW ; Borrow

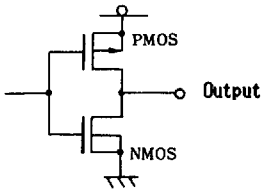
After execute the no mentioned status instruction, the status becomes 1 always.

■ INPUT/OUTPUT CIRCUITS

• INPUT/OUTPUT TERMINALS
(with Pull-Down Resistance)
IO_0, IO_1, I_0~I_3, TEST

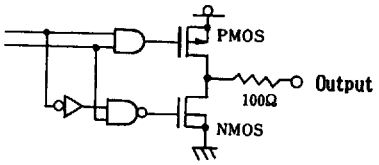


• OUTPUT TERMINALS
(without Pull-Down Resistance)
O_0~O_7, CLK

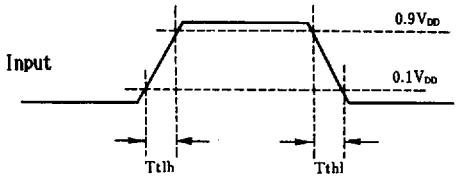


• INPUT TERMINALS
(with Schmitt)
RST, INT

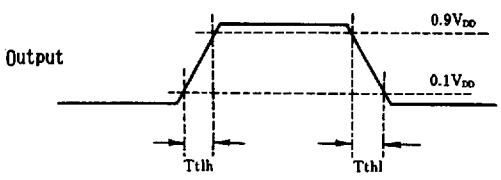
• OUTPUT TERMINALS
(Voice Output)
V_O, $\overline{V_O}$



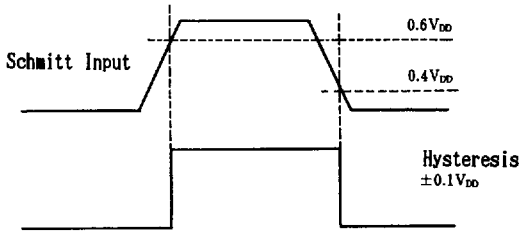
■ INPUT/OUTPUT CHARACTERISTICS



Ttlh = 0 ns (MIN) ~ 100ns (MAX)
Tthl = 0 ns (MIN) ~ 100ns (MAX)



Ttlh = 5ns (MIN) ~ 50ns (MAX)
Tthl = 5ns (MIN) ~ 50ns (MAX)



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}~V_{SS}	- 0.3 ~ + 6.5	V
Input Voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output Voltage	V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 20 ~ + 70	℃
Storage Temperature	Tstg	- 55 ~ + 125	℃

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=25℃, V_{DD}=4.5V, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}	V_{DD} Terminal	2.4		5.4	V
Stand-by Current	I_{DD1}				3.0	μA
Operating Current	I_{DD2}	V_O, $\overline{V_O}$ Terminals=Open		3.0	5.0	mA
Input Voltage	V_{IH}		V_{DD}-0.8			V
	V_{IL}				V_{SS}+0.8	V
Output Current(PWM)	I_{OH1}	V_{OH}=V_{DD}/2	3.0	5.0		mA
	I_{OL2}	V_{OH}=V_{DD}/2	3.0	5.0		
Output Current (OUT Terminals)	I_{OO1}	V_{OH}=3.7V	1.0	2.0		mA
	I_{OO2}	V_{OH}=0.8V	1.0	2.0		
Output Current (CLK Terminal)	I_{OC1}	V_{OH}=3.7V	1.0	2.0		mA
	I_{OC2}	V_{OH}=0.8V	1.0	2.0		

AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{OSC}	V_{DD}=5V, R=31kΩ		1.536		MHz
Clock Cycle Time	$t_{C(\phi)}$		0.65			μs
Instruction Cycle Time	t_C		3.9			μs

8

■ APPLICATION CIRCUITS