SONY

CXA3108Q & CXA3038N

Digital Satellite Broadcast Chip-set Offers Low-Cost, Low Power Miniaturized Tuner Block Solution

Satellite broadcasting using digital modulation first entered the U.S. market in 1994. Today, as digital satellite broadcasting is expanding rapidly to world markets, OEMs are looking for smaller, more cost effective components to meet growing demand.

Sony Semiconductor Company of America recently announced a tuner chip-set for digital satellite broadcasting that integrates all the functions of the tuner in just two chips *(figure 1)*. By reducing the size and number of chips, it provides a low cost, easily integrated tuner block. The new chip-set con-

figure 1 DBS Reception Set-top Box Block Diagram

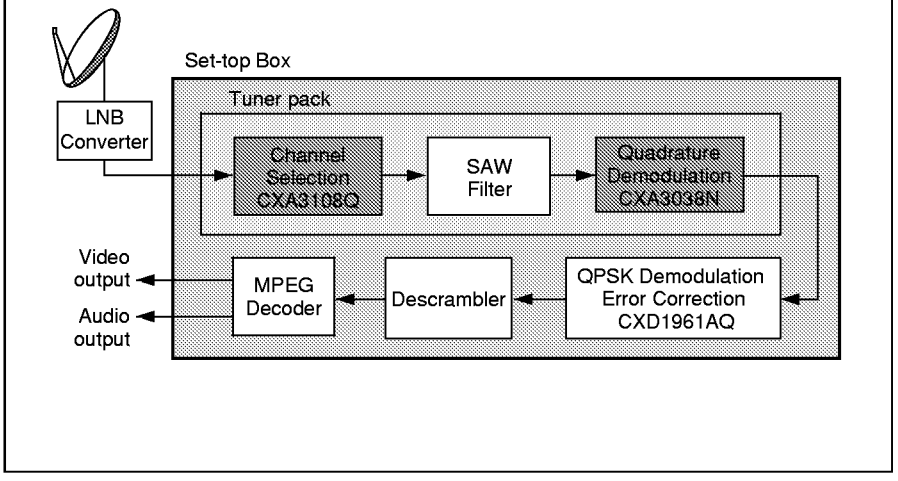
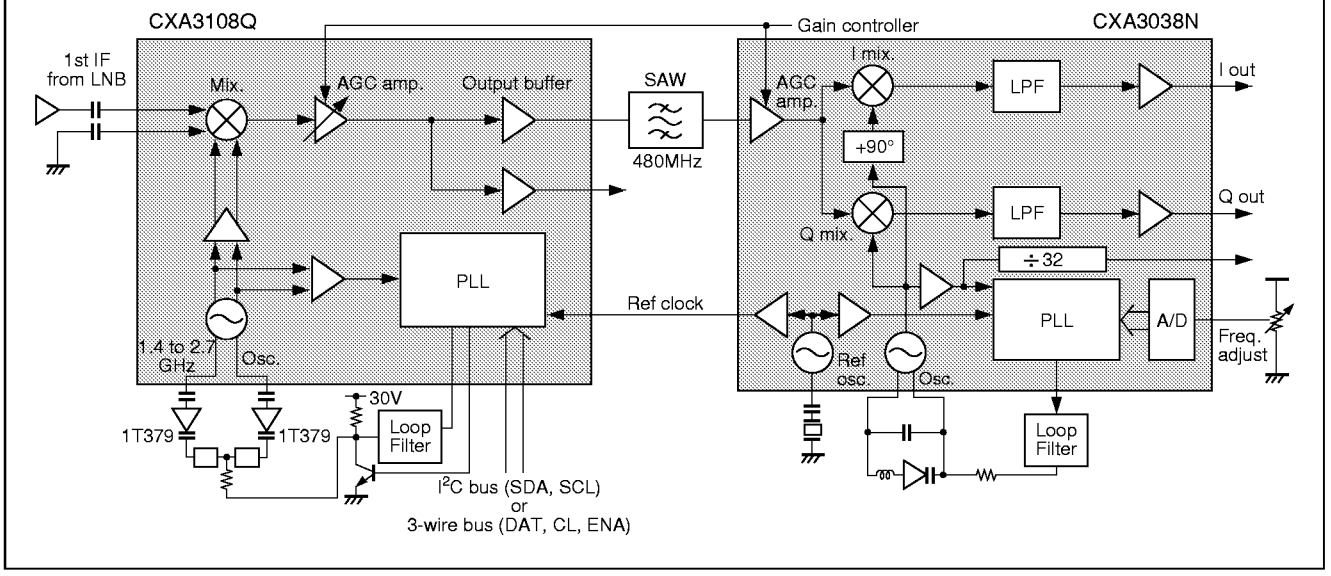


figure 2 CXA3108Q and CXA3038N Block Diagrams



sists of the CXA3108Q and the CXA3038N and is part of Sony's Virtuoso™ family of digital media devices *(figure 2)*.

The CXA3108Q takes full advantage of Sony's high-speed bipolar process by integrating an oscillator/mixer circuit for the L-band down converter functions and a phase lock loop (PLL) circuit for channel selection on a single chip rather than the two chips previously required. The onboard PLL control function supports both the I^2C bus and the three-wire bus allowing for a wider range of reference frequencies.

The benefits of this integration are realized in the newly developed P42 high-frequency linear process (fT = 30GHz). Sony also offers a unique differential Colpitts oscillator circuit, allowing this device to provide a stable oscillator signal

with no parasitic oscillation over the wide band of 1.3 to 2.7GHz. As shown (*figure 3*), the frequency conversion characteristics are extremely flat and produce high gain and low noise.

The CXA3038N features adjustment-free carrier recovery through the on-chip PLL circuit. This function is required for 480MHz band quadrature detection whenever an on-chip PLL circuit is present *(figure 4)*. Because the PLL circuit includes divide data, it can replace the high-cost SAW resonator and eliminate the need for an external

figure 3 CXA3108Q Frequency Conversion Characteristics

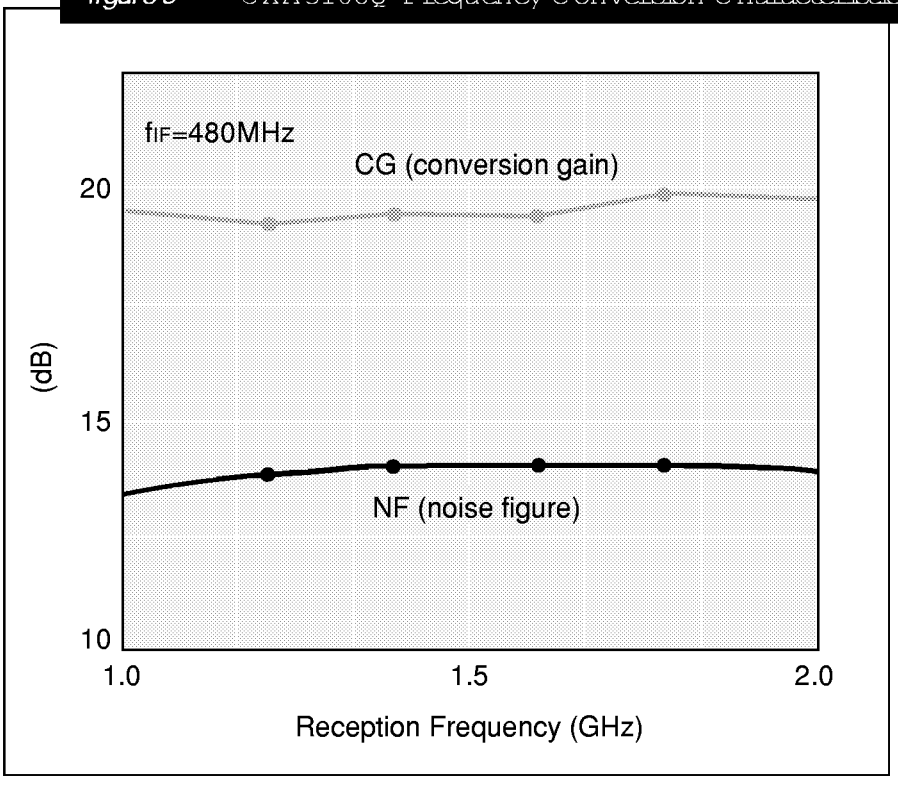
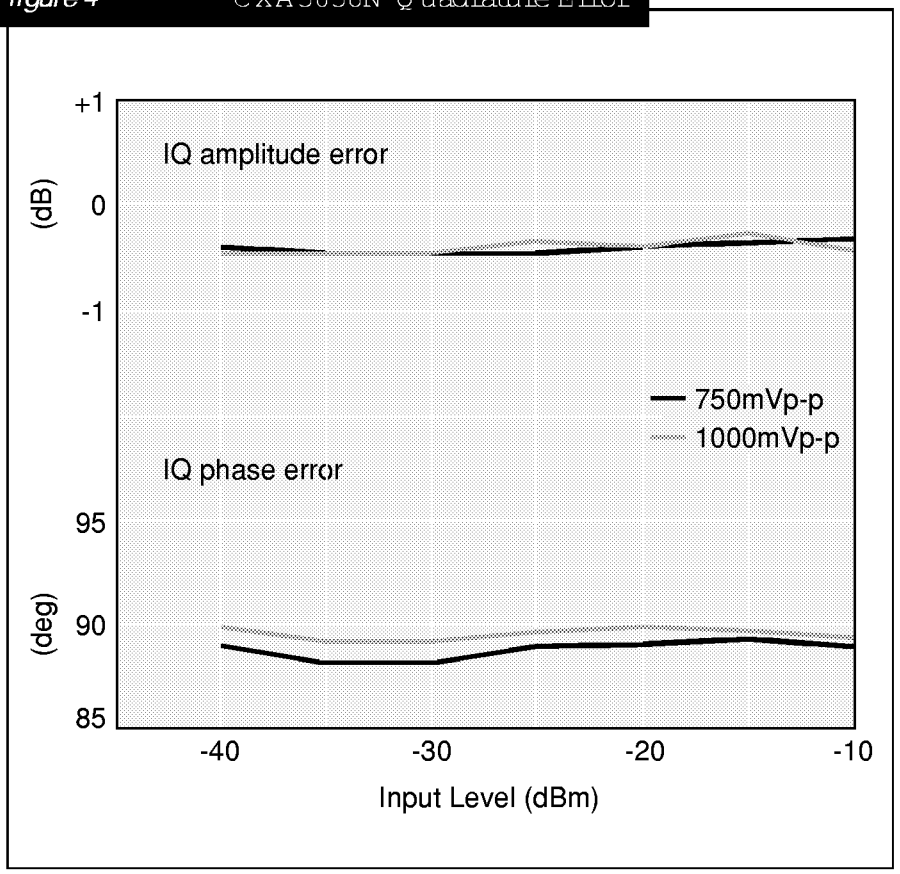


figure 4 CXA3038N Quadrature Error



control. The CXA3038N includes an A/D converter allowing the carrier frequency to be adjusted +450kHz steps from the center frequency of 479.5MHz .

Support for a Wide Range of Applications

While integrating the key features of a tuner block, Sony designed the chip-set to support a wide range of applications such as single-unit tuners for both analog and digital satellite broadcasts and tuners for both UHF and VHF broadcasts. This is achieved by integrating two IF output circuit systems on the CXA3108Q and an external input pin for the PLL circuit. The CXA3038N features an on-chip 32-frequency divider for local oscillator signals. This enables the support of older carrier recovery techniques when a PLL circuit is

included in the QPSK demodulation IC.

The devices consume 350mW and 250mW power respectively - a significant reduction over previous solutions. This feature makes the chip-set optimal for bit stream output tuner pack products that implement the whole tuner up to the QPSK demodulation and error correction circuit, which typically generates a significant amount of heat.

Sony's integration of high-frequency/low-noise analog circuits and high-speed digital circuits, as well as its ability to suppress mutual interference between the circuits, offers the highest functionality in the lowest number of chips. This new chip-set will greatly contribute to reduced cost and significant miniaturization of digital satellite broadcast tuner blocks.