2-Digit BCD Counter
671493

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Features/Benefits

- **Drive numeric displays**
- **Expansion in 2-digit increments**
- **24-pin SKINNYDIP® saves space**
- **Bus structured pinout**
- **Low current PNP inputs reduce loading**
- **Three-state output drive bus lines**

Description

The 2-digit BCD (Binary Coded Decimal) Counter is a synchronous counter with complementary count enables ($\overline{CE1}$, CE2), parallel load ($\overline{LD}$), and carry out ($\overline{CO}$). Three control inputs ($\overline{LD}$, $\overline{CE1}$, CE2) provide one of three operations which occur synchronously on the rising edge of the clock (CK).

The load operation loads the inputs (D1 and D2) into the output register (Q1 and Q2) when load is LOW. Note that the load line overrides the increment.

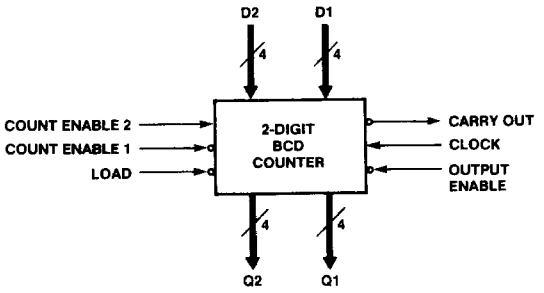
When $\overline{LD}$ is not active, the counter will increment in a Binary-Coded-Decimal sequence if both count enables are asserted ($\overline{CE1}$ = L and CE2 = H), otherwise it holds.

Two or more BCD Counters can be cascaded to implement larger BCD counters by connecting carry out ($\overline{CO}$) of the first stage to count enable ($\overline{CE1}$) of the second stage. This signal is not affected by $\overline{OE}$.

Parallel loading allows programmability of the BCD Counter and numeric indicator.

This BCD Counter is ideal in an industrial control application where an event counter is needed to drive numeric displays. The device can receive one count enable in the form of strobes from a motor or other device. The second count enable can receive the period signal. With connections in this manner, the counter counts events during a period. The device will provide two active high BCD outputs (Q1 and Q2) to drive two numeric indicators, which feature an on-board decoder/driver.

Block Diagram



Ordering Information

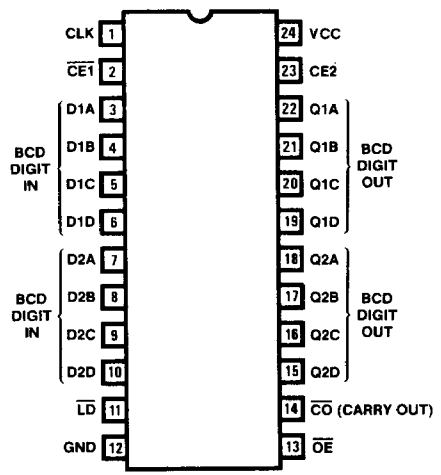
PART NUMBER	PACKAGE	TEMPERATURE
671493	NS, JS	Com

Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{CE1}$	CE2	D1A-D1D/ D2A-D2D	Q1A-Q1D/ Q2A-Q2D	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	X	X	D	D	Load
L	↑	H	H	X	X	Q	Hold (CE1=H)
L	↑	H	X	L	X	Q	Hold (CE2=L)
L	↑	H	L	H	X	Q plus 1	Increment

* When $\overline{OE}$ is HIGH, Q1 and Q2 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Pin Configuration



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Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Clock width	Low	35			ns
		High	25			
t_{su}	Setup time		50			ns
t_h	Hold time		0	−15		ns

Electrical Characteristics Over Operating Conditions

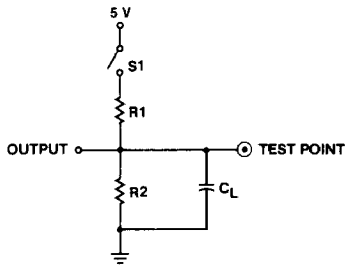
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	
I_{OS}**	Output short-circuit current**	V_{CC} = 5.0 V	V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* V_{IL} and V_{IH} are, in effect, input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $V_{IL} \leq 0.8$ V and $V_{IH} \geq 2.0$ V.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See test load)	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	Commercial, C_L = 50 pF, R_1 = 200 Ω, R_2 = 390 Ω	12.5			MHz
t_{PD1}	Clock to Q			20	30	ns
t_{PD2}	Clock to CO			55	80	ns
t_{PZX}	Output enable delay			35	45	ns
t_{PXZ}	Output disable delay			35	45	ns

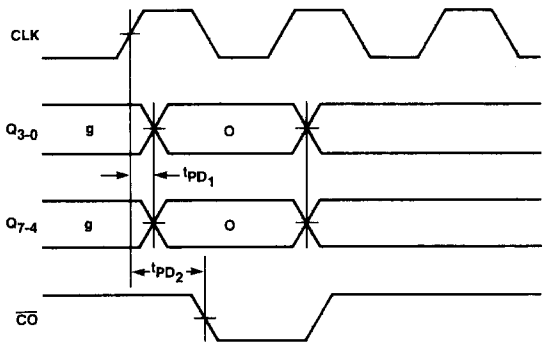
Standard Test Load



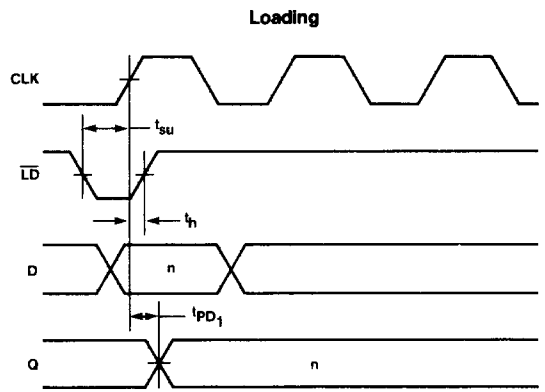
Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

7

Output Timing



Input Timing



Application: LED Displays

The Event Counter can be implemented using the 2-Digit BCD Counters. The 2-Digit BCD Counters control the display for three pairs of LED displays. The 2-Digit BCD Counters count the events.

The displays are controlled by the output enable. These counters display the count in 10s, 100s and 1000s respectively. These simply count the occurrence of an external event.

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