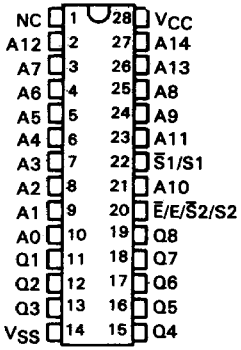
JUNE 1983 – REVISED NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down

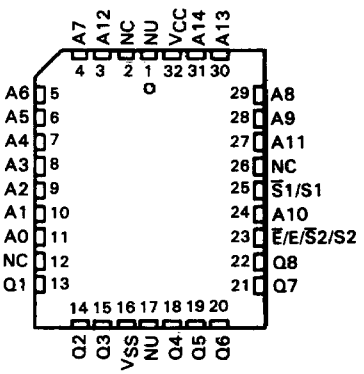
TMS47256-20	200 ns
TMS47256-25	250 ns
TMS47256-30	300 ns

- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW
- Pin Compatible with 27256 and 27C256 Type EPROMs

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 22 (dual-in-line package) and pins 23 and 25 (chip carrier) are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of $\overline{E}$ and $\overline{S}$ pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package designed for surface mount applications using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$/E/$\overline{S}$2/S2	Chip Enable/Power Down or Chip Select
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
$\overline{S}$1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 is the most-significant bit of the word address.

chip select ($\overline{S}1$ or S1)

Pin 22 (dual-in-line package) and pin 25 (chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both pins 22 and 20 (dual-in-line package) and pins 23 and 25 (chip carrier) are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When the signal on either of these pins is not active, all eight outputs are in a high-impedance state.

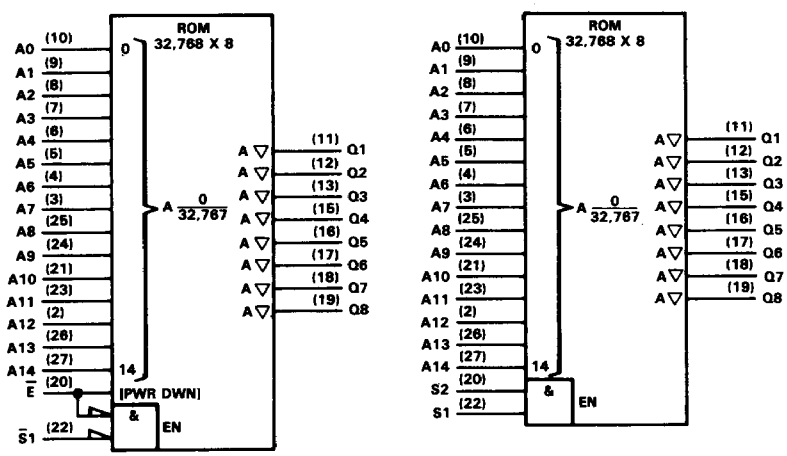
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 (dual-in-line package) and pin 23 (chip carrier) can be programmed during mask fabrication to be a chip-enable/power down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22 for the dual-in-line package and pin 23 is functionally identical to pin 25 for the chip carrier.

data out (Q1-Q8)

The eight outputs must be enabled by the $\overline{E}$ and $\overline{S}$ pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

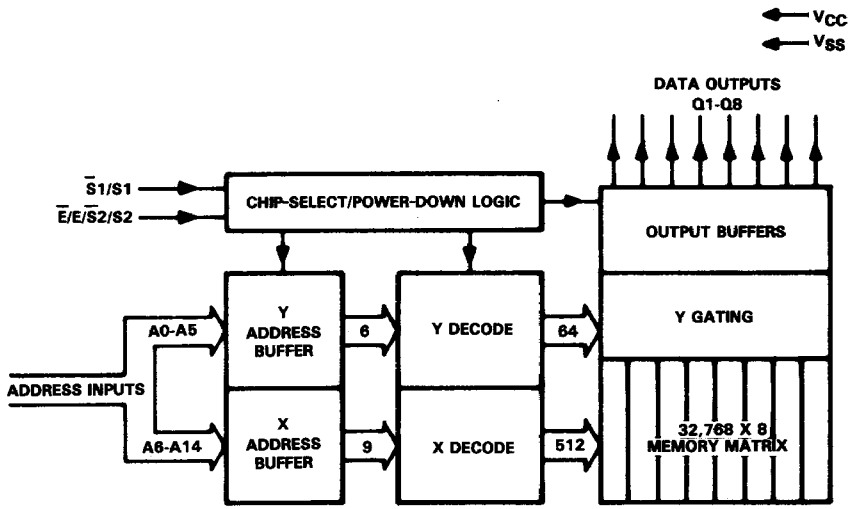
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 22 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a secondary chip select (S2 or $\overline{S}2$) or a chip enable/power down (E or $\overline{E}$). The pin numbers shown are for the 28-pin dual-in-line package.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . -0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . -1 V to 7 V
Applied input voltage (see Note 1) . . . . . -1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	-1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (see Figure 1)†

PARAMETER		TMS47256-20		TMS47256-25		TMS47256-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(AD)}$	Access time from address		200		250		300	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

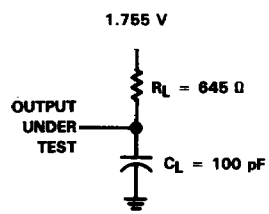
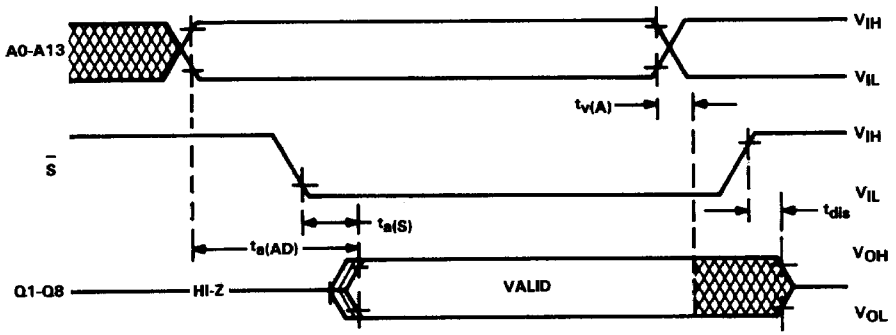


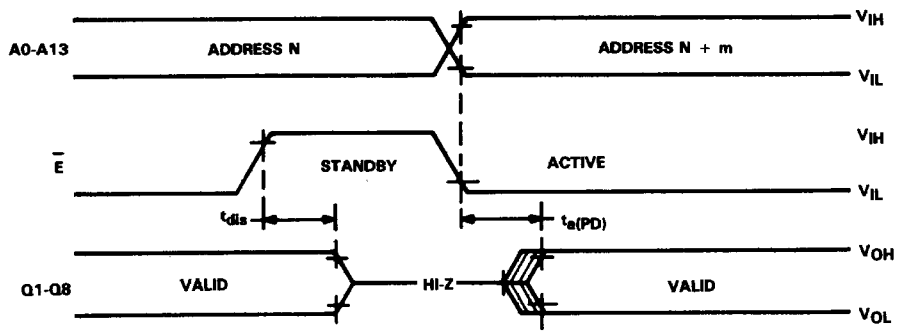
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47256 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number from 00 and FF. Q1 is considered the least-significant bit and Q8 is the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

N PACKAGE: PIN 20 _____ PIN 22 _____ PD/CS _____

FM PACKAGE: PIN 23 _____ PIN 25_____ PD/CS _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001