This version: Apr. 1999

# OKI Semiconductor

# MSM514102D/DL

**4,194,304-Word × 1-Bit DYNAMIC RAM : STATIC COLUMN MODE TYPE**

## DESCRIPTION

The MSM514102D/DL is a 4,194,304-word × 1-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM514102D/DL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM514102D/DL is available in a 26/20-pin plastic SOJ, 20-pin plastic ZIP, or 26/20-pin plastic TSOP. The MSM514102DL (the low-power version) is specially designed for lower-power applications.

## FEATURES

- 4,194,304-word × 1-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (L-version)
- Static Column mode, read modify write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Package options:

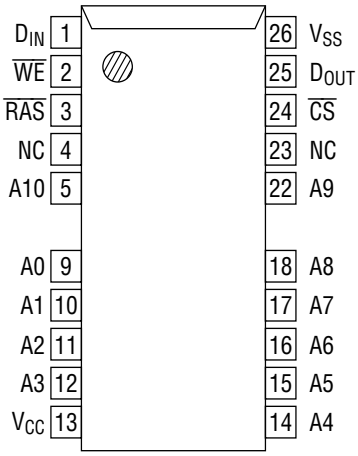
| | | |
|---|---|---|
| 26/20-pin 300 mil plastic SOJ | (SOJ26/20-P-300-1.27) | (Product : MSM514102D/DL-xxSJ) |
| 20-pin 400 mil plastic ZIP | (ZIP20-P-400-1.27) | (Product : MSM514102D/DL-xxZS) |
| 26/20-pin 300 mil plastic TSOP | (TSOPII26/20-P-300-1.27-K) | (Product : MSM514102D/DL-xxTS-K) |

xx indicates speed rank.

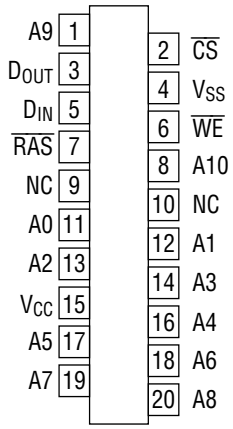
## PRODUCT FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation | |
|---|---|---|---|---|---|---|
| | $t_{RAC}$ | $t_{AA}$ | $t_{CAC}$ | | Operating (Max.) | Standby (Max.) |
| MSM514102D/DL-60 | 60 ns | 30 ns | 15 ns | 110 ns | 495 mW | 5.5 mW/ 1.1 mW (L-version) |
| MSM514102D/DL-70 | 70 ns | 35 ns | 20 ns | 130 ns | 440 mW | |
| MSM514102D/DL-80 | 80 ns | 40 ns | 20 ns | 150 ns | 385 mW | |

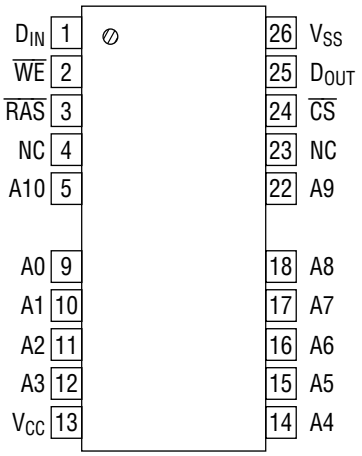
## PIN CONFIGURATION (TOP VIEW)




26/20-Pin Plastic SOJ



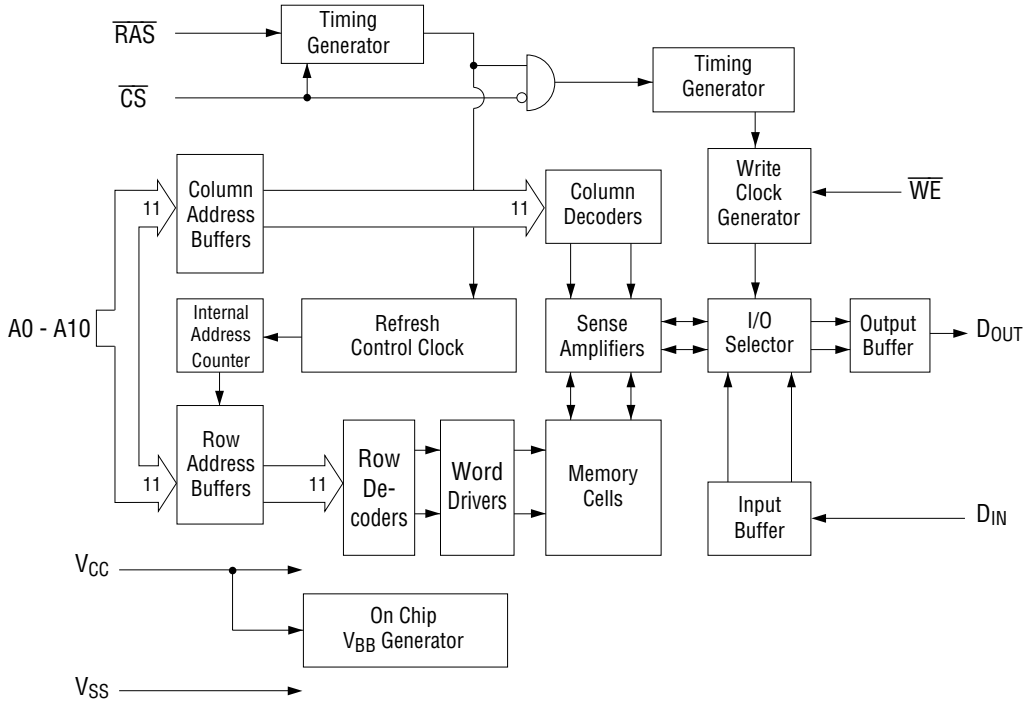

20-Pin Plastic ZIP




26/20-Pin Plastic TSOP
(K Type)

| Pin Name | Function |
|---|---|
| A0 - A10 | Address Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CS}$ | Chip Select Input |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power Supply (5 V) |
| $V_{SS}$ | Ground (0 V) |
| NC | No Connection |

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$ | –1.0 to 7.0 | V |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_D$* | 1 | W |
| Operating Temperature | $T_{opr}$ | 0 to 70 | °C |
| Storage Temperature | $T_{stg}$ | –55 to 150 | °C |

*: Ta = 25°C

### Recommended Operating Conditions

(Ta = 0°C to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | — | 6.5 | V |
| Input Low Voltage | $V_{IL}$ | –1.0 | — | 0.8 | V |

### Capacitance

($V_{CC}$ = 5 V ±10%, Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance (A0 - A10, $D_{IN}$) | $C_{IN1}$ | — | 6 | pF |
| Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$) | $C_{IN2}$ | — | 7 | pF |
| Output Capacitance ($D_{OUT}$) | $C_{OUT}$ | — | 7 | pF |

## DC Characteristics

($V_{CC}$ = 5 V ±10%, Ta = 0°C to 70°C)

| Parameter | Symbol | Condition | MSM514102 D/DL-60 | | MSM514102 D/DL-70 | | MSM514102 D/DL-80 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –5.0 mA | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.2 mA | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | $I_{LI}$ | 0 V ≤ $V_I$ ≤ 6.5 V; All other pins not under test = 0 V | –10 | 10 | –10 | 10 | –10 | 10 | µA | |
| Output Leakage Current | $I_{LO}$ | $D_{OUT}$ disable 0 V ≤ $V_O$ ≤ 5.5 V | –10 | 10 | –10 | 10 | –10 | 10 | µA | |
| Average Power Supply Current (Operating) | $I_{CC1}$ | $\overline{RAS}$, $\overline{CS}$ cycling, $t_{RC}$ = Min. | — | 90 | — | 80 | — | 70 | mA | 1, 2 |
| Power Supply Current (Standby) | $I_{CC2}$ | $\overline{RAS}$, $\overline{CS}$ = $V_{IH}$ | — | 2 | — | 2 | — | 2 | mA | 1 |
| | | $\overline{RAS}$, $\overline{CS}$ | — | 1 | — | 1 | — | 1 | | |
| | | ≥ $V_{CC}$ –0.2 V | — | 200 | — | 200 | — | 200 | µA | 1, 5 |
| Average Power Supply Current ($\overline{RAS}$-only Refresh) | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CS}$ = $V_{IH}$, $t_{RC}$ = Min. | — | 90 | — | 80 | — | 70 | mA | 1, 2 |
| Power Supply Current (Standby) | $I_{CC5}$ | $\overline{RAS}$ = $V_{IH}$, $\overline{CS}$ = $V_{IL}$, $D_{OUT}$ = enable | — | 5 | — | 5 | — | 5 | mA | 1 |
| Average Power Supply Current ($\overline{CS}$ before $\overline{RAS}$ Refresh) | $I_{CC6}$ | $\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$ | — | 90 | — | 80 | — | 70 | mA | 1, 2 |
| Average Power Supply Current (Static Column Mode) | $I_{CC9}$ | $\overline{RAS}$ = $V_{IL}$, Address cycling, $t_{SC}$ = Min. | — | 80 | — | 70 | — | 60 | mA | 1, 3 |
| Average Power Supply Current (Battery Backup) | $I_{CC10}$ | $t_{RC}$ = 125 µs, $\overline{CS}$ before $\overline{RAS}$, $t_{RAS}$ ≤ 1 µs | — | 300 | — | 300 | — | 300 | µA | 1, 4, 5 |

Notes : 1. $I_{CC}$ Max. is specified as $I_{CC}$ for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. The address can be changed once or less while $\overline{CS}$ = $V_{IH}$.
4. $V_{CC}$ – 0.2 V ≤ $V_{IH}$ ≤ 6.5 V, –1.0 V ≤ $V_{IL}$ ≤ 0.2 V.
5. L-version.

## AC Characteristics (1/2)

($V_{CC}$ = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 12, 13

| Parameter | Symbol | MSM514102 D/DL-60 | | MSM514102 D/DL-70 | | MSM514102 D/DL-80 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 110 | — | 130 | — | 150 | — | ns | |
| Read Modify Write Cycle Time | $t_{RWC}$ | 130 | — | 155 | — | 175 | — | ns | |
| Static Column Mode Cycle Time | $t_{SC}$ | 35 | — | 40 | — | 45 | — | ns | |
| Static Column Mode Read Modify Write Cycle Time | $t_{SRWC}$ | 60 | — | 70 | — | 80 | — | ns | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 4, 5, 6 |
| Access Time from $\overline{CS}$ | $t_{CAC}$ | — | 15 | — | 20 | — | 20 | ns | 4, 5 |
| Access Time from Column Address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 4, 6, 7 |
| Access Time from Last Write | $t_{ALW}$ | — | 55 | — | 65 | — | 75 | ns | 4, 7 |
| Output Enable Time referenced to $\overline{WE}$ | $t_{OW}$ | — | 15 | — | 20 | — | 20 | ns | 4 |
| Output Low Impedance Time from $\overline{CS}$ | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| Data Output Hold Time referenced to Column Address | $t_{AOH}$ | 5 | — | 5 | — | 5 | — | ns | |
| Data Output Hold Time from $\overline{WE}$ | $t_{WOH}$ | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{CS}$ to Data Output Buffer Turn-off Delay Time | $t_{OFF}$ | 0 | 15 | 0 | 20 | 0 | 20 | ns | 8 |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | — | 16 | — | 16 | — | 16 | ms | |
| Refresh Period (L-version) | $t_{REF}$ | — | 128 | — | 128 | — | 128 | ms | |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | |
| $\overline{RAS}$ Pulse Width (Static Column Mode) | $t_{RASC}$ | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 15 | — | 20 | — | 20 | — | ns | |
| $\overline{CS}$ Precharge Time (Static Column Mode) | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{CS}$ Pulse Width | $t_{CS}$ | 15 | 10,000 | 20 | 10,000 | 20 | 10,000 | ns | |
| $\overline{CS}$ Hold Time | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | ns | |
| $\overline{CS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{RAS}$ to $\overline{CS}$ Delay Time | $t_{RCD}$ | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 6 |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | |
| Column Address Hold Time from $\overline{RAS}$ (Write Cycle) | $t_{AWR}$ | 50 | — | 55 | — | 60 | — | ns | |
| Column Address Hold Time from $\overline{RAS}$ | $t_{AR}$ | 75 | — | 85 | — | 95 | — | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Column Address Hold Time from $\overline{RAS}$ Precharge | $t_{AH}$ | 10 | — | 10 | — | 10 | — | ns | |

## AC Characteristics (2/2)

($V_{CC}$ = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 12, 13

| Parameter | Symbol | MSM514102 D/DL-60 | | MSM514102 D/DL-70 | | MSM514102 D/DL-80 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Column Address Hold Time | $t_{AHLW}$ | 55 | — | 65 | — | 75 | — | ns | |
| Last Write to Column Address Delay Time | $t_{LWAD}$ | 20 | 25 | 20 | 30 | 20 | 35 | ns | 7 |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Write Command Hold Time | $t_{WCH}$ | 10 | — | 10 | — | 15 | — | ns | |
| Write Command Hold Time from $\overline{RAS}$ | $t_{WCR}$ | 45 | — | 50 | — | 60 | — | ns | |
| Write Command Pulse Width | $t_{WP}$ | 10 | — | 10 | — | 15 | — | ns | |
| Write Invalid Time | $t_{WI}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write Command Hold Time ($D_{OUT}$ Disable) | $t_{WH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 15 | — | 20 | — | 20 | — | ns | |
| Write Command to $\overline{CS}$ Lead Time | $t_{CWL}$ | 15 | — | 20 | — | 20 | — | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 11 |
| Data-in Hold Time | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | 11 |
| Data-in Hold Time from $\overline{RAS}$ | $t_{DHR}$ | 50 | — | 55 | — | 60 | — | ns | |
| $\overline{CS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 15 | — | 20 | — | 20 | — | ns | 10 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 30 | — | 35 | — | 40 | — | ns | 10 |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 60 | — | 70 | — | 80 | — | ns | 10 |
| $\overline{CS}$ Active Delay Time from $\overline{RAS}$ Precharge | $t_{RPC}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$) | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{RAS}$ to $\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$) | $t_{CHR}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$) | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CS}$ before $\overline{RAS}$) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode) | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode) | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |

Notes:

1. A start-up delay of 200 μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume $t_T$ = 5 ns.

3. $V_{IH}$ (Min.) and $V_{IL}$ (Max.) are reference levels for measuring input timing signals. Transition times ($t_T$) are measured between $V_{IH}$ and $V_{IL}$.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the $t_{RCD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RCD}$ (Max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (Max.) limit, then the access time is controlled by $t_{CAC}$.

6. Operation within the $t_{RAD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RAD}$ (Max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (Max.) limit, then the access time is controlled by $t_{AA}$.

7. Operating within the $t_{LWAD}$ (Max.) limit ensures that $t_{ALW}$ (Max.) can be met. $t_{LWAD}$ (Max.) is specified as a reference point only. If $t_{LWAD}$ is greater than the specified $t_{LWAD}$ (Max.) limit, then the access time is controlled by $t_{AA}$.

8. $t_{OFF}$ (Max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

9. $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

10. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

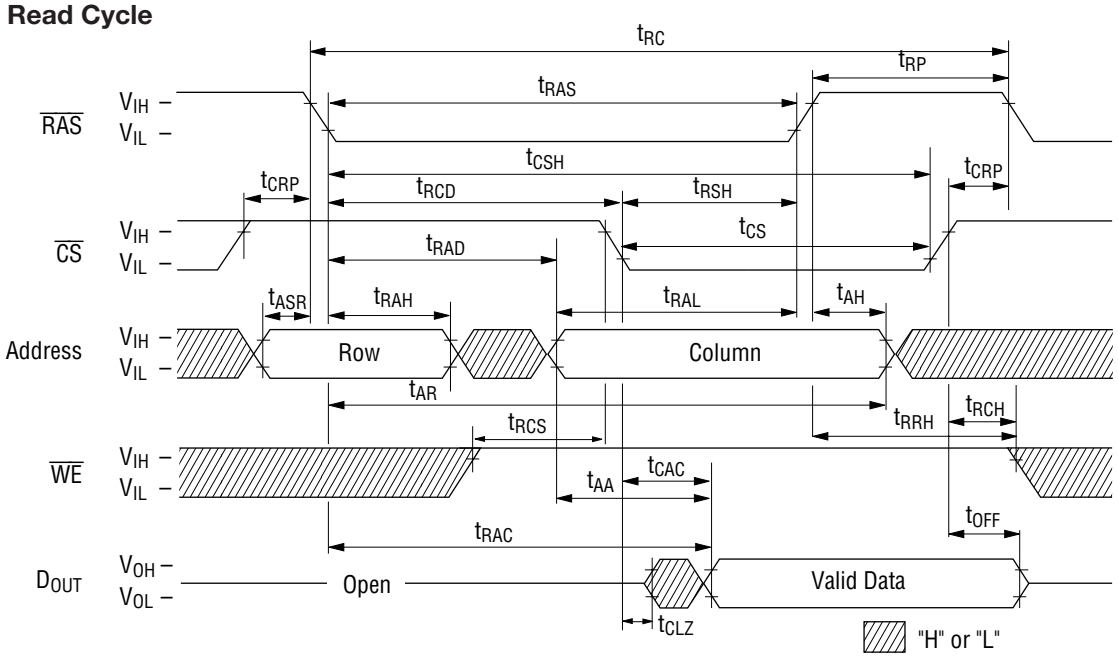
11. These parameters are referenced to the $\overline{CS}$ leading edge in an early write cycle, and to the $\overline{WE}$ leading edge in a read modify write cycle.

12. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
    The test mode specified in this data sheet is an 8-bit parallel test function. RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, the data output pin will indicate a low level.
    The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle.

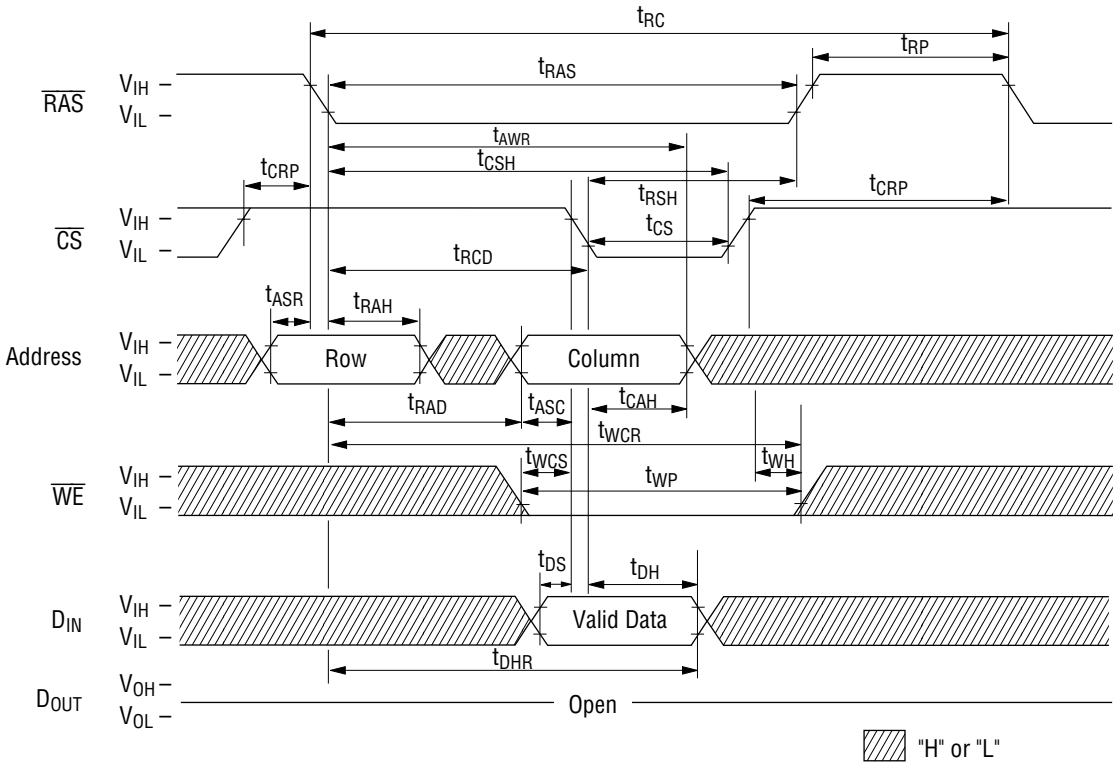
13. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

## TIMING WAVEFORM

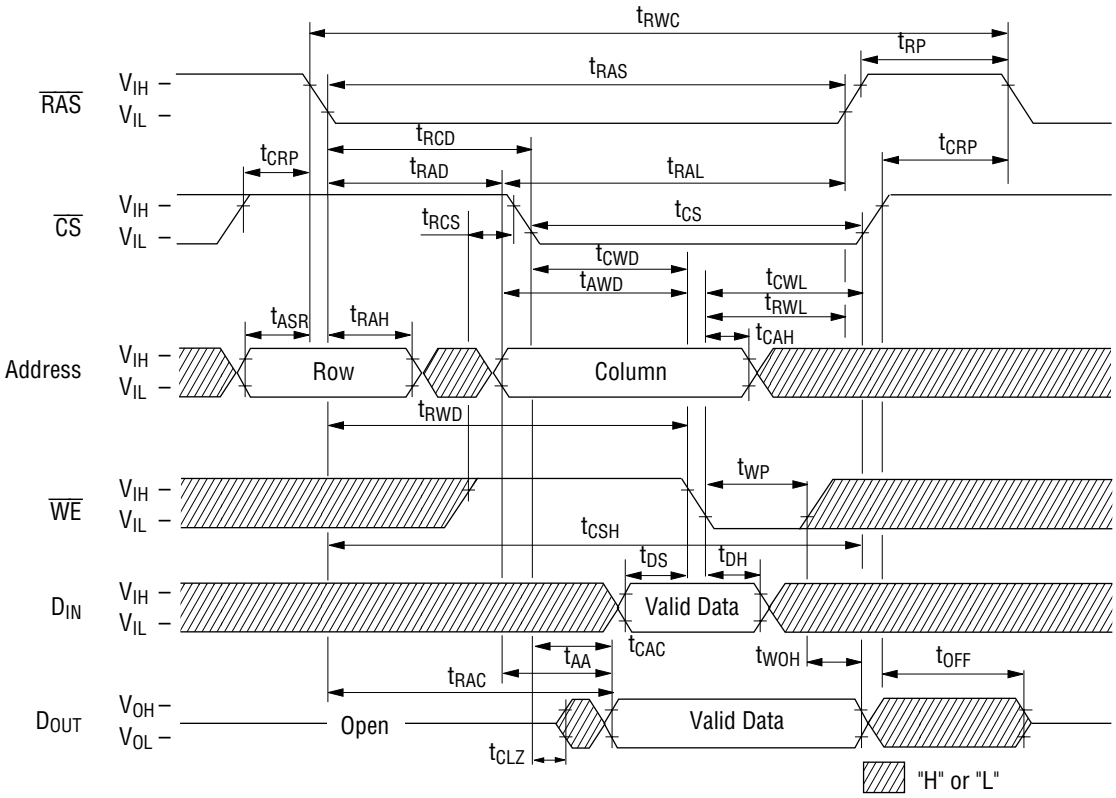
### Read Cycle



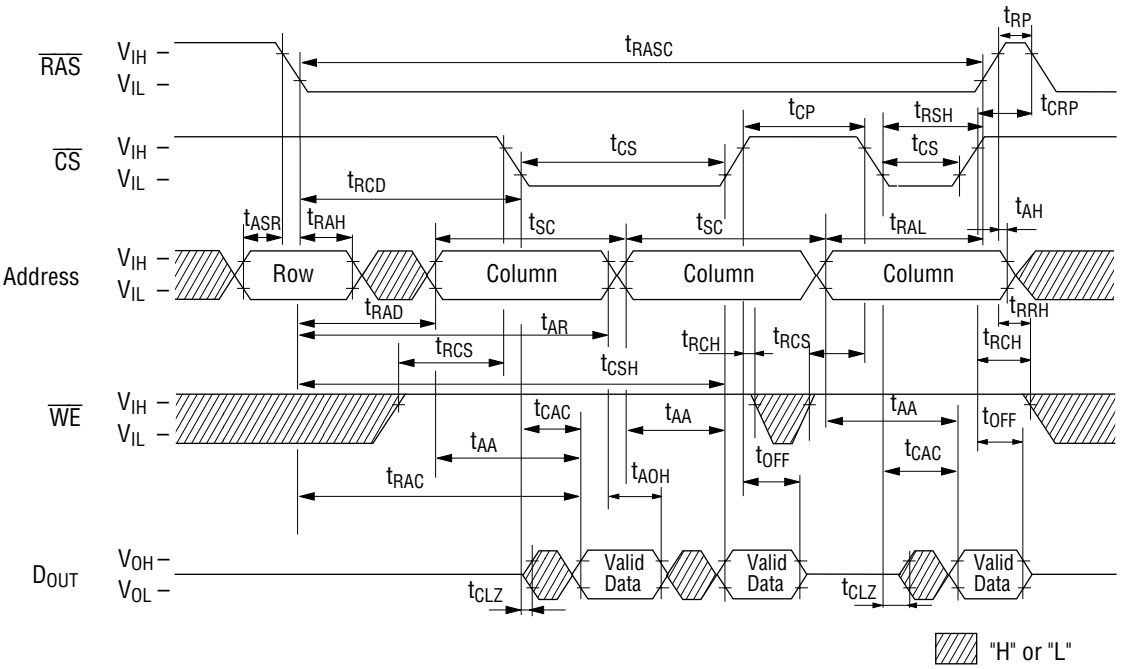

### Write Cycle (Early Write)



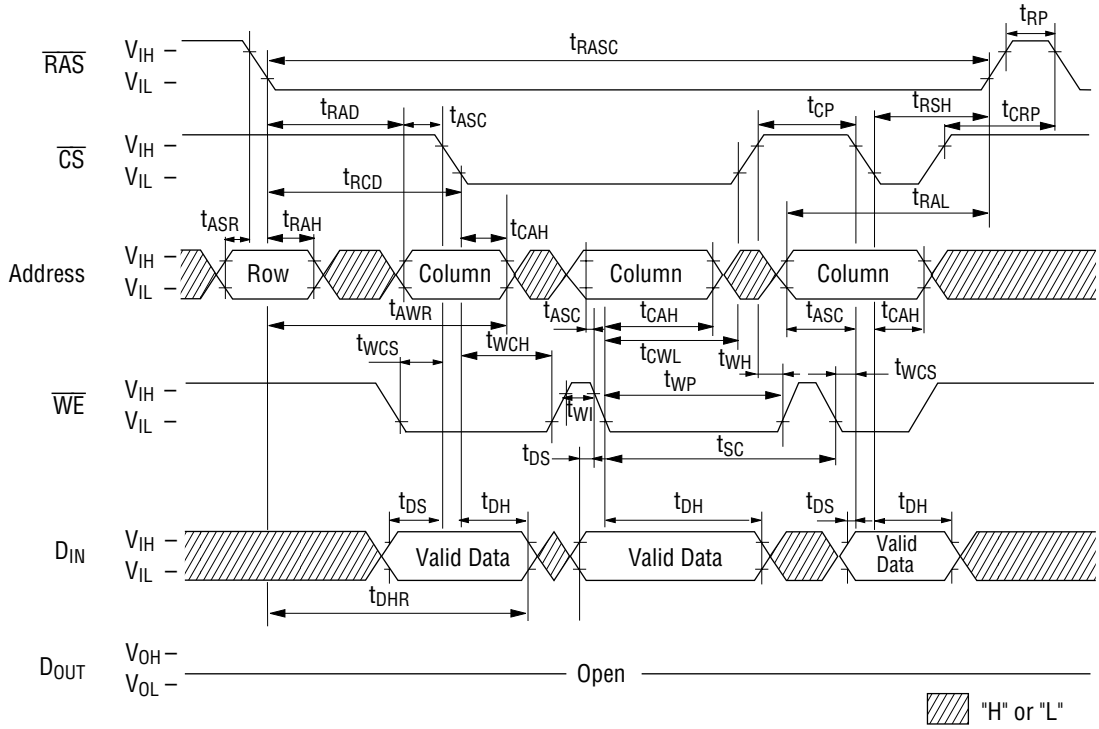
## Read Modify Write Cycle



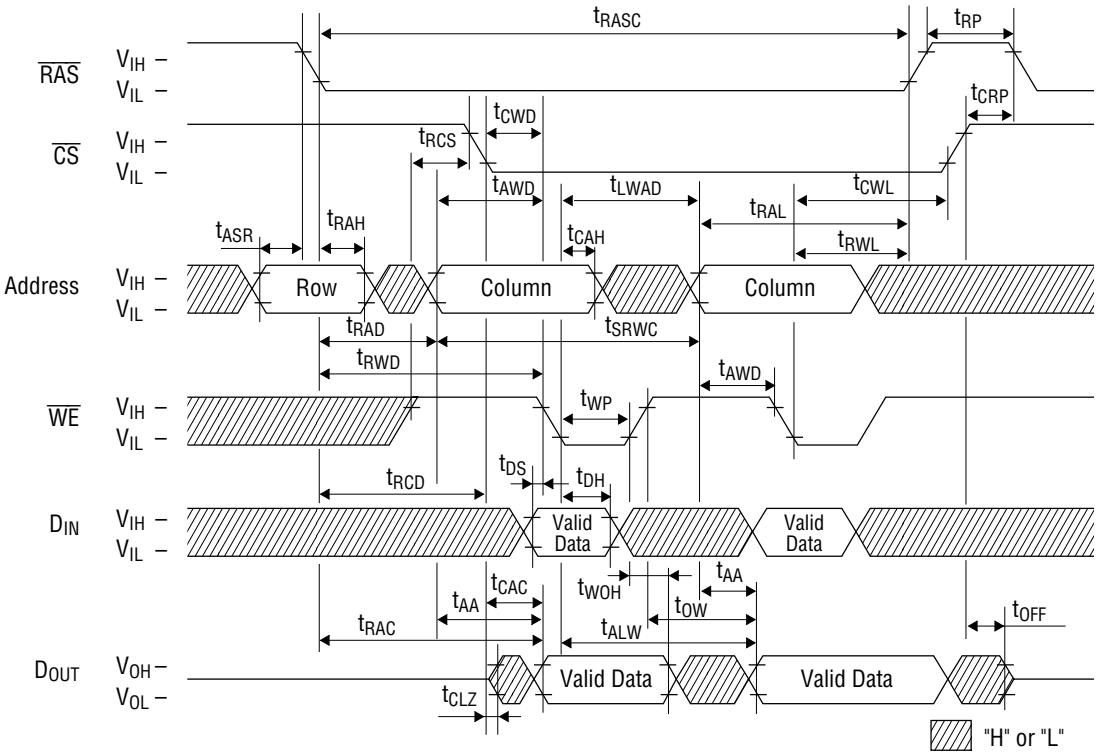

## Static Column Mode Read Cycle



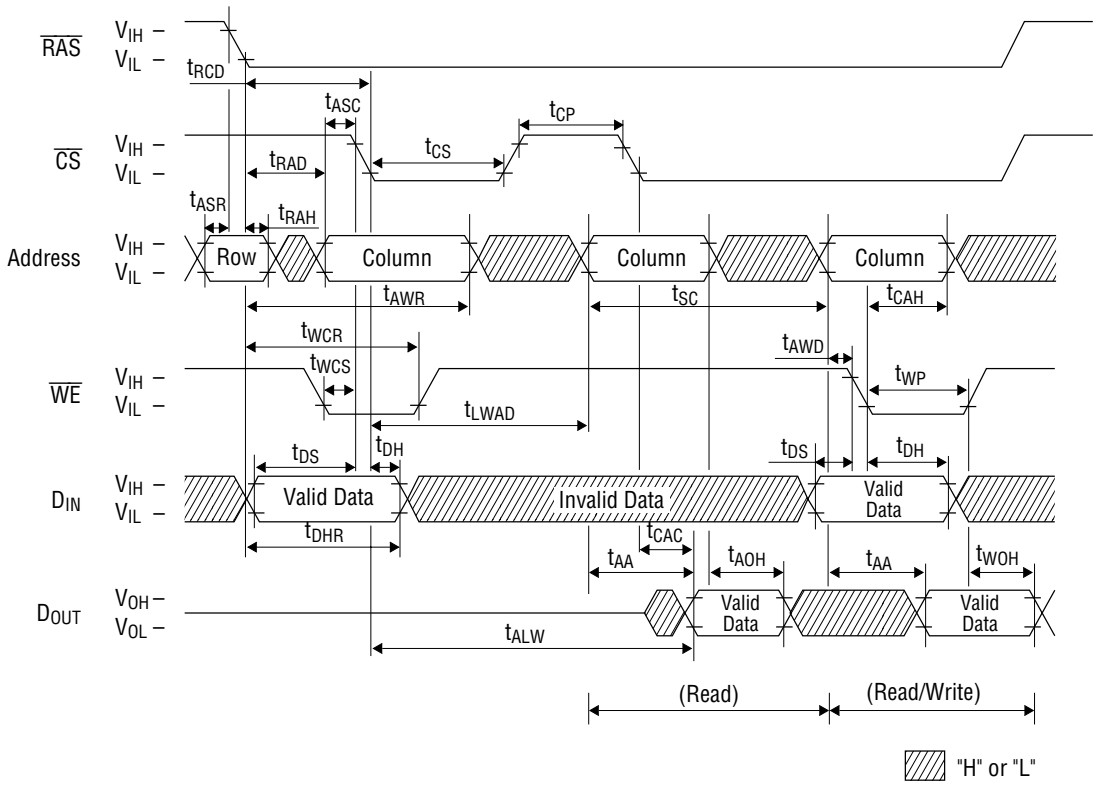
### Static Column Mode Write Cycle (Early Write)



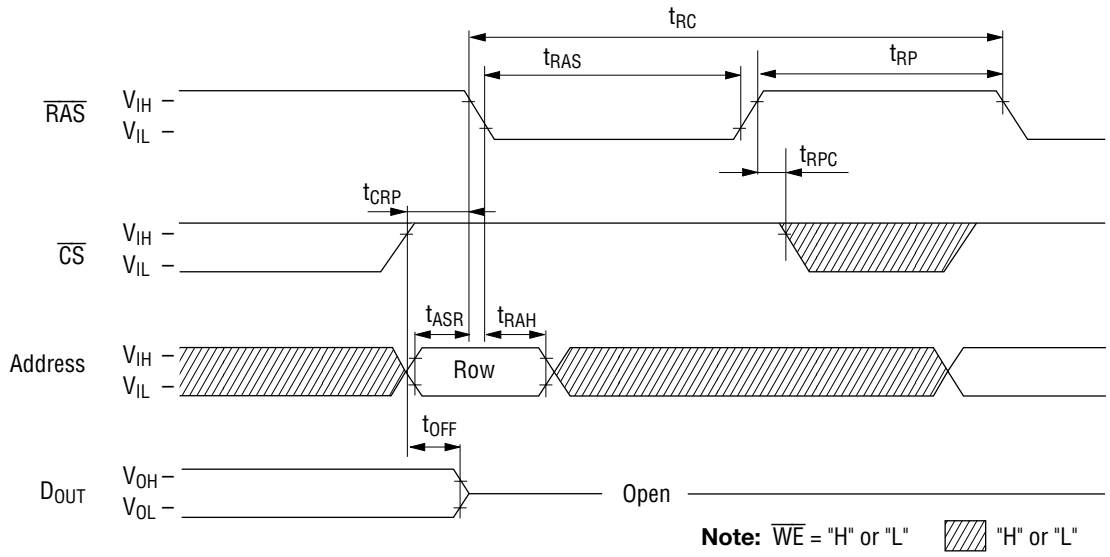

### Static Column Mode Read Modify Write Cycle



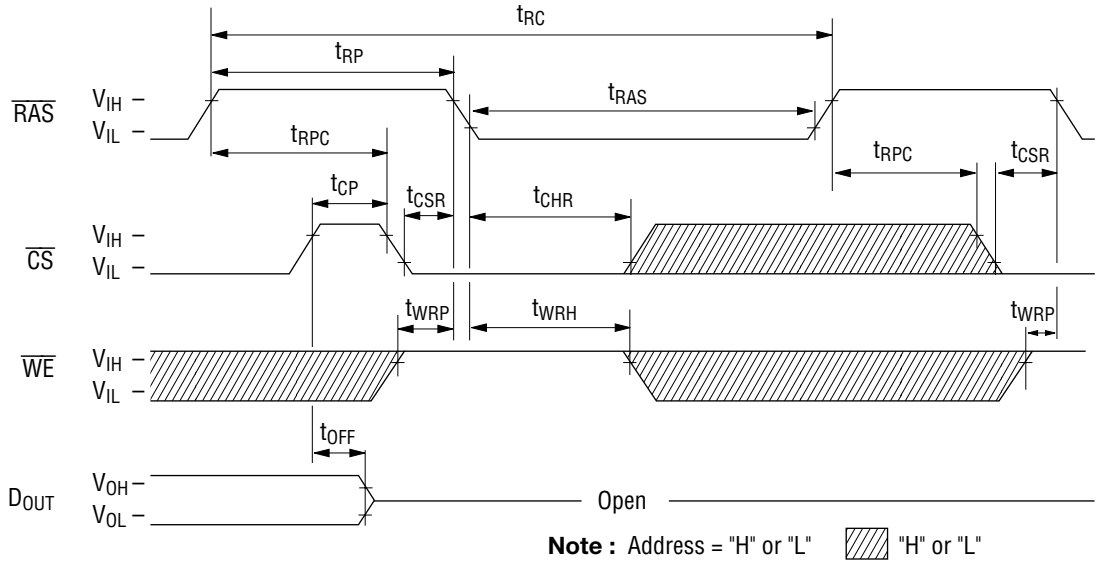
### Static Column Mode Read/Write Mixed Cycle



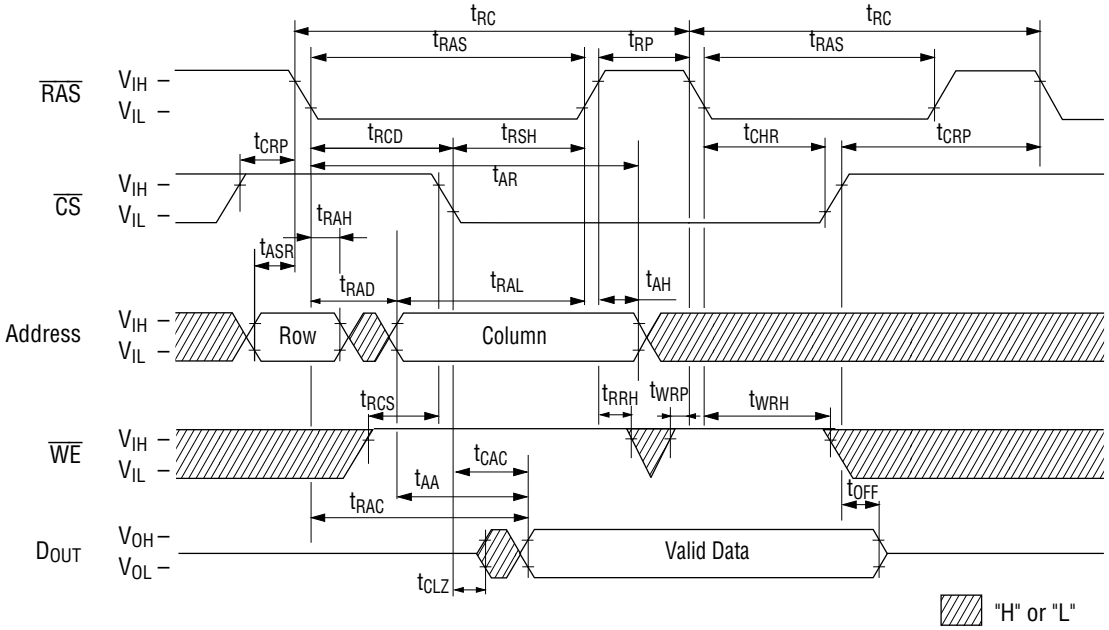

### RAS-Only Refresh Cycle



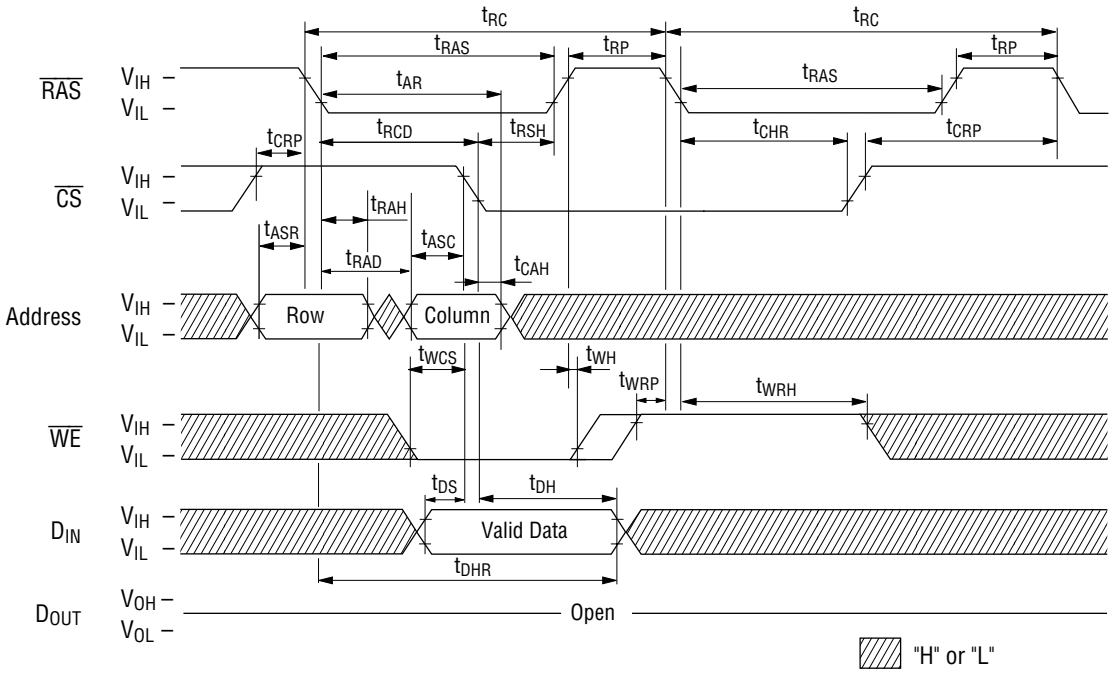
## $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle



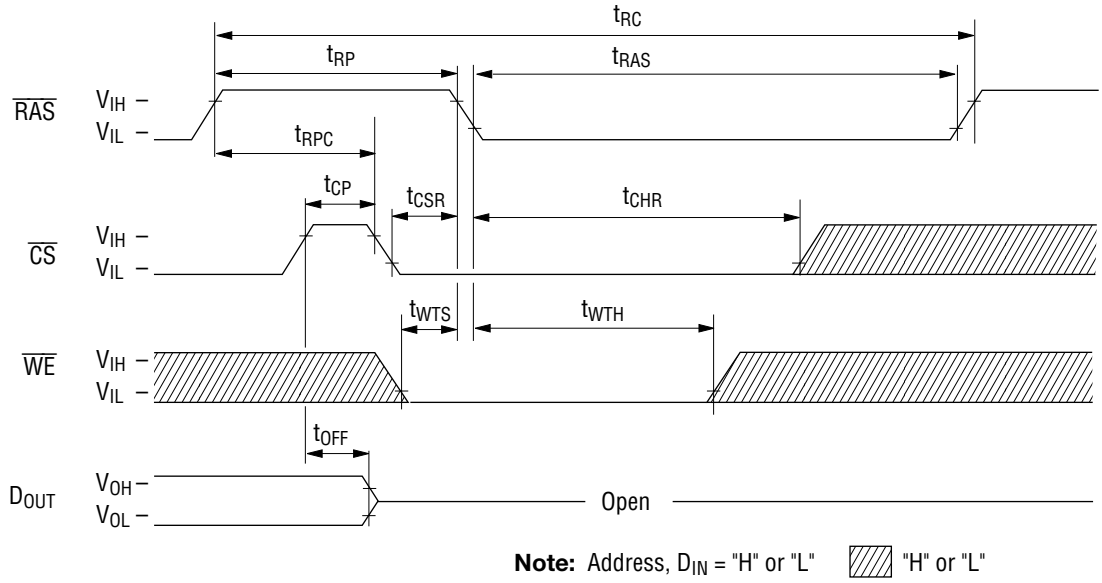

## Hidden Refresh Read Cycle



### Hidden Refresh Write Cycle



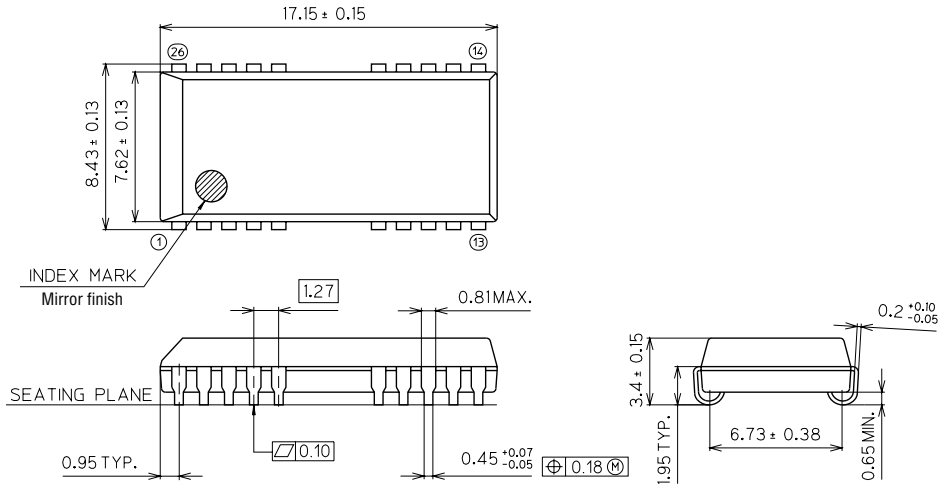

### Test Mode Initiate Cycle



## PACKAGE DIMENSIONS

(Unit : mm)

SOJ26/20-P-300-1.27



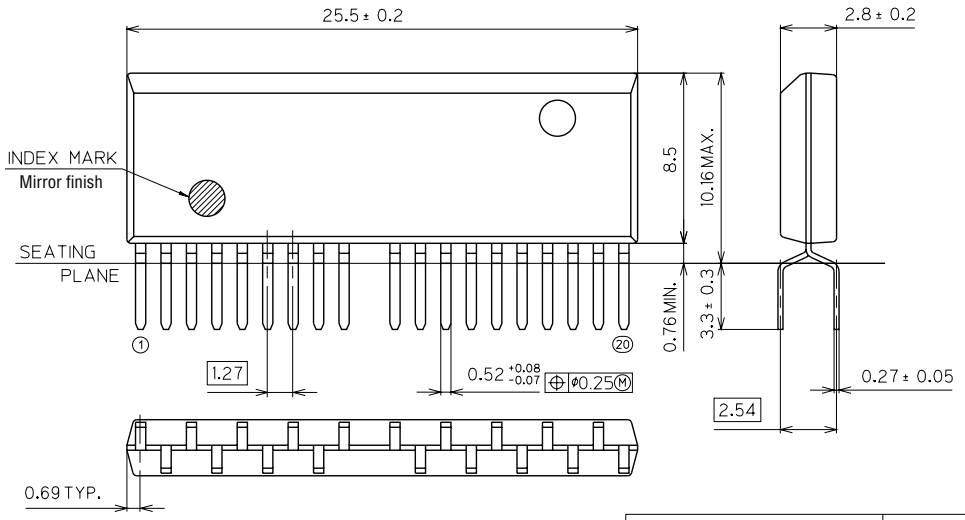

| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 0.80 TYP. |

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

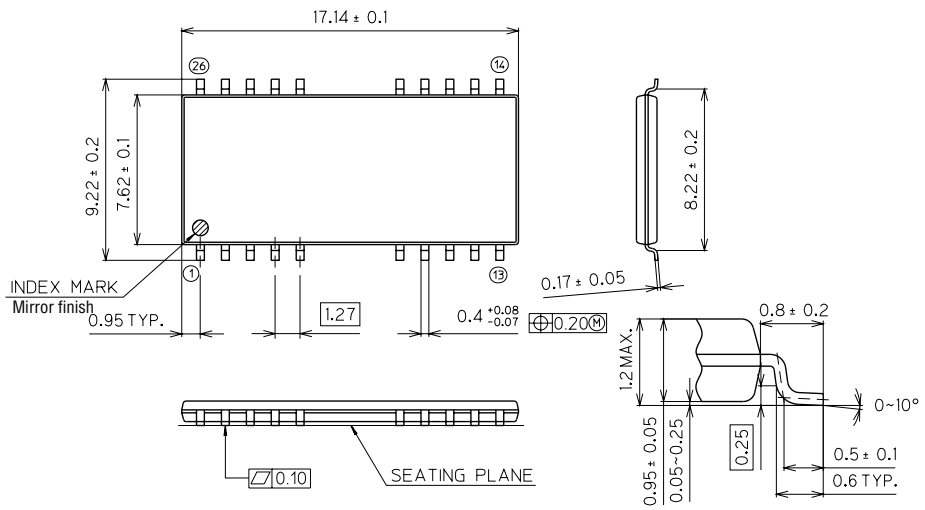
ZIP20-P-400-1.27




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.50 TYP. |

(Unit : mm)

TSOPII26/20-P-300-1.27-K




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 0.38 TYP. |

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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