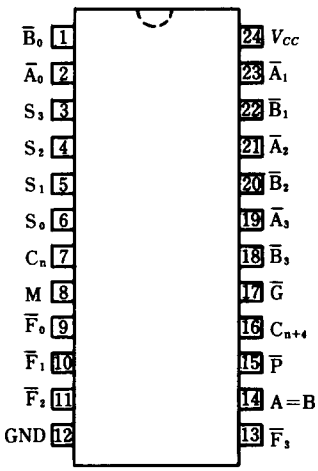
HD74AC181/HD74ACT181 ●4-Bit Arithmetic Logic Unit

Description

The HD74AC181/HD74ACT181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

- Outputs Source/Sink 24 mA
- HD74ACT181 has TTL-Compatible Inputs

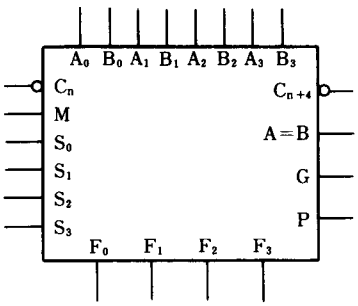
Pin Assignment



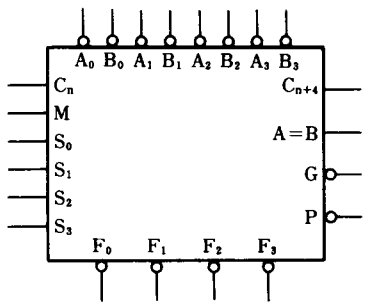
(Top View)

Logic Symbol

Active-HIGH Operands



Active-LOW Operands



Pin Names

$\overline{A}_0$—$\overline{A}_3$	A Operand Inputs (Active Low)
$\overline{B}_0$—$\overline{B}_3$	B Operand Inputs (Active Low)
S_0—S_3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}_0$—$\overline{F}_3$	Function Outputs (Active Low)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active Low)
$\overline{P}$	Carry Propagate Output (Active Low)
C_{n+4}	Carry Output

Truth Table

Mode Select Inputs				Active Low Operands & F_n Outputs		Active High Operands & F_n Outputs	
S_3	S_2	S_1	S_0	Logic (M=H)	Arithmetic** (M=L) (C_n=L)	Logic (M=H)	Arithmetic** (M=L) (C_n=H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{AB}$	A plus (A+B)	$\overline{A}+B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A+B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A+B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position
**arithmetic operations expressed in 2s complement notation
H = High Voltage Level
L = Low Voltage Level

Functional Description

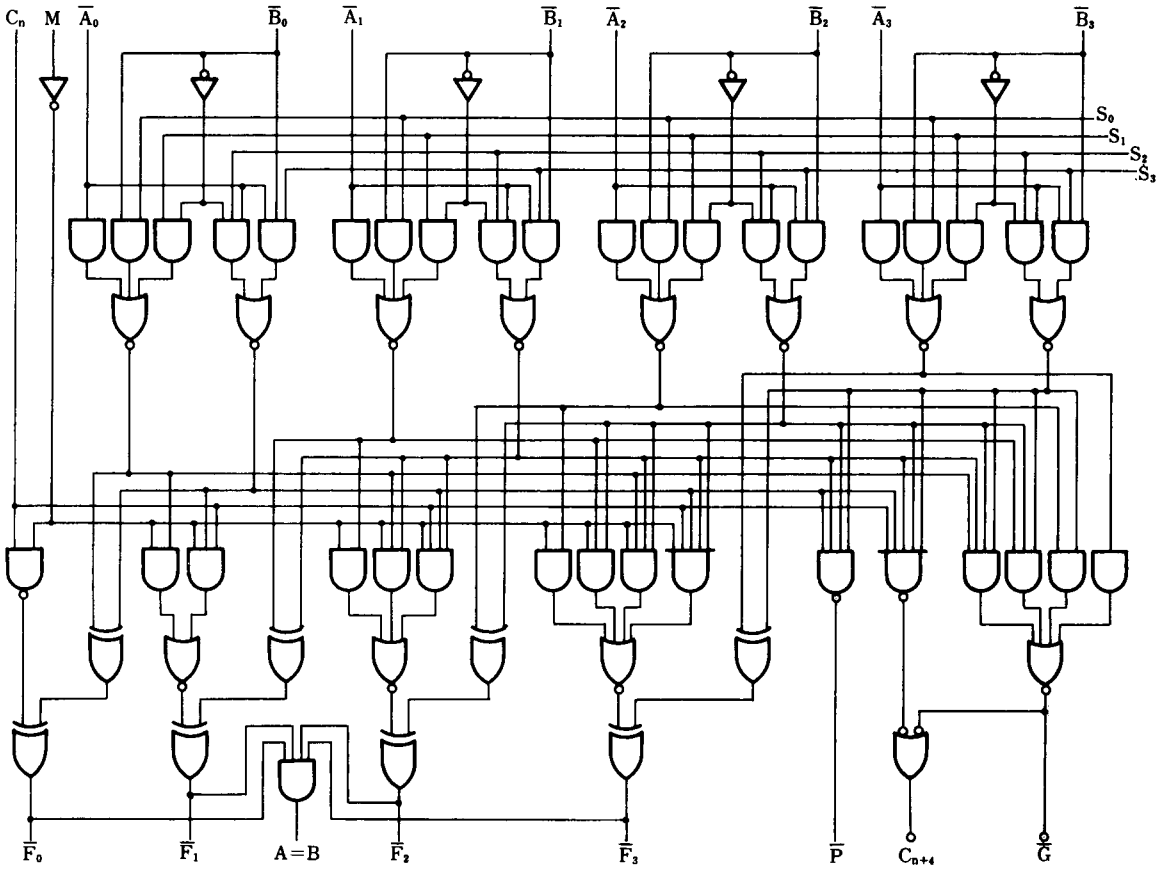
The HD74AC181/HD74ACT181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0—S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active High or Active Low operands. The Function Table lists these operations.

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the HD74AC181/HD74ACT181 can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four HD74AC181/HD74ACT181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open drain and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active Low inputs producing active Low outputs or with active High inputs producing active High outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = 25°C
I_{CCT}	Maximum Icc/Input (HD74ACT181)	1.5	mA	V_{IN} = Vcc − 2.1V Vcc = 5.5V Ta = Worst Case

AC Characteristics : HD74AC181

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Cn to C_{n+4}	3.3 5.0	1.0 1.0	11.0 8.5	14.0 11.0	1.0 1.0	15.5 12.0	ns
t_{PHL}	Propagation Delay Cn to C_{n+4}	3.3 5.0	1.0 1.0	10.5 8.0	13.5 10.5	1.0 1.0	16.0 11.5	ns
t_{PLH}	Propagation Delay A, B to C_{n+4} $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	16.5 13.5	20.0 16.0	1.0 1.0	22.0 17.5	ns
t_{PHL}	Propagation Delay A, B to C_{n+4} $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	16.0 13.0	19.5 15.5	1.0 1.0	21.5 17.0	ns
t_{PLH}	Propagation Delay A, B to C_{n+4} $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	16.5 13.5	20.0 16.0	1.0 1.0	22.0 17.5	ns
t_{PHL}	Propagation Delay A, B to C_{n+4} $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	16.0 13.0	19.5 15.5	1.0 1.0	21.5 17.0	ns
t_{PLH}	Propagation Delay Cn to $\overline{F}$ $M = GND$	3.3 5.0	1.0 1.0	12.5 10.0	16.0 12.5	1.0 1.0	17.5 13.5	ns
t_{PHL}	Propagation Delay Cn to $\overline{F}$ $M = GND$	3.3 5.0	1.0 1.0	11.5 9.0	15.0 11.5	1.0 1.0	16.5 12.5	ns
t_{PLH}	Propagation Delay A, B to $\overline{G}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	13.5 11.0	17.0 13.5	1.0 1.0	19.0 15.0	ns
t_{PHL}	Propagation Delay A, B to $\overline{G}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	13.0 10.5	16.5 13.0	1.0 1.0	18.5 14.5	ns
t_{PLH}	Propagation Delay A, B to $\overline{G}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	13.5 11.0	17.0 13.5	1.0 1.0	19.0 15.0	ns
t_{PHL}	Propagation Delay A, B to $\overline{G}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	13.0 10.5	16.5 13.0	1.0 1.0	18.5 14.5	ns
t_{PLH}	Propagation Delay A, B to $\overline{P}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	12.5 10.0	15.5 12.5	1.0 1.0	17.0 13.5	ns
t_{PHL}	Propagation Delay A, B to $\overline{P}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	12.0 9.5	15.0 12.0	1.0 1.0	16.5 13.0	ns
t_{PLH}	Propagation Delay A, B to $\overline{P}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	12.5 10.0	15.5 12.5	1.0 1.0	17.0 13.5	ns
t_{PHL}	Propagation Delay A, B to $\overline{P}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	12.0 9.5	15.0 12.0	1.0 1.0	16.5 13.0	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	18.5 15.0	22.5 18.0	1.0 1.0	25.0 20.0	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = S_1 = S_2 = GND$, $S_0 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	17.5 14.0	21.5 17.0	1.0 1.0	24.0 19.0	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	18.5 15.0	22.5 18.0	1.0 1.0	25.0 20.0	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	17.5 14.0	21.5 17.0	1.0 1.0	24.0 19.0	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = V_{CC}$	3.3 5.0	1.0 1.0	16.5 13.5	20.0 16.0	1.0 1.0	22.0 17.5	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $M = V_{CC}$	3.3 5.0	1.0 1.0	15.5 12.5	19.0 15.0	1.0 1.0	21.0 16.5	ns
t_{PLH}	Propagation Delay A, B to A = B $M = S_0 = S_1 = GND$, $S_2 = S_3 = V_{CC}$	3.3 5.0	1.0 1.0	20.5 16.5	25.0 19.5	1.0 1.0	27.5 21.5	ns
t_{PHL}	Propagation Delay A, B to A = B $M = S_0 = S_3 = GND$, $S_1 = S_2 = V_{CC}$	3.3 5.0	1.0 1.0	20.0 16.0	24.5 19.0	1.0 1.0	27.0 21.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Characteristics: HD74ACT181

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Cn to Cn+4	5.0	1.0	10.0	12.5	1.0	13.5	ns
t_{PHL}	Propagation Delay Cn to Cn+4	5.0	1.0	10.0	12.5	1.0	13.5	ns
t_{PLH}	Propagation Delay A, B to Cn+4 $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	15.5	18.5	1.0	20.0	ns
t_{PHL}	Propagation Delay A, B to Cn+4 $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	14.5	17.5	1.0	19.0	ns
t_{PLH}	Propagation Delay A, B to Cn+4 $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	15.5	18.5	1.0	20.0	ns
t_{PHL}	Propagation Delay A, B to Cn+4 $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	14.5	17.5	1.0	19.0	ns
t_{PLH}	Propagation Delay Cn to $\overline{F}$ $\overline{M}$ = GND	5.0	1.0	12.0	14.5	1.0	15.5	ns
t_{PHL}	Propagation Delay Cn to $\overline{F}$ $\overline{M}$ = GND	5.0	1.0	10.5	13.0	1.0	14.0	ns
t_{PLH}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{G}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	12.5	15.0	1.0	16.5	ns
t_{PHL}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{G}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	12.5	15.0	1.0	16.5	ns
t_{PLH}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{G}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	12.5	15.0	1.0	16.5	ns
t_{PHL}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{G}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	12.5	15.0	1.0	16.5	ns
t_{PLH}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{P}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	11.5	14.0	1.0	15.0	ns
t_{PHL}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{P}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	11.5	14.0	1.0	15.0	ns
t_{PLH}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{P}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	11.5	14.0	1.0	15.0	ns
t_{PHL}	Propagation Delay $\overline{A}$, $\overline{B}$ to $\overline{P}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	11.5	14.0	1.0	15.0	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	16.5	19.5	1.0	21.5	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = S_1 = S_2 = GND, S_0 = S_3 = Vcc	5.0	1.0	16.5	19.5	1.0	21.5	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	16.5	19.5	1.0	21.5	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	16.5	19.5	1.0	21.5	ns
t_{PLH}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = Vcc	5.0	1.0	15.0	18.0	1.0	19.5	ns
t_{PHL}	Propagation Delay $\overline{Ai}$, $\overline{Bi}$ to $\overline{Fi}$ $\overline{M}$ = Vcc	5.0	1.0	15.0	18.0	1.0	19.5	ns
t_{PLH}	Propagation Delay $\overline{A}$, $\overline{B}$ to A = B $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	18.0	21.5	1.0	23.5	ns
t_{PHL}	Propagation Delay $\overline{A}$, $\overline{B}$ to A = B $\overline{M}$ = S_0 = S_3 = GND, S_1 = S_2 = Vcc	5.0	1.0	18.0	21.5	1.0	23.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance		pF	Vcc = 5.5V
C_{PD}	Power Dissipation Capacitance		pF	Vcc = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

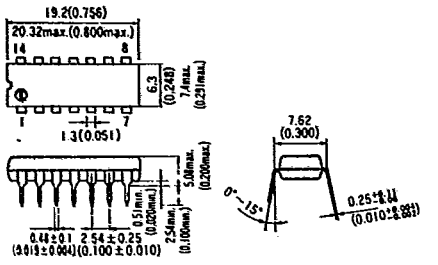
• Package code of Advanced CMOS Logic

HD74AC XXXX P

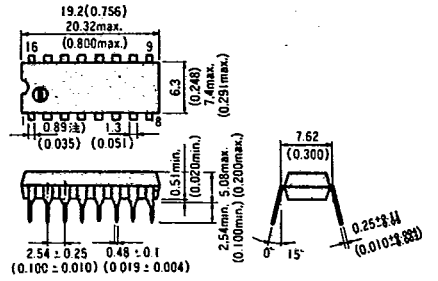
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

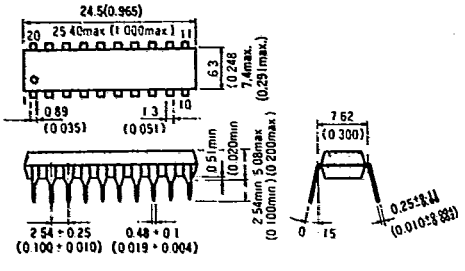
14 Pin type



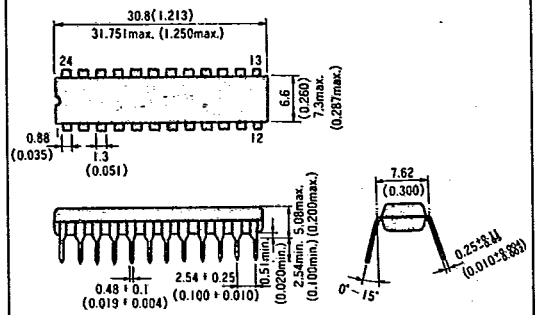
16 Pin type



20 Pin type



24 Pin type

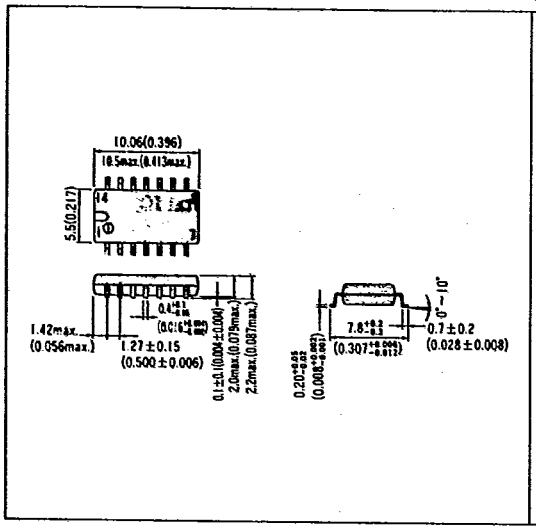


Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

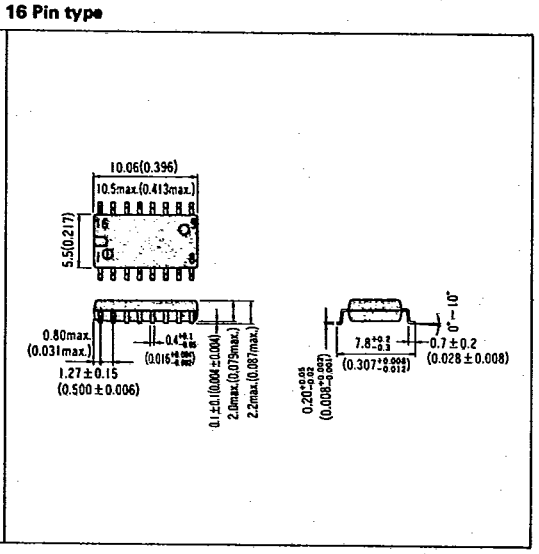
Package Information

Small Outline Package [Unit: mm (inch)]

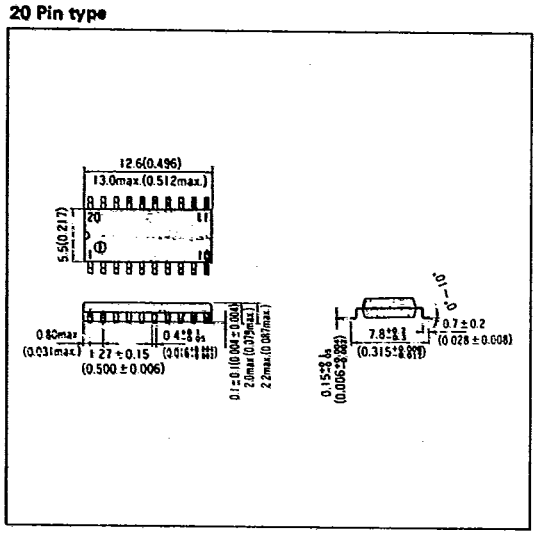
14 Pin type



16 Pin type



20 Pin type



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300