VANTIS
AN AMD COMPANY

ADVANCE INFORMATION **COM'L: -5/7/10/12** **IND: -7/10/12/15**

MACH5LV-128

MACH5LV-128/68-5/7/10/12 MACH5LV-128/104-5/7/10/12 MACH5LV-128/120-5/7/10/12

Fifth Generation MACH® Architecture

DISTINCTIVE CHARACTERISTICS

- **Pin-, function- and JEDEC-compatible with the MACH5-128**
- **Fifth generation MACH architecture**
  - 100% routable
  - Pin-out retention
  - Four power/speed options per block for maximum performance and lowest power
  - Synchronous and asynchronous clocking, including dual-edge clocking
  - Asynchronous product- or sum-term set or reset
  - Functions of up to 32 product terms
  - Fixed, predictable delays
- **High speed**
  - 5.5 ns t_{PD} Commercial, 7.5 ns t_{PD} Industrial
  - 125 MHz f_{CNT}
- **High density**
  - 128 macrocells
  - 2 MACH211SP-size segments
  - 16 output enables
  - 100-, 144-, and 160-pin package options
- **System performance capabilities**
  - In-system programmable across 0°C to +70°C
  - JTAG (IEEE 1149.1) boundary scan testing
  - PCI compliant (-5/-7/-10/-12 speed grades)
  - Safe for mixed supply voltage system design
  - Bus Friendly™ I/Os
  - Individual output slew rate control
  - Programmable security bit
- **Leading-edge 0.35-µm (L_{eff}) EECMOS process technology**
- **Supported by Vantis MACHXL® software**
  - Design entry ports to universal tools
  - Low-cost entry-level tool
  - Windows GUI interface
  - Auto device selection
  - Multiple device partitioning
- **Extensive software development support**
- **Third-party hardware programming support**

MACH 5 Family

Publication# 21550 Rev: A
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VANTIS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Device Junction Temperature . . . . . +130°C
Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V
DC Input Voltage . . . . . –0.5 V to 5.5 V
Static Discharge Voltage . . . . . 2000 V
Latchup Current (0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) LV Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C
Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Description		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 3)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 3)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–15		–180	mA
I_{CC}	Supply Current	All PAL Blocks Power Level 0 (PL0) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			180		mA
		All PAL Blocks Power Level 1 (PL1) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			115		mA
		All PAL Blocks Power Level 2 (PL2) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			70		mA
		All PAL Blocks Power Level 3 (PL3) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			35		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} = 2.0 V	3.3 V, 25°C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} = 2.0 V	3.3 V, 25°C, 1 MHz	10	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output	1	5.5	2	7.5	2	10	2	12	ns
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock	3		4		5		6		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		4.5		6		7		8	ns
t_{WLS}	Global Clock Low Width (Note 3)	2.5		3		4		5		ns
t_{WHS}	Global Clock High Width (Note 3)	2.5		3		4		5		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$	142		100		83		71		MHz
	Internal Feedback PAL Block Level	167		125		100		83.3		MHz
	No Feedback PAL Block Level	200		166.7		125		100		MHz
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level	3		4		5		6		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	3		4		5		6		ns
t_{COA}	Product Term Clock to Output		8		10		12		15	ns
t_{WLA}	Product Term Clock Width LOW	3		4		5		6		ns
t_{WHA}	Product Term Clock Width HIGH	3		4		5		6		ns
f_{MAXA}	External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$	90		71		58		47.6		MHz
	Internal Feedback, PAL Block Level	142		88		72		60		MHz
	No Feedback, PAL Block Level	167		125		100		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	3		4		5		6		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	3		4		5		6		ns
t_{GO}	Latch Gate to Output		9		10		11		12	ns

BASIC (all signals from within PAL block except global control signals) (Continued)

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GOL}	Latch Gate to Output through Transparent Latch		16		17		18		19	ns
t_{GCO}	Latch Gate to Combinatorial Output		16		17		18		19	ns
t_{IGS}	Latch Gate to Output Latch Setup	9		10		11		12		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	3		4		5		6		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		8		10		12		14	ns
t_{PRW}	Asynchronous Reset or Preset Width	3		4		5		6		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	5.5		7.5		8		9		ns
t_{EA}	Input, I/O, or Feedback to Output Enable	2	7.5	2	9.5	2	10	2	12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		7.5		9.5		10		12	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Edge	4		5		6		7		ns
t_{CEH}	Hold Time for Clock Enable After Last Enabled Clock Edge	3		4		5		6		ns
t_{RCEH}	Hold Time for Registered Clock Enable After Last Enabled Clock Edge	0		0		0		0		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Output Latch		9		10		12		15	ns
t_{PDIL}	Input, I/O, or Feedback to Output Through Transparent Latch		11		13		15		17	ns
t_{ICOG}	Input Register Global Clock to Combinatorial Output		11		13		14		16	ns
t_{ICOA}	Input Register Product Term Clock to Combinatorial Output		16		17		18		19	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		2		3		3		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	3		3		4		4		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	6		6		7		7		ns
t_{WICW}	Input Register Clock Width Low or High	3		4		5		6		ns
f_{MAXI}	Maximum Input Register Frequency	167		125		100		83.3		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	7.5		9.5		12		14		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	10		12.5		15		17		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	10		12.5		15		17		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time	8		10		10		12		ns
t_{SIL}	Input Latch Setup Time	2		2		3		3		ns
t_{HIL}	Input Latch Hold Time	6		6		7		7		ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		10		11		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12		14		16		18	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		1.5		1.5		2		2	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delays. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		4.5		5		6		6	ns

POWER, LOGIC, and SLEW

Parameter Symbol	Parameter Description	-5		-7		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		4		4		4		4	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		6		6		6		6	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		9		9		9		9	ns
t_{PT}	Product term cluster steering delay. This delay is added for each additional cluster of product terms used beyond the first cluster, to t_{PD}, t_{SS}, t_{SA}, t_{PDL}, t_{PDLL}, t_{SLL}, t_{SL}.		0.3		0.3		0.3		0.3	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COS}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) LV Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Description		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 µA	V_{CC} - 0.2			V
			I_{OH} = -3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 3)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 3)				-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)				-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		-15		-180	mA
I_{CC}	Supply Current	All PAL Blocks Power Level 0 (PL0) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			180		mA
		All PAL Blocks Power Level 1 (PL1) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			115		mA
		All PAL Blocks Power Level 2 (PL2) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			70		mA
		All PAL Blocks Power Level 3 (PL3) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 0 MHz, T_A = 25°C (Note 5)			35		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} = 2.0 V	3.3 V, 25°C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} = 2.0 V	3.3 V, 25°C, 1 MHz	10	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output	2	7.5	2	10	2	12	2	15	ns
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock	4		5		6		8		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		6		7		8		10	ns
t_{WLS}	Global Clock Low Width (Note 3)	3		4		5		6		ns
t_{WHS}	Global Clock High Width (Note 3)	3		4		5		6		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$	100		83		71		55		MHz
	Internal Feedback PAL Block Level	125		100		83.3		83.3		MHz
	No Feedback PAL Block Level	166.7		125		100		83.3		MHz
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level	4		5		6		7		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	4		5		6		7		ns
t_{COA}	Product Term Clock to Output		10		12		15		17	ns
t_{WLA}	Product Term Clock Width LOW	4		5		6		7		ns
t_{WHA}	Product Term Clock Width HIGH	4		5		6		7		ns
f_{MAXA}	External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$	71		58		47.6		42		MHz
	Internal Feedback, PAL Block Level	88		72		60		52		MHz
	No Feedback, PAL Block Level	125		100		83.3		71.4		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	4		5		6		7		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	4		5		6		7		ns
t_{GO}	Latch Gate to Output		10		11		12		13	ns
t_{GOL}	Latch Gate to Output through Transparent Latch		17		18		19		20	ns

BASIC (all signals from within PAL block except global control signals) (Continued)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GCO}	Latch Gate to Combinatorial Output		17		18		19		20	ns
t_{IGS}	Latch Gate to Output Latch Setup	10		11		12		13		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	4		5		6		7		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		10		12		14		16	ns
t_{PRW}	Asynchronous Reset or Preset Width	4		5		6		7		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	7.5		8		9		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable	2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		10		12		15	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Pulse	5		6		7		7		ns
t_{CEH}	Hold Time for Clock Enable Following Last Enabled Clock Pulse	4		5		6		6		ns
t_{RCEH}	Hold Time for Registered Clock Enable After Last Enabled Clock Edge	0		0		0		0		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Output Latch		10		12		15		20	ns
t_{PDIL}	Input, I/O, or Feedback to Output Through Transparent Input Latch		13		15		17		20	ns
t_{ICOG}	Input Register Global Clock to Combinatorial Output		13		14		16		18	ns
t_{ICOA}	Input Register Product Term Clock to Combinatorial Output		17		18		19		20	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		3		3		3		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	3		4		4		4		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	6		7		7		7		ns
t_{WICW}	Input Register Clock Width Low or High	4		5		6		7		ns
f_{MAXI}	Maximum Input Register Frequency	125		100		83.3		71.4		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	9.5		10		12		15		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	12.5		15		17		18		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	12 5		15		17		18		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time	10		10		12		15		ns
t_{SIL}	Input Latch Setup Time	2		3		3		3		ns
t_{HIL}	Input Latch Hold Time	6		7		7		7		ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	9		10		11		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		18		20	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		1.5		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		5		6		6		6	ns

POWER, LOGIC, and SLEW

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		4		4		4		4	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		6		6		6		6	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		9		9		9		9	ns
t_{PT}	Product term cluster steering delay. This delay is added for each additional cluster of product terms used beyond the first cluster, to t_{PD}, t_{SS}, t_{SA}, t_{PDL}, t_{PDLL}, t_{SLL}, t_{SL}.		0.3		0.3		0.3		0.3	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COS}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*