Am8151A

Graphics Color Palette (GCP)

FINAL

DISTINCTIVE CHARACTERISTICS

- A 256 x 8 color map and a video DAC on a single chip
- Pixel rates up to 200 MHz
- Full military range specifications
- Connects directly to singly or doubly terminated 50Ω or 75Ω RS-343A monitors
- No external compensation capacitors required
- Three Am8151As in parallel allow 256 displayable colors out of a palette of over 16 million colors
- 8-bit settling in 9.5 ns
- Glitch energy of 10 pV-sec
- Power consumption only 2/3 of the Am8151
- Plug-in replacement for Am8151

GENERAL DESCRIPTION

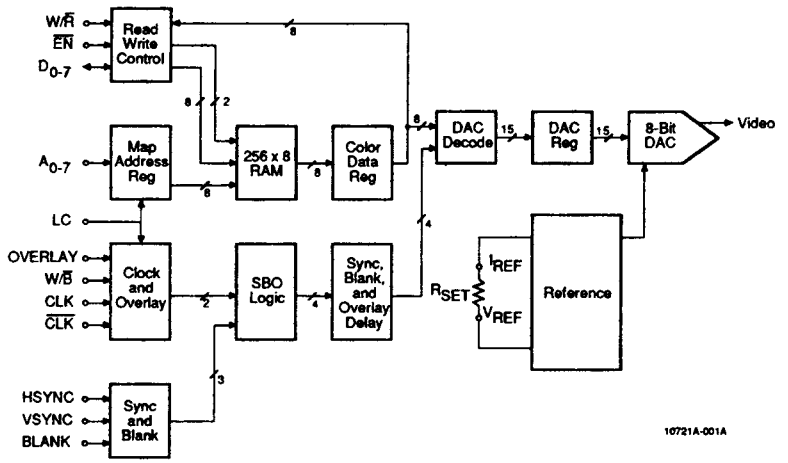
The Am8151A is a Graphics Color Palette providing a color lookup table and a video DAC for use in high-performance graphics systems. It is a low-power replacement for the original Am8151 Color Palette, featuring operation with video output loads from 25Ω to 75Ω. Logical structure of the Am8151A is identical to the Am8151 and is implemented with noise-free CML circuits to eliminate synchronous noise output from the video DAC. Three Am8151As connected in parallel provide simultaneous display of 256 colors from a palette of over 16 million colors.

The Am8151A has three levels of pipeline to allow a high pixel rate and to ease system timing requirements. The first level is prior to a 256 x 8 color lookup table in high-speed RAM. Eight bits of color address, $A_0 - A_7$ (ECL or TTL) are latched and used to select one of 256 intensities to be fed to the DAC. At the second level, the intensity selected is latched at the output of the RAM prior to being decoded to select which of the 15 current sources will be turned on. An additional high-speed register between the DAC Decoder and the DAC ensures that all DAC inputs switch simultaneously, thereby reducing the maximum duration of the glitch at the output of the DAC. This additional register adds a third level of pipeline to the pixel data path.

The color lookup table is stored in RAM and may therefore be read and writtten by a graphics processor. In addition to the 8 address lines, and 8 control lines, an 8-bit data path $D_0 - D_7$ (TTL), and two control signals $\overline{EN}$ (TTL) and $W/\overline{R}$ (TTL), are provided for this purpose.

The text capabilty of the AMD Alphanumeric Display Products or a generic overlay may be added with the OVERLAY (ECL or TTL) and $W/\overline{B}$ (ECL or TTL) inputs. A HIGH on the OVERLAY input overrides the color pixel data and drives the DAC output to peak white or reference black depending on the state of the $W/\overline{B}$ input. When three Am8151As are used in a system these pins can be connected to provide text or overlay capability in eight colors.

BLOCK DIAGRAM



TC004770

Publication # 10721 | Rev. A | Amendment /0
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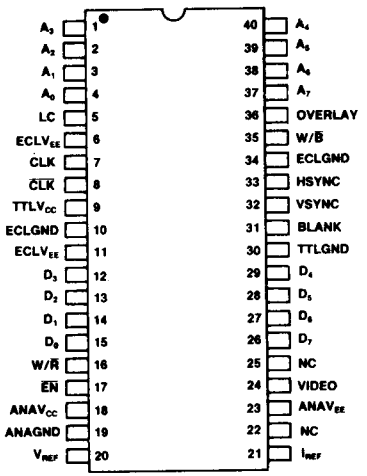
RELATED AMD PRODUCTS

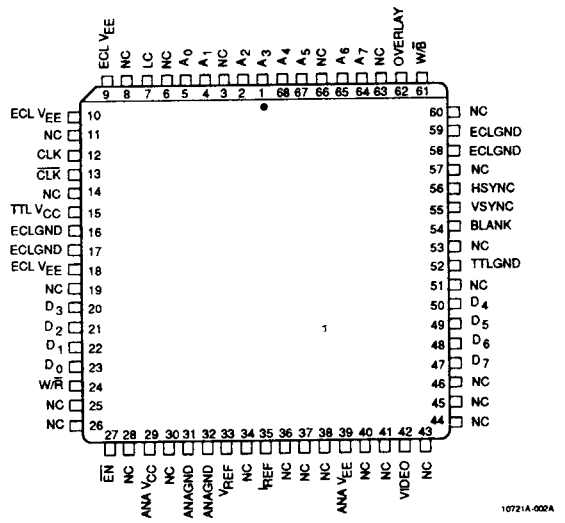
Part No.	Description
Am81C458	CMOS Color Palette
Am8172	Video Data Assembly FIFO (VDAF)
Am8177	Video Data Serializer
Am95C60	Quad Pixel Dataflow Manager

CONNECTION DIAGRAMS

Top View



CD005973



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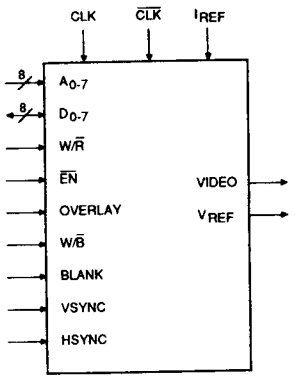
Note: Pin 1 is marked for orientation, NC = No Connection

LOGIC SYMBOL



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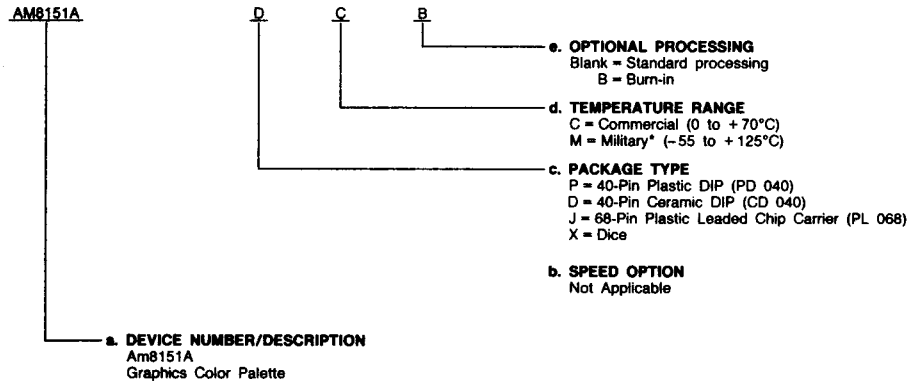
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM8151A	PC, DC, DCB, DM, DMB, JC, XC

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

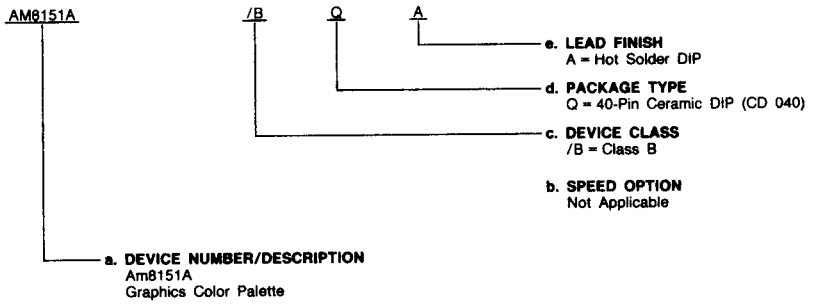
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM8151A	/BQA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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PIN DESCRIPTION

A_0–A_7 Address (Inputs; TTL/ECL)
These eight pins are used to address data stored in the color lookup table. The address on these pins is latched on the first rising CLK edge and decoded to select one of 256 intensities stored in the color lookup table. During a video refresh these pins should be connected to the color pixel data. During a color lookup table update these pins should be connected to the graphics processor's address bus. The logic compatability of these pins is determined by the LC pin.

D_0–D_7 Data (Inputs/Outputs; TTL)
These eight pins are used to write data in to the color lookup table or to read data out of the color lookup table. The MSB is D_7.

W/$\overline{R}$ Write/$\overline{Read}$ (Input; TTL)
The W/$\overline{R}$ controls the direction of color lookup table access by the system processor. When W/$\overline{R}$ is HIGH and $\overline{EN}$ is LOW, data is written in to the color lookup table. When W/$\overline{R}$ is LOW and $\overline{EN}$ is LOW, data is read from the color lookup table.

$\overline{EN}$ $\overline{Enable}$ (Input; TTL, Active LOW)
The $\overline{EN}$ pin is used to enable color lookup table data onto the data bus D_0–D_7 during a read operation and to enable a write into the color lookup table during a write operation. When $\overline{EN}$ is HIGH, the eight data lines D_0–D_7 are three-stated.

CLK, $\overline{CLK}$ Clock, $\overline{Clock}$ (Inputs; TTL/ECL)
CLK and $\overline{CLK}$ are the pixel clock inputs. In ECL mode these pins operate differentially. In TTL mode, $\overline{CLK}$ must be tied to ground. The clock is used internally to latch the address pins, data at the output of the color lookup table, and the decoded DAC inputs. The logic compatability of CLK is controlled by the LC pin.

OVERLAY Overlay (Input; TTL/ECL)
The OVERLAY pin, when active, overrides the color pixel data to force the DAC output to a peak white or reference black level. The level the DAC output is forced to is set by the W/$\overline{B}$ pin. The overlay signal is kept synchronized with the color pixel data inside the Am8151A by delaying the overlay signal the same number of clock cycles as the color pixel data. The logic compatibility of this pin is determined by the LC pin.

W/$\overline{B}$ White/$\overline{Black}$ (Input; TTL/ECL)
The W/$\overline{B}$ pin determines the level the OVERLAY pin will force the DAC output to. When W/$\overline{B}$ is HIGH, a HIGH on the OVERLAY pin will force the DAC output to a peak white level. When W/$\overline{B}$ is LOW, a HIGH on the OVERLAY pin will force the DAC output to a reference black level. The logic compatibility of this pin is determined by the LC pin.

BLANK Blanking (Input; TTL)
The BLANK pin, when active, overrides the color pixel and overlay data to force the DAC output to a "blacker than black" blank level. A "blacker than black" level is required during the monitor's horizontal and vertical retrace. The blank signal is kept synchronized with the pixel data inside the Am8151A by delaying the blank signal the same number of clock cycles as the pixel data.

VSYNC, HSYNC Vertical Sync Horizontal Sync (Input; TTL)
The HSYNC and VSYNC signals are internally x-ored to generate a composite sync signal. The composite sync signal, when HIGH, overrides the pixel, overlay, and blank signals to force the DAC output to a sync level. If both HSYNC and VSYNC are HIGH (composite sync is LOW) the DAC output is forced to a blank level. The composite signal is kept synchronized with the pixel data inside the Am8151A by delaying the sync signal the same number of clock cycles as the pixel data.

VIDEO Video (Output; Analog)
The VIDEO pin is the output of the DAC and is intended to directly drive monitor inputs which are singly or doubly terminated into 50 or 75Ω.

V_{REF} Voltage Reference (Output; Analog)
The V_{REF} pin provides a precision reference voltage for use in setting the full scale current of the DAC. The reference input current (I_{REF}) for the DAC, which determines the full scale current, may be generated from V_{REF} by connecting an external resistor from V_{REF} to I_{REF}. The reference resistor value may be calculated by the relation $R_{REF} = 28.44/IFS$.

I_{REF} Reference Current (Input; Analog)
A scaling current to the DAC should be provided at the I_{REF} pin. The full scale current of the DAC can be determined from the relation $IFS = 13.22\ I_{REF}$.

$TTLV_{CC}$ TTL-Positive Supply
Positive supply voltage for the TTL portions of the chip.

$ANAV_{CC}$ Analog Positive Supply
Positive supply voltage for the analog portions of the chip.

$ECLV_{EE}$ (2 pins) ECL Negative Supply
Negative supply voltage for the ECL portions of the chip.

LC Level Control (Power Suppy)
Level Control determines the logic compatability of the twelve TTL/ECL input pins. If LC is tied to V_{CC}, the logic levels are TTL. If LC is tied to ground, the logic levels are ECL.

$ANAV_{EE}$ Analog Negative Supply
Negative supply voltage for the analog portions of the chip.

TTLGND TTL Ground
Ground for the TTL portions of the chip.

ECLGND (2 pins) ECL Ground
Ground for the ECL portions of the chip.

ANAGND Analog Ground
Ground for the analog portions of the chip.

FUNCTIONAL DESCRIPTION

The Am8151A is a Graphics Color Palette (GCP) providing a color lookup table and a video DAC for use in high performance graphics systems. The Am8151A is pipelined with digital color pixel data, overlay, blank, and sync inputs entering the pipeline, and an analog signal exiting 3 CLK cycles later. The three levels of pipeline are prior to the 256 x 8 RAM color lookup table, the DAC decoder, and the 15 current sources to generate an analog signal.

Color Lookup Table

Eight lines of color pixel data are read through the pins $A_0 - A_7$ and latched into the Address Registers on the first rising edge of the CLK. $A_0 - A_7$ may be at either ECL or TTL logic levels. The LC pin is used to select the logic compatibility of these pins. These eight lines ($A_0 - A_7$) are used as an address for the color lookup table and are decoded to select one of the 256 intensities stored in the color lookup table. Each intensity stored is 8 bits wide, with 255 corresponding to reference white and 0 corresponding to reference black. On the next

rising CLK edge the intensity is latched into the color data registers to be decoded for the DAC. On a third rising CLK edge the decoded DAC inputs are latched and used to turn on or off the current sources making up the DAC.

Color Lookup Table Update

The color lookup table may be loaded and read back by the graphics processor. For this purpose 8 bidirectional data lines ($D_0 - D_7$) have been provided. D_7 is the Most Significant Bit (MSB) and D_0 is the Least Significant Bit (LSB) of data. In addition to the 8 data lines, 2 control lines are provided ($\overline{EN}$ and W/$\overline{R}$). $\overline{EN}$ is an active LOW input that selects the chip for both write and read operations. When $\overline{EN}$ is HIGH, the 8 bidirectional data lines are three-stated. W/$\overline{R}$ controls the direction of the operation. If this pin is LOW, color lookup table data is read from the table and placed on the data lines $D_0 - D_7$. If W/$\overline{R}$ is HIGH, data is read from the 8 data lines and written in to the color lookup table. For both the read and write operations the address of the data stored in the color lookup table is taken from the eight address lines ($A_0 - A_7$). Because both the address inputs and the outputs of the color lookup table are latched, the clock must be left running during an update. Time must be allowed for the address to be latched before beginning a write cycle and for the address and then data to be latched before ending a read cycle. To insure the update cycle does not interfere with the screen refresh, modifications to the color lookup table should occur while blank is active. The ten additional lines ($D_0 - D_7$, $\overline{EN}$, and W/$\overline{R}$) used for a color lookup table update are all TTL-compatible.

Overlay

Some graphics systems require a separate bit plane in addition to the color bit planes. An example of this might be separate hardware and a separate bit plane to handle text processing. The Am8151A provides two pins (OVERLAY and W/$\overline{B}$) which override the color pixel data to provide an additional video source. If OVERLAY is HIGH, the pixel data on $A_0 - A_7$ is overridden. W/$\overline{B}$ selects the intensity of the overlay. If W/$\overline{B}$ is HIGH, the DAC output will be at the Peak White level (10% brighter than Reference White. If W/$\overline{B}$ is LOW, the DAC output will be at the Reference Black level. OVERLAY and W/$\overline{B}$ may be at either TTL or ECL logic levels. The LC pin is used to select the logic compatibility of these pins. The OVERLAY and W/$\overline{B}$ signals are delayed the same number of clock cycles as the color pixel data before being fed into the DAC Decoder to keep overlay and color pixel data synchronized.

Blank

During horizontal and vertical retrace, pixel data should be ignored and the intensity output of the DAC should be driven to a "blacker than black" blank state. This is done by means of the BLANK input. BLANK is TTL-compatible and latched on the same clock as the pixel data. The BLANK signal is delayed the same number of clock cycles as the pixel data before being fed into the DAC Decoder to keep the BLANK signal and the pixel data synchronized. BLANK, when active, overrides the data and overlay inputs to drive the DAC output to the blank level.

Composite Sync

In some systems, the monitor control signals HSYNC and VSYNC are mixed with the Red, Green, and Blue signals. These control signals synchronize the monitor sweep oscillators to the R, G and B signal information. The Am8151A provides the necessary circuitry to mix these signals with the pixel information. Two inputs are provided, HSYNC and VSYNC, which are combined to generate the composite sync. These inputs are TTL-compatible and are latched with the same clock as the pixel data. Internally to the chip, HSYNC and VSYNC are XORed to generate a composite sync signal. The composite sync signal is generated in this manner to provide inverted HSYNC pulses during the much longer VSYNC pulse. This prevents the horizontal oscillator from losing synchronization during a vertical retrace and causes the horizontal oscillator to change phase by the width of HSYNC. The composite sync signal is delayed the same number of cycles as the pixel data and then, if active, overrides the data, OVERLAY, and BLANK signals to drive the output to the composite sync level.

Voltage Reference

The Am8151A provides an on-chip precision voltage supply between the V_{REF} and I_{REF} pins. A scaling current is generated at the I_{REF} input by connecting an external R_{SET} resistor from V_{REF} to I_{REF}. The SET value can be calculated from R_{SET} = 28.44/IFS, where IFS is the nominal Sync level output current. Nominal Reference Black output of −714 mV is obtained with R_{SET} = 1000 ohms and RT = 37.5 ohms. For these values, the Am8151A will have a Reference Black output level between −728 mV and −700 mV for operation over specified temperature range and ±10% supplies. The output drive current of the Am8151A has been increased to 9.7 mA to allow operation of three Am8151A's with 667-ohm resistors connected to their respective I_{REF} inputs for doubly terminated 50-ohm loads.

The Am8151A provides the I_{REF} input to scale the VIDEO output. The relationship between I_{REF} and IFS is IFS = 13.22 I_{REF}. The reference amplifier in the Am8151A is internally compensated, eliminating the need for external bypass capacitors. In addition, the analog V_{EE} may be connected directly to the $ECLV_{EE}$ supply. Analog V_{CC} should be bypassed separately from $TTLV_{CC}$. The Am8151A has no connections on pins 22 and 25 (the Am8151 COMP1 and COMP2 pins).

DAC and DAC Decoder

The VIDEO output of the Am8151A is obtained by switching identical multiples of the 255 gray scale LSB currents. Blank and Peak White outputs are 28 LSBs each, adding 0.71 mV to VIDEO output; and Sync is 112 LSBs. All output switching occurs at the third pipeline clock. Blank and Peak White currents are delay-matched grey scale data. The video gray scale is generated by decoding the three most significant bits into seven 32 LSB equal segments and binary scaling the five LSBs. The reference feedback current, I_{REF}, is two 16 LSB currents matched with D4 for a total of 32 LSBs.

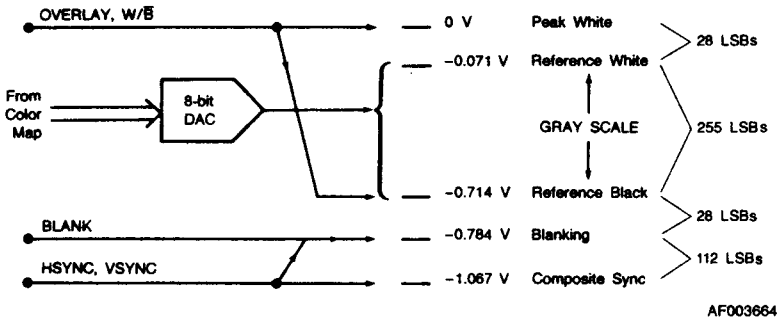
The twelve gray scale switches (seven MSB segments and five LSB segments) and the three control switches are operated from glitch-free internal CML differential logic gates which eliminate current spikes characteristic of normal Bipolar Emitter Followers. All logic in the Am8151A, as well as the output switches, use glitch-free CML to reduce internal current spikes synchronous with CLK transitions. As a result, the clock feedthrough in the Am8151A is less than 4 pV-sec for ECL operating mode. The glitch energy output of the Am8151A is reduced to 10 pV-sec which allows true 8-bit operation at up to 125 MHz clock rate. The low glitch energy error produced at the Am8151A VIDEO output is a result of matching the five LSB's switching to the seven MSB segments within 0.2 ns. The elimination of external compensation capacitors for the Reference Amplifier also contribute to the reduction in Glitch Energy Output.

The following truth table lists the nominal DAC output for all combinations of inputs assuming a reference current of 1.076 mA. These output levels are obtained with R_{SET} = 2000 ohms and R_T = 75 ohms.

TRUTH TABLE

W/$\overline{B}$	OVERLAY	BLANK	HSYNC	VSYNC	Data	Current	Voltage into 75 Ω	Level	Cum LSBs
1	1	0	0	0	X	0 mA	0 mV	Peak White	0
X	0	0	0	0	255	.94 mA	−71 mV	Reference White	28
						•			
						•	255 Equal Steps		
						•			
X	0	0	0	0	0	9.52 mA	−714 mV	Reference Black	283
0	1	0	0	0	X	9.52 mA	−714 mV	Reference Black	283
X	X	1	0	0	X	10.46 mA	−784 mV	Blanking	311
X	X	X	1	1	X	10.466 mA	−784 mV	Blanking	311
X	X	X	0	1	X	14.22 mA	−1067 mV	Composite Sync	423
X	X	X	1	0	X	14.22 mA	−1067 mV	Composite Sync	423

Am8151A DAC OUTPUT LEVELS



ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous (TTL V_{CC} and $ANAV_{CC}$) ..... −0.5 to +7.0 V
Supply Voltage to Ground Potential
Continuous (ECL V_{EE} and $ANAV_{EE}$) ..... +0.5 to −7.0 V
DC Input Voltage (TTL) ..... −0.5 to 5.5 V
DC Input Current ..... −30 to +5.0 mA
DC Input Voltage (LC Controlled) ..... −2 V to 5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commericial (C) Devices
Ambient Temperature (T_A) ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Supply Voltage (V_{EE}) ..... −5.72 V to −4.68 V

Military (M) Devices
Case Temperature (T_C) ..... −55°C to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Supply Voltage (V_{EE}) ..... −5.72 V to −4.68 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

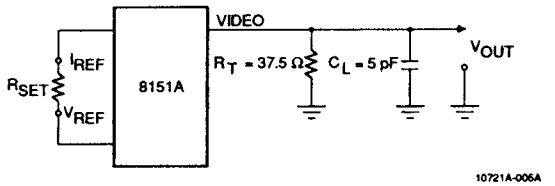
DC CHARACTERISTICS over operating ranges (TTL) (for APL Products, Group A Subgroups 1, 2, 3, 7, 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 9)	2.0			V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 9)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V		−0.01	−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V		.01	40	μA
I_I	Input HIGH Current	V_{IN} = V_{CC} = 5.25 V			1	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} = V_{IL} I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} = V_{IL} I_{OL} = 8 mA		0.3	0.5	V
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = Max.	−20	−30	−70	mA
$TTLI_{CC}$	Power Supply Current	$TTLV_{CC}$ = Max.		33	55	mA
$ANAI_{CC}$	Power Supply Current	$ANAV_{CC}$ = Max.		7.1	10	mA
$ECLI_{EE}$	Power Supply Current	$ECLV_{EE}$ = Max.		195	300	mA
$ANAI_{EE}$	Power Supply Current	$ANAV_{EE}$ = Max. R_{SET} = 667 Ω		51	60	mA
LCI_{CC}	Logic Control Supply Current	LC = Max.		15	25	mA

ECL CHARACTERISTICS (Notes 4 & 5)

Parameter Description	Parameter Symbol	Test Conditions	−55°C	0°C	25°C	70°C	125°C	Unit
ECL Inputs	V_{IH} (Max.)	(Note 9)	−860	−840	−810	−730	−650	mV
	V_{IH} (Min.)		−1215	−1145	−1105	−1045	−1005	
	V_{IL} (Max.)	(Note 9)	−1590	−1565	−1550	−1525	−1470	mV
	V_{IL} (Min.)		−1900	−1870	−1850	−1830	−1800	
	I_{IH} (Max.)	V_{EE} = Max. V_{IN} = V_{IH} (Max.)	250	200	200	200	200	μA
	I_{IL} (Max.)	V_{EE} = Max. V_{IN} = V_{IL} (Min.)	200	150	150	150	150	μA

Notes:
1. For conditions shown as Min. or Max. use the appropriate value specified under recommended operating range.
2. Typical values are for $TTLV_{CC}$ and $ANAV_{CC}$ = 5.0 V, $ECLV_{EE}$ and $ANAV_{CC}$ = −5.2 V, LC = 5.0 V or 0 V as appropriate, T_A = 25°C.
3. Not more than one output should be shorted at a time. Duration of short not to exceed one second.
4. With airflow ≥ 500 lfpm and two-minute warmup.
5. A combination of skewing the limits and adjusting the pulse test ambient temperature is used to ensure that the data sheet steady state limits are met at the ambient temperatures specified.
6. Trimmable to −714 mV
7. Gray scale is defined as output levels between reference white and reference black, −71 mV to −714 mV. For these conditions the absolute value of 0.5 LSB = 1.26 mV.
8. Clock feedthrough for rising or falling input may be measured with either constant memory address or constant memory data. For the Am8151A it is expressed as an Energy error with units of pV−S, consistent with glitch energy.
9. Not all tests are being performed in manufacturing. Tests are guaranteed by Engineering characterization.
10. Tests are performed in manufacturing under worst temperature conditions.



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DAC SPECIFICATIONS over COMMERCIAL operating range

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
	Resolution	Gray Scale (Note 6)		8	8	8	bits
	Linearity	Gray Scale (Note 7)			±0.15	±.5	LSB
	Differential Linearity	Gray Scale (Note 7)			±.05	±.5	LSB
V_{OC}	Output Compliance Voltage	$I_O \leq I_{MAX}$ (Note 9)		±1.5	±2.2		V
I_{ZS}	Zero Scale Current				.01	1	LSB
$I_{Max.}$	Output Maximum Current			42.7	60		mA
PSS IFS±	Power Supply Sensitivity, Full Scale Positive	V_{CC} = 5 V ±10% V_{EE} = −5.2 V ±10%			±0.1	±0.5	%/% Δ V
	Glitch Energy Feedthrough	LC = GND, CLK ≤ Max.			±10		pV-sec
	Output Capacitance				10		pF
I_{REF}	DAC Reference Current					3.4	mA
CLK	Clock Frequency	LC = GND, ECL Mode		D.C	250	200	MHz
		LC = V_{CC}, TTL Mode		D.C		83	
t_R	Risetime: 10 to 90% (Note 9)	R_{SET} = 1000Ω R_T = 37.5Ω			1.8	2.3	ns
t_F	Falltime: 90 to 10% (Note 9)	R_{SET} = 1000Ω R_T = 37.5Ω			1.55	2.1	ns
t_S	Setting Time (255 Level of Gray)	% Gray Scale (Notes 7 & 9)	Bits Accuracy				
		±0.2	8		9.5		
		±0.4	7		5.2		
		±0.8	6		3.2		
		±1.6	5		2.8		
		±3.2	4		2.4		ns
V_{OB}	Reference Black Output (Note 6)	R_{SET} = 1000Ω R_T = 37.5Ω		−728	−714	−700	mV
I_{FSTC}	Output Current Temp Coefficient				±20		ppm/°C
V_{REF}	DAC Reference Voltage	$I_O \leq$ 4 mA V_{CC} = 5.0 V V_{EE} = −5.2 V		2.122	2.152	2.177	V
	Reference Voltage Line Regulation	ΔV_{CC} = ±10% ΔV_{EE} = ±10%			±0.13	±0.4	% V_{REF}
	Reference Voltage Load Regulation	3.2 mA ≤ I_O ≤ 9.7 mA			±.06	±0.4	% V_{REF}
	Reference Voltage Temperature Coeffiecient				±15		ppm/°C
CLK_n	Clock Feedthrough (Note 8)	LC = GND CLK ≤ Max.			±4		pV-S

Notes: See notes following ECL Characteristics

DAC SPECIFICATIONS over **MILITARY** operating range (for APL Products, Group A, Subgroups 1, 2, 3, 7, 8, 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
	Resolution	Gray Scale (Note 6)		8	8	8	bits
	Linearity	Gray Scale (Note 7)			±0.15	±1	LSB
	Differential Linearity	Gray Scale (Note 7)			±.05	±1	LSB
V_{OC}	Output Compliance Voltage	$I_O \leq I_{MAX}$ (Note 9)		±1.5	±2.2		V
I_{ZS}	Zero Scale Current				.01	1	LSB
$I_{Max.}$	Output Maximum Current			40	60		mA
PSS IFS±	Power Supply Sensitivity, Full Scale Positive	V_{CC} = 5 V ±10% V_{EE} = −5.2 V ±10%			±0.1	±0.5	%/% Δ V
	Glitch Energy Feedthrough	LC = GND, CLK ≤ Max.			±10		pV-sec
	Output Capacitance				10		pF
I_{REF}	DAC Reference Current					3.4	mA
CLK	Clock Frequency	LC = GND, ECL Mode		D.C	250	160	MHz
		LC = V_{CC}, TTL Mode		D.C		83	
t_R	Risetime: 10 to 90% (Note 9)	R_{SET} = 1000Ω R_T = 37.5Ω			1.8	2.5	ns
t_F	Falltime: 90 to 10% (Note 9)	R_{SET} = 1000Ω R_T = 37.5Ω			1.55	2.3	ns
t_S	Setting Time (255 Level of Gray)	% Gray Scale (Notes 7 & 9)	Bits Accuracy				
		±0.2	8		9.5		
		±0.4	7		5.2		
		±0.8	6		3.2		
		±1.6	5		2.8		
		±3.2	4		2.4		ns
V_{OB}	Reference Black Output (Note 6)	R_{SET} = 1000Ω R_T = 37.5Ω		−728	−714	−700	mV
I_{FSTC}	Sync Output Current Temp Coefficient				±20		ppm/°C
V_{REF}	DAC Reference Voltage	$I_O \leq$ 4 mA V_{CC} = 5.0 V V_{EE} = −5.2 V		2.122	2.152	2.177	V
	Reference Voltage Line Regulation	ΔV_{CC} = ±10% ΔV_{EE} = ±10%			±0.13	±0.4	% V_{REF}
	Reference Voltage Load Regulation	3.2 mA ≤ I_O ≤ 9.7 mA			±.06	±0.4	% V_{REF}
	Reference Voltage Temperature Coefficient				±15		ppm/°C
CLK_n	Clock Feedthrough (Note 8)	LC = GND CLK ≤ Max.			±4		pV-S

Notes: See notes following ECL Characteristics

3

EXPLANATION OF DAC SPECIFICATIONS

Resolution:
Resolution refers to the number of discrete steps or levels which the DAC can provide, and is expressed as a number of bits. A DAC with n bits of resolution provides 2^n discrete analog levels. For the Am8151A the gray scale code between Reference Black and Reference White has 255 codes.

Linearity:
Linearity is the maximum deviation of an actual output from its ideal value. For the Am8151A, linearity is expressed as a fraction of an LSB.

Differential Linearity:
Differential Linearity is the measure of the difference between any two code values. For the Am8151A, differential linearity is expressed as a fraction of an LSB.

Output Compliance Voltage:
The DC voltage output for which the Am8151A will meet its Output Current, Linearity, and Differential Linearity specifications.

Zero Scale Current:
The output current of the Am8151A at Peak White output level.

Full Scale Current: (I_{FS}):
The output current at Sync output level. $I_{FS} = 13.22\ I_{REF}$.

Full Scale Current Temperature Coefficient (I_{FSTC}):
The ratio of the full scale output current to the temperature change causing it.

Power Supply Sensitivity (P_{SS} I_{FS}):
The change in the full scale output current for changes in one or more power supply voltages, expressed as a percentage of the power supply change.

Ref Black Output Level (V_{OB}):
The video voltage output of the Am8151A with $R_{SET} = 1000\ \Omega$, $R_T = 37.5\ \Omega$, and Reference Black as the output level.

Reference Current (I_{REF}):
The current into the I_{REF} pin.

Output Capacitance (C_O):
The package and DAC output capacitance of the Video pin on the Am8151A. For the ceramic DIP package C_O is 11 pF, while the plastic DIP and PLCC is 6 pF.

Output Delay:
Propagation delay from the CLK logic threshold to a 50% change in gray scale output level.

Output Settling Time:
Propagation delay from the 50% output change to within the specified percentage of final value.

Output Clock Feedthrough (CLK_n):
Synchronous video output noise. In the Am8151A, expressed as pV-S of energy.

Output Glitch Energy:
The mismatch in the energy of the undershoot and overshoot pulse for a 1 LSB transition at the Video output. In the Am8151A glitch energy is expressed in pV-S. It may also be expressed as LSB error for a given clock period. A half LSB glitch energy error at $f_{CLK} =$ 125 MHz is 10.1 pV-S.

EXPLANATION OF REFERENCE VOLTAGE SPECIFICATIONS

Reference Voltage ($V_{REF} - V$ (I_{REF})):
The voltage from the V_{REF} to the I_{REF} pin.

Line Regulation:
The change in the reference voltage produced by changes in one or more of the Am8151A power supply voltages expressed as a percentage of the reference voltage.

Load Regulation:
The change in the reference voltage produced with changes in the current in the V_{REF} pin expressed as a percentage of the reference voltage.

Reference Voltage Temperature Coefficient:
The change in the reference voltage divided by the temperature change producing it expressed in ppm/°C.

AC SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
1	t_{CLK}	Clock Period (Note 9)	LC = GND, ECL Mode LC = V_{CC}, TTL Mode	5 12	4.1		ns ns
2	t_S	Address, OVERLAY, W/$\overline{B}$ Setup before Clock ↑ HSYNC, VSYNC, BLANK Setup before Clock ↑ Address, OVERLAY, W/$\overline{B}$, HSYNC, VSYNC, BLANK Setup before Clock ↓ (Note 9)	LC = GND LC = GND LC = V_{CC}	0.7 5.0 2.0	0.05 1.5 0.5		ns ns ns
3	t_H	Address, OVERLAY, W/$\overline{B}$ Hold after Clock ↑ HSYNC, VSYNC, BLANK Hold after Clock ↑ Address, OVERLAY, W/$\overline{B}$, HSYNC, VSYNC, BLANK after Clock ↓ (Note 9)	LC = GND LC = GND LC = V_{CC}	0.7 2.0 2.0	−0.05 −1.5 −0.5		ns ns ns
4	t_{PD}	Clock ↑ to 50% VIDEO change (Note 9)	LC = GND LC = V_{CC}	2.0 4.0	5.3	8 12	ns ns
5	t_{PD} ECL/TTL	Clock ↑ to Data Valid (Read) (Note 10)		5	13	30	ns
6	t_S	W/$\overline{R}$ Setup before $\overline{EN}$ ↓ (Note 9)		10	1.5		ns
7	t_H	W/$\overline{R}$ Hold after $\overline{EN}$ ↑ (Note 9)		10	1.5		ns
8	t_{PD}	$\overline{EN}$ ↓ to Data Active (Read) (Note 10)		5	11	25	ns
9	t_{PD}	$\overline{EN}$ ↑ to Data Three-State (Read) (Note 10)			7	20	ns
10	t_S	Address latched (Clock ↑) to $\overline{EN}$ ↓ Setup (Write) (Note 9)		10	4		ns
11	t_S	Data (and Address) Setup before $\overline{EN}$ ↑, Write Cycle Time (Write) (Note 9)		12	1.5		ns
12	t_H	Data Hold after $\overline{EN}$ ↑ (Note 9)		10	1.5		ns
13	t_{PD}	$\overline{EN}$ Low Pulse Width to Write (Note 9)			3		ns

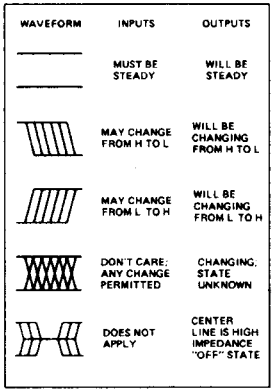
AC SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
1	t_{CLK}	Clock Period (Note 9)	LC = GND, ECL Mode LC = V_{CC}, TTL Mode	6.25 12	4.1		ns ns
2	t_S	Address, OVERLAY, W/$\overline{B}$ Setup before Clock ↑ HSYNC, VSYNC, BLANK Setup before Clock ↑ Address, OVERLAY, W/$\overline{B}$, HSYNC, VSYNC, BLANK Setup before Clock ↓ (Note 9)	LC = GND LC = GND LC = V_{CC}	1.0 5.0 2.0	0.05 1.5 0.5		ns ns ns
3	t_H	Address, OVERLAY, W/$\overline{B}$ Hold after Clock ↑ HSYNC, VSYNC, BLANK Hold after Clock ↑ Address, OVERLAY, W/$\overline{B}$, HSYNC, VSYNC, BLANK after Clock ↓ (Note 9)	LC = GND LC = GND LC = V_{CC}	1.0 2.0 2.0	−0.05 −1.5 −0.5		ns ns ns
4	t_{PD}	Clock ↑ to 50% VIDEO change (Notes 9)	LC = GND LC = V_{CC}	2.0 4.0	5.3	8 12	ns ns
5	t_{PD} ECL/TTL	Clock ↑ to Data Valid (Read) (Note 10)		5	13	30	ns
6	t_S	W/$\overline{R}$ Setup before $\overline{EN}$ ↓ (Note 9)		10	1.5		ns
7	t_H	W/$\overline{R}$ Hold after $\overline{EN}$ ↑ (Note 9)		10	1.5		ns
8	t_{PD}	$\overline{EN}$ ↓ to Data Active (Read) (Note 10)		5	11	25	ns
9	t_{PD}	$\overline{EN}$ ↑ to Data Three-State (Read) (Note 10)			7	20	ns
10	t_S	Address latched (Clock ↑) to $\overline{EN}$ ↓ Setup (Write) (Note 9)		10	4		ns
11	t_S	Data (and Address) Setup before $\overline{EN}$ ↑, Write Cycle Time (Write) (Note 9)		12	1.5		ns
12	t_H	Data Hold after $\overline{EN}$ ↑ (Note 9)		10	1.5		ns
13	t_{PD}	$\overline{EN}$ Low Pulse Width to Write (Note 9)			3		ns

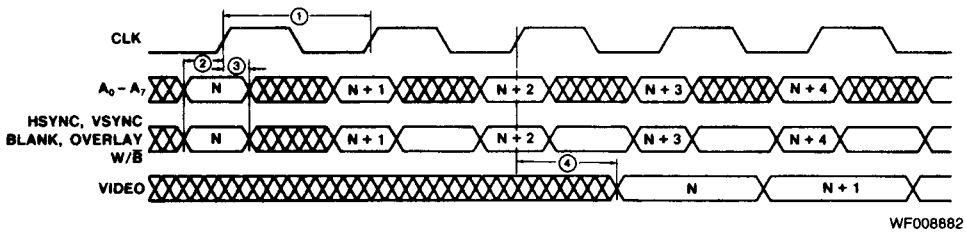
Notes: See notes following ECL Characteristics

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



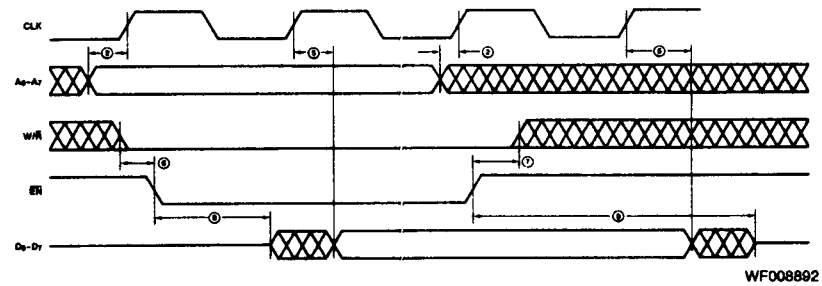
KS000010



WF008882

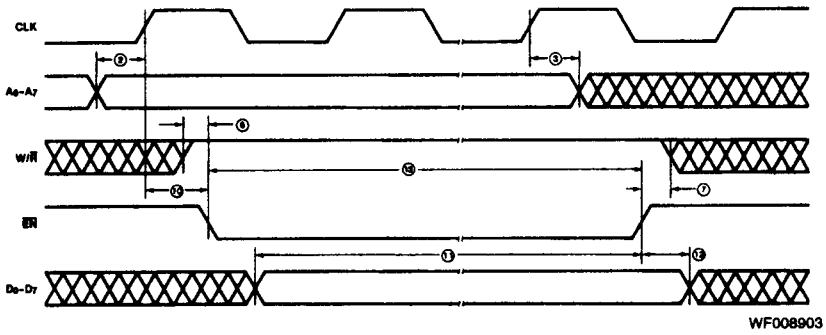
Video Refresh Timing

SWITCHING WAVEFORMS (Cont'd.)



WF008892

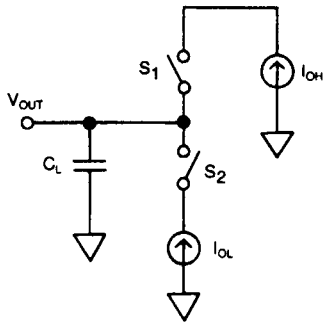
Read Timing



WF008903

Write Timing

SWITCHING TEST CIRCUIT

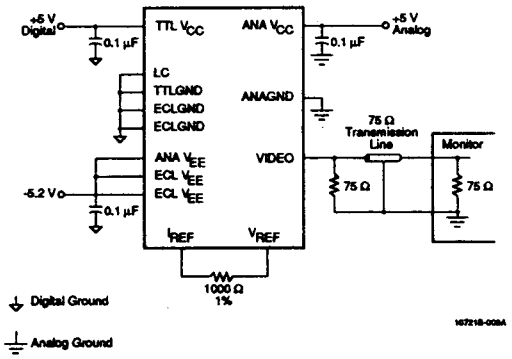


TC003132

A. Outputs

Notes: 1. C_L = 50 pF. The load capacitance includes scope probe, wiring, and stray capacitance without the device in the test fixture.
2. S_1 and S_2 are open during all DC and functional testing.
3. During AC testing, switches are set as follows:
   1) For $V_{OUT} > 1.5$ V, S_1 is closed and S_2 open
   2) For $V_{OUT} < 1.5$ V, S_1 is open and S_2 closed

TYPICAL CONNECTION DIAGRAM



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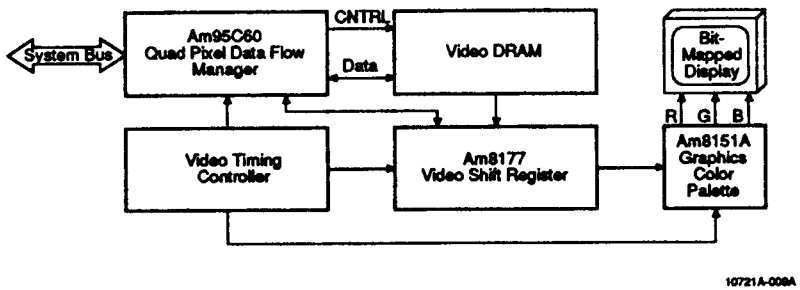
TYPICAL APPLICATION



BD006170

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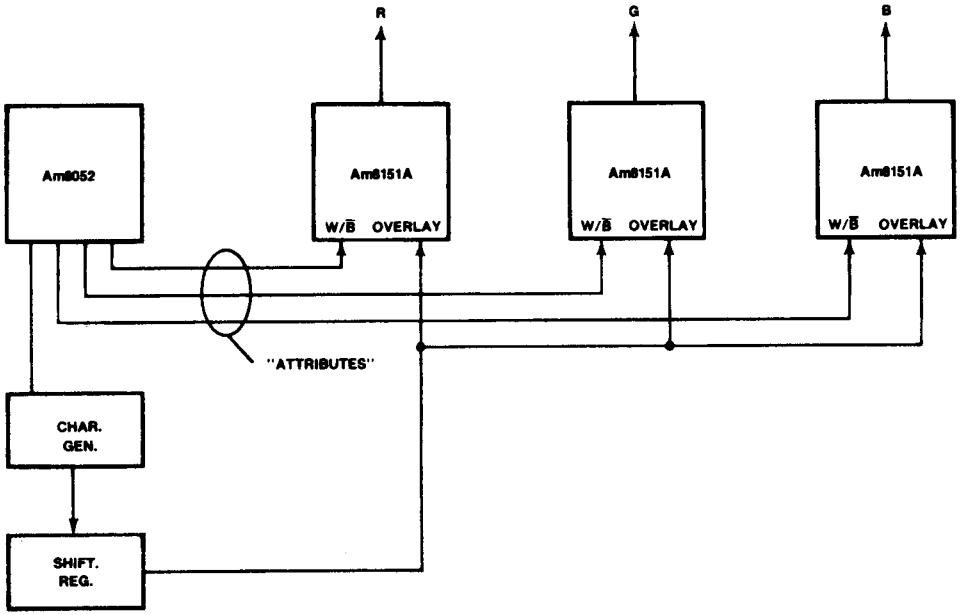
GENERATING 8 COLOR TEXT OVERLAY WITH W/$\overline{B}$ AND OVERLAY INPUTS



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SINGLE Am8151A TRUTH TABLE

Overlay	W/$\overline{B}$	Output
0	X	Graphics
1	1	Peak White
1	0	Ref. Black

TRUTH TABLE FOR THREE Am8151As

	W/$\overline{B}$			
Overlay	(R)	(G)	(B)	Output
0	X	X	X	Graphics
1	0	0	0	Black
1	0	0	1	Blue
1	0	1	0	Green
1	0	1	1	Cyan
1	1	0	0	Red
1	1	0	1	Magenta
1	1	1	0	Yellow
1	1	1	1	White