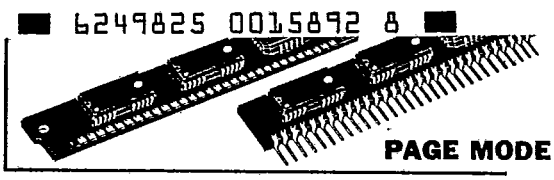

MH25609AJ-85,-10,-12/ MH25609AJA-85,-10,-12

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

DESCRIPTION

The MH25609AJ, AJA is 262144 word x 9 bit dynamic RAM and consists of two industry standard 256K x 4 dynamic RAMS in SOJ and one industry standard 256K x 1 dynamic RAM in PLCC.

The mounting of SOJ and PLCC on a single in-line package provides any application where high densities and large quantities of memory are required.

MH25609AJA is a leaded type-memory module, allowing direct insertion to normal through-hole-board like DIP devices.

MH25609AJ is a socket type-memory module, suitable for easy interchanging or addition of modules.

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH25609AJ-85 MH25609AJA-85	85	160	700
MH25609AJ-10 MH25609AJA-10	100	190	610
MH25609AJ-12 MH25609AJA-12	120	220	530

- Utilizes industry standard 1M RAMs in SOJ and 256K RAM in PLCC
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation . . . . . 305mW (max)
- Low operation power dissipation
  - MH25609AJ-85/MH25609AJA-85 . . 1211mW (max)
  - MH25609AJ-10/MH25609AJA-10 . . 1076mW (max)
  - MH25609AJ-12/MH25609AJA-12 . . . 936mW (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF x 3) decoupling capacitors

PIN CONFIGURATION (TOP VIEW)

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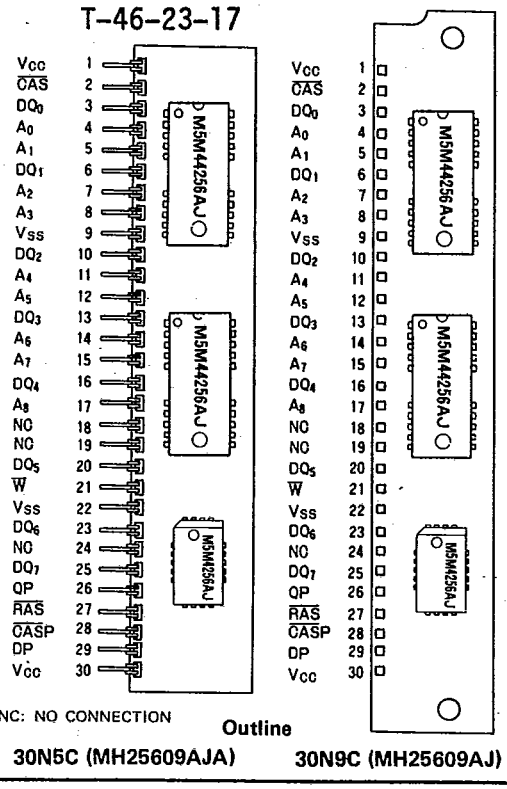


NC: NO CONNECTION

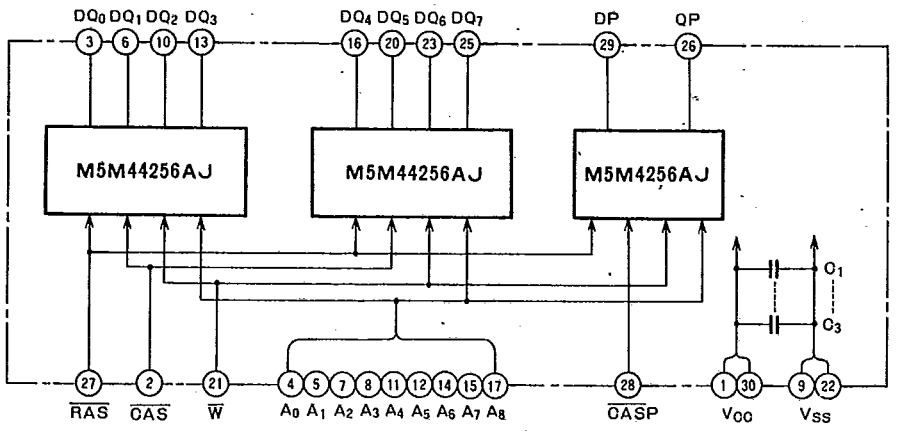
Outline

30N5C (MH25609AJA) 30N9C (MH25609AJ)

APPLICATION

Main memory unit for computers, Microcomputer memory

BLOCK DIAGRAM



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MITSUBISHI (MEMORY/ASIC)

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

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FUNCTION

The MH25609AJ, AJA provide, in addition to normal read, and early write operations, a number of other functions, e.g., page mode. $\overline{RAS}$-only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	3	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage all inputs	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

MH25609AJ-85,-10,-12/MH25609AJA-85,-10,-12

MITSUBISHI (MEMORY/ASIC)

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

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ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−20		20	μA
I_I	Input current		0V≦V_{IH}≦6.5V, Other input pins=0V	−20		20	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	MH25609A-85	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min, output open			210	mA
		MH25609A-10				185	
		MH25609A-12				160	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			6.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	MH25609A-85	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min, output open			200	mA
		MH25609A-10				175	
		MH25609A-12				150	
$I_{CC4(AV)}$	Average supply current from V_{CC} page mode (Note 3, 4)	MH25609A-85	$\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycling t_{PC}=min, output open			175	mA
		MH25609A-10				150	
		MH25609A-12				125	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH25609A-85	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min, output open			205	mA
		MH25609A-10				180	
		MH25609A-12				165	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_i=25mVrms			30	pF
$C_{I(W)}$	Input capacitance, write control input				25	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				25	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				20	pF
$C_{I/O}$	Input/Output capacitance, data ports				15	pF
$C_{I(CASP)}$	Input capacitance, $\overline{CASP}$ input				12	pF
$C_{I(DP)}$	Input capacitance				10	pF
$C_{I(OP)}$	Output capacitance	V_O=V_{SS}, f=1MHz, V_i=25mVrms			12	pF

MITSUBISHI ELECTRIC

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MITSUBISHI (MEMORY/ASIC)

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

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SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			MH25609A-85		MH25609A-10		MH25609A-12		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		45		50		60	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		85		100		120	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 10)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.

8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.

9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.

10: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq$ |±20μA|) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Early Write, Page Mode Cycles)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, see notes 11, 12)

Symbol	Parameter		Limits						Unit
			MH25609A-85		MH25609A-10		MH25609A-12		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			4		4		4	ms
t_{RP}	$\overline{RAS}$ high pulse width		70		80		90		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 13)	25	40	25	50	25	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 14)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 15)	35		35		35		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	15	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		15		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		20		20		20		ns
t_T	Transition time	(Note 17)	3	50	3	50	3	50	ns

Note 11: The timing requirements are assumed t_T = 5ns.

12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

13: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} as shown in note 7, 9.

14: t_{CRP} requirement is applicable for all $\overline{RAS}$/$\overline{CAS}$ cycles.

15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for t_{CP} of page mode cycle.

16: $t_{ASC(max)}$ is specified as a reference point only of address access time.

17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			MH25609A-85		MH25609A-10		MH25609A-12		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		85	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		45	10000	50	10000	60	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		85		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		45		50		60		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 18)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 18)	10		10		10		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH25609A-85		MH25609A-10		MH25609A-12		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width	85	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	45	10000	50	10000	60	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	85		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	45		50		60		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 19)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		20		25		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	30		35		40		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	30		35		40		ns
t_{WP}	Write pulse width	15		20		25		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		20		25		ns

Note 19: When $t_{WCS} < t_{WCS(min)}$, Data input will contend with the data output because of the common I/O feature.

Page-Mode Cycle (Read, Early Write Cycle)

Symbol	Parameter	Limits						Unit
		MH25609A-85		MH25609A-10		MH25609A-12		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Read, Write cycle time	80		100		120		ns
t_{CP}	$\overline{CAS}$ high pulse width	25		40		50		ns

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

Symbol	Parameter	Limits						Unit
		MH25609A-85		MH25609A-10		MH25609A-12		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		20		25		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 20: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

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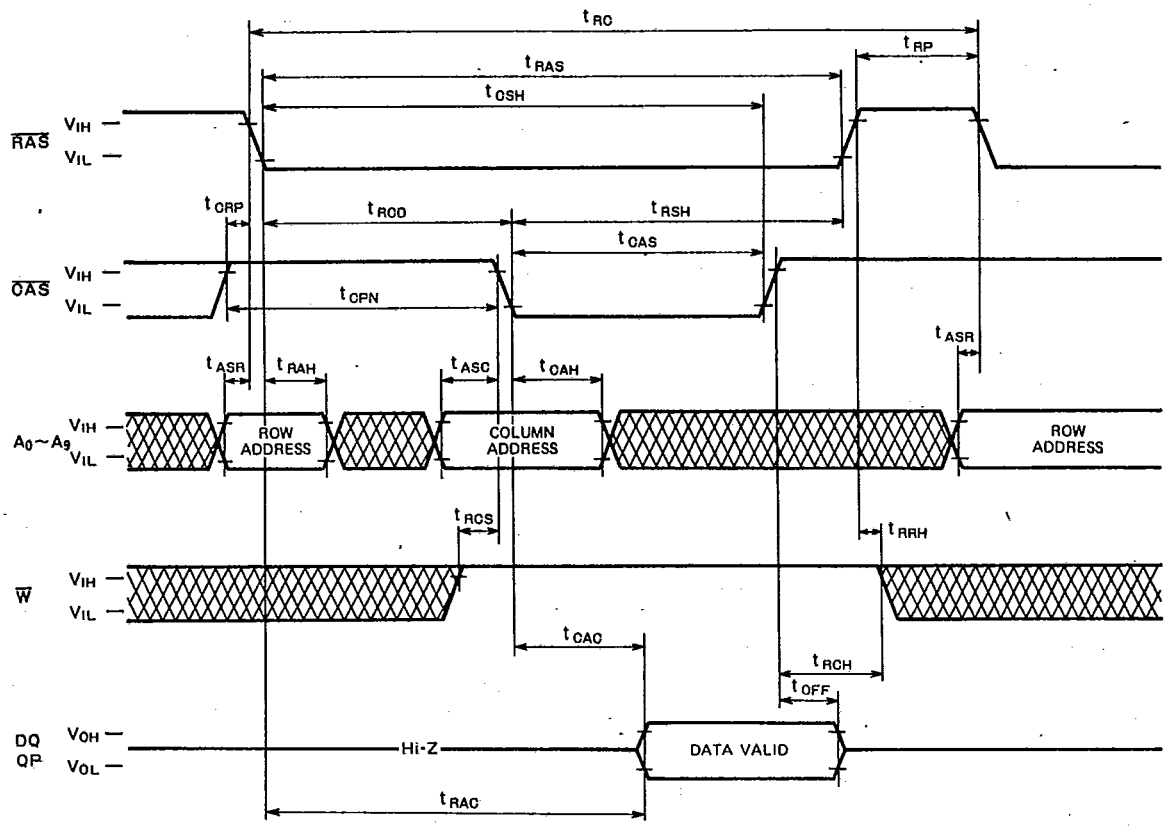
Timing Diagrams (Note 21)

Read Cycle



Note 21 Indicates the don't care input.

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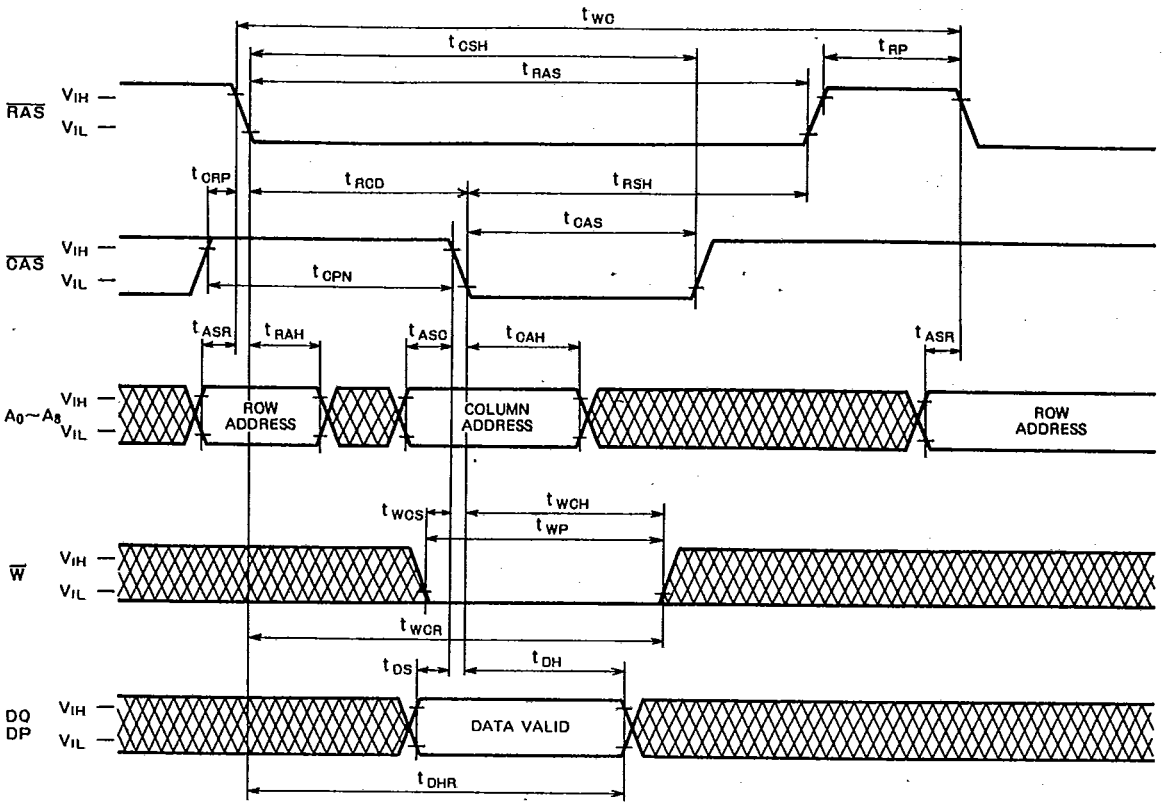
Early Write Cycle



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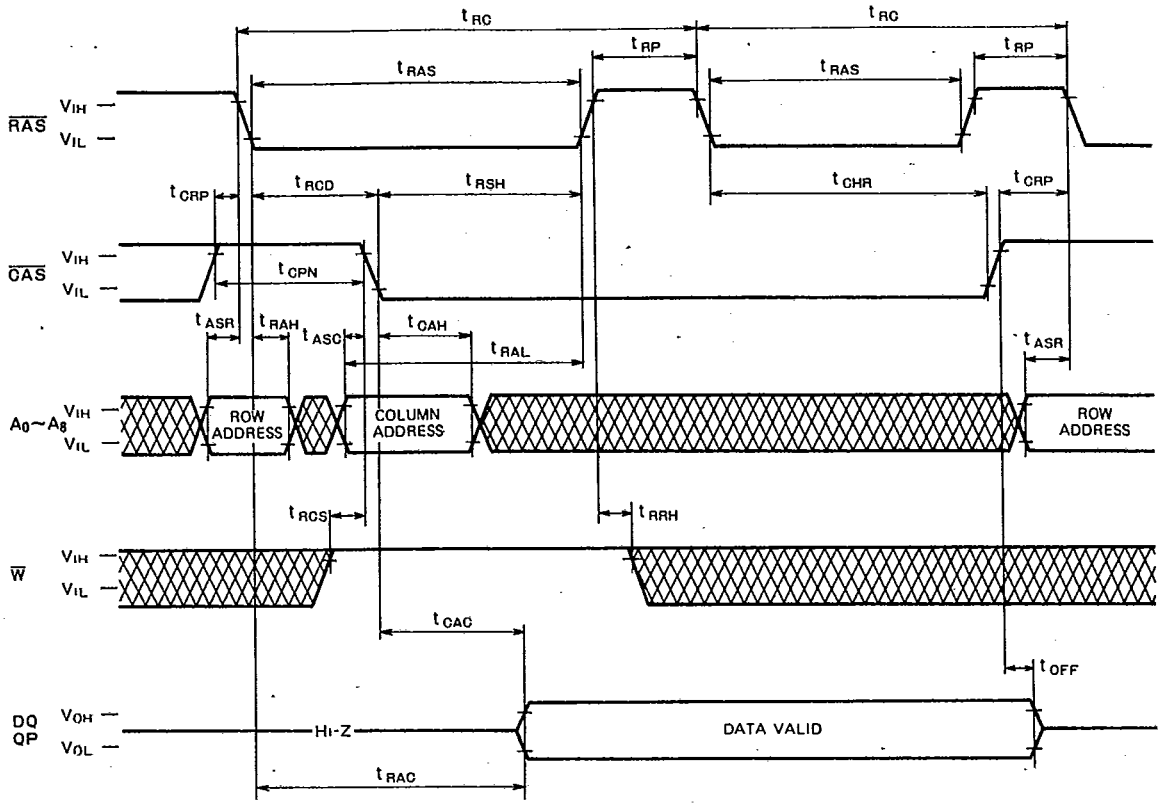
Hidden Refresh Cycle



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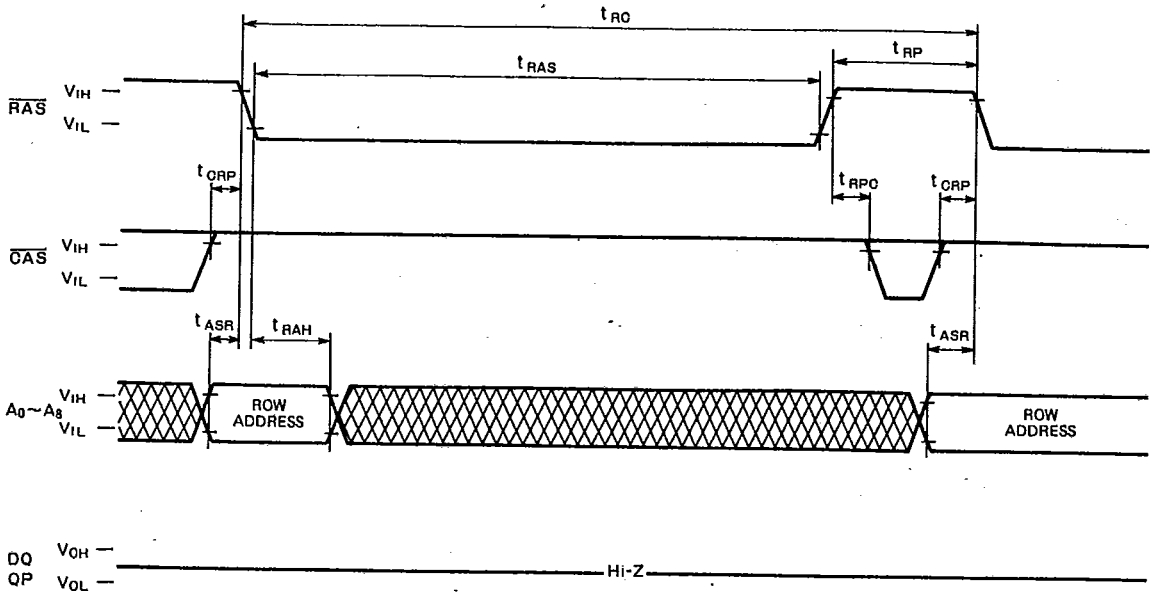
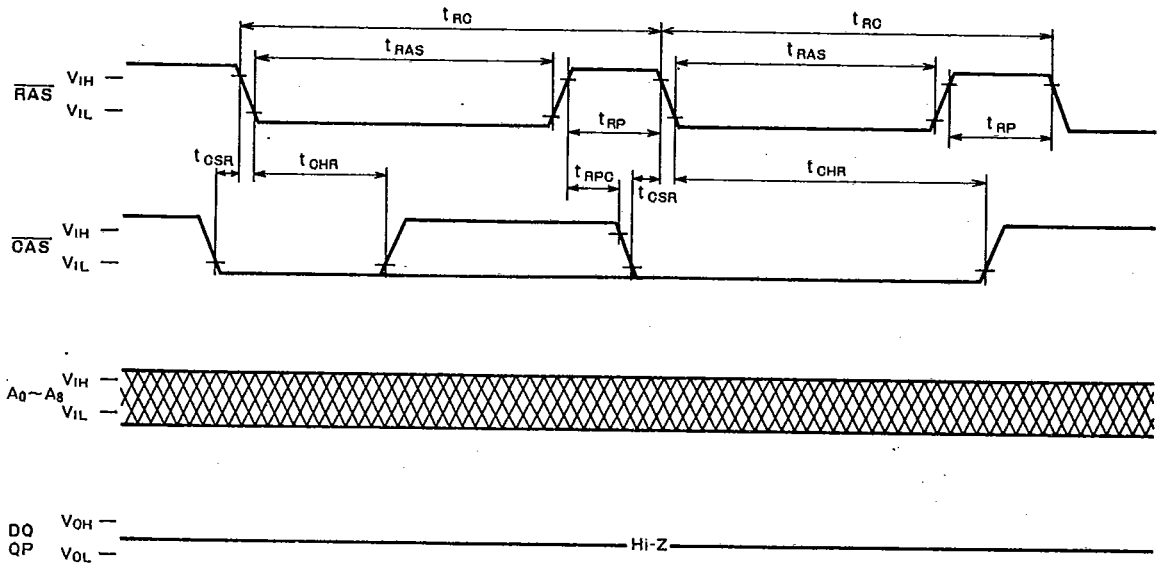
$\overline{RAS}$ only Refresh Cycle (Note 22)



Note 22: $\overline{W}$ = don't care, A_8 may be V_{IH} or V_{IL}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)



Note 23: $\overline{W}$ = don't care

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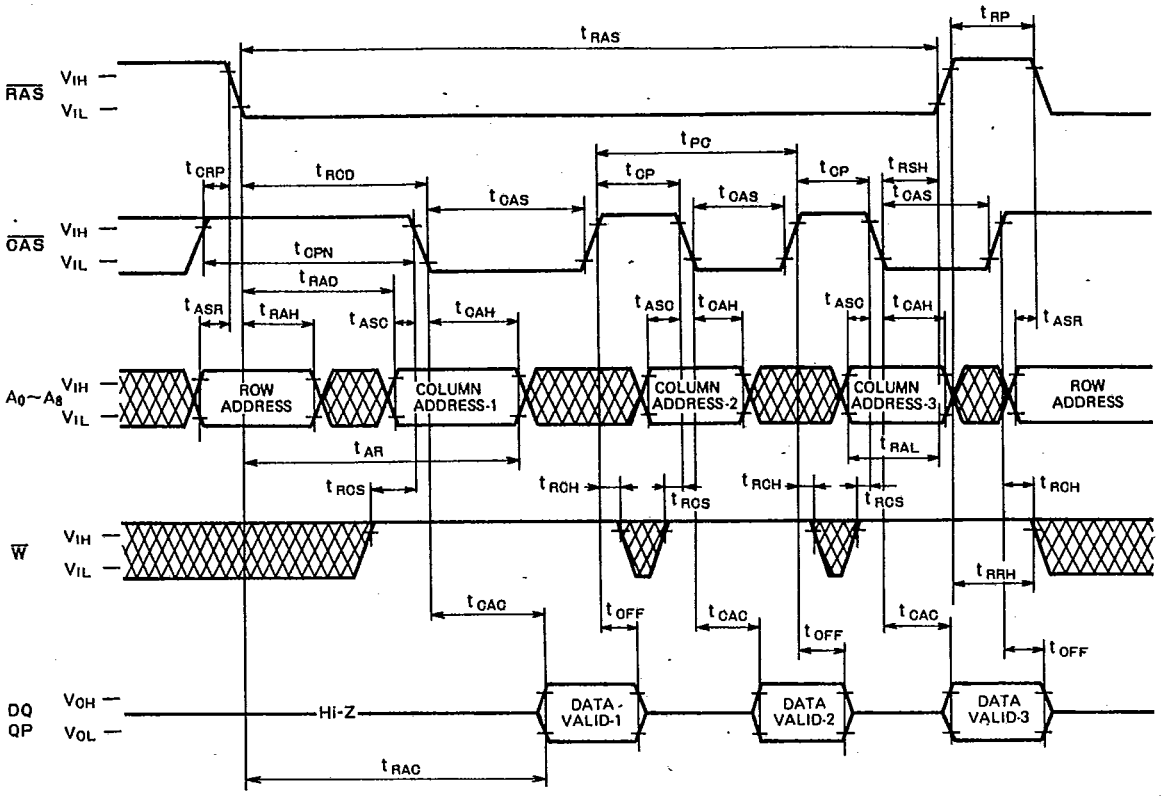
Page-Mode Read Cycle



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Page-Mode Early Write Cycle