

## FEATURES

- Separate clock inputs for count-up, count-down
- Asynchronous parallel load and clear
- Cascadable
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved  $V_{OL}$  compared to 9LS/74LS
- 440 $\mu$ A source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

## DESCRIPTION

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The 25LS192 is a BCD counter and the 25LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

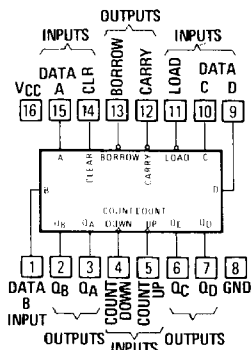
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

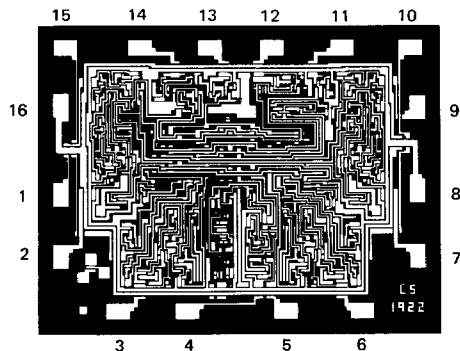
## PIN-OUT DIAGRAM



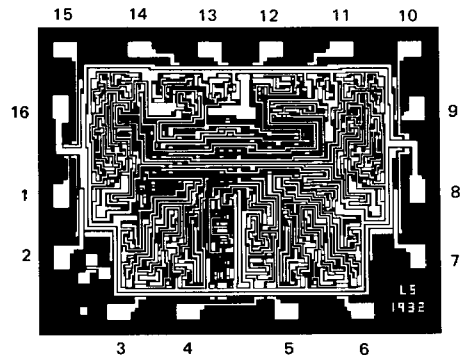
Low input to load sets  $Q_A = A$ ,  $Q_B = B$ ,

$Q_C = C$ , and  $Q_D = D$

25LS192



25LS193



Die Size: .100 x .077 (both types)

## Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-440			-440	$\mu$ A
Low-level output current, $I_{OL}$	4		8	4		8	mA
Count frequency, $f_{count}$	0		25	0		25	MHz
Width of any input pulse, $t_w$	20			20			ns
Data setup time, $t_{setup}$ (see Figure 1)	20			20			ns
Data hold time, $t_{hold}$	0			0			ns
Operating free-air temperature range, $T_A$	-55		125	0		70	$^{\circ}$ C

## Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*	Military			Commercial			Unit
		Min	Typ**	Max	Min	Typ**	Max	
$V_{IH}$		2			2			V
$V_{IL}$				0.7			0.8	V
$V_I$	$V_{CC} = \text{MIN}, I_I = -18$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -440\mu\text{A}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4\text{mA}$	0.25	0.40		0.25	0.40	V
		$I_{OL} = 8\text{mA}$	0.30	0.45		0.30	0.45	
$I_I$	$V_{CC} = \text{MAX}, V_I = 7V$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7V$			20			20	$\mu$ A
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4V$			-0.4			-0.4	mA
$I_{OS}^{\dagger}$	$V_{CC} = \text{MAX}$	-15		-85	-15		-85	mA
$I_{CC}^{\dagger\dagger}$	$V_{CC} = \text{MAX}$		19	34		19	34	mA

\*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\*All typical values are at  $V_{CC} = 5V, T_A = 25^{\circ}\text{C}$ .

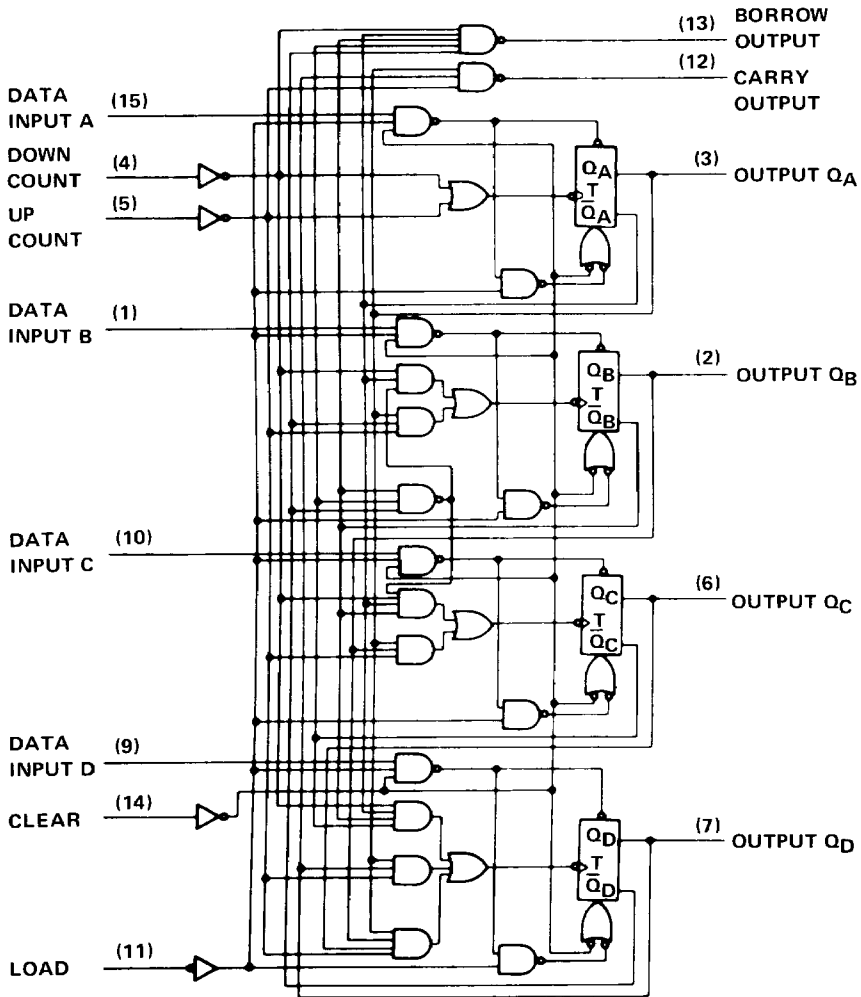
$\dagger$ Not more than one output should be shorted at a time.

$\dagger\dagger I_{CC}$  is measured with all inputs grounded and all outputs open.

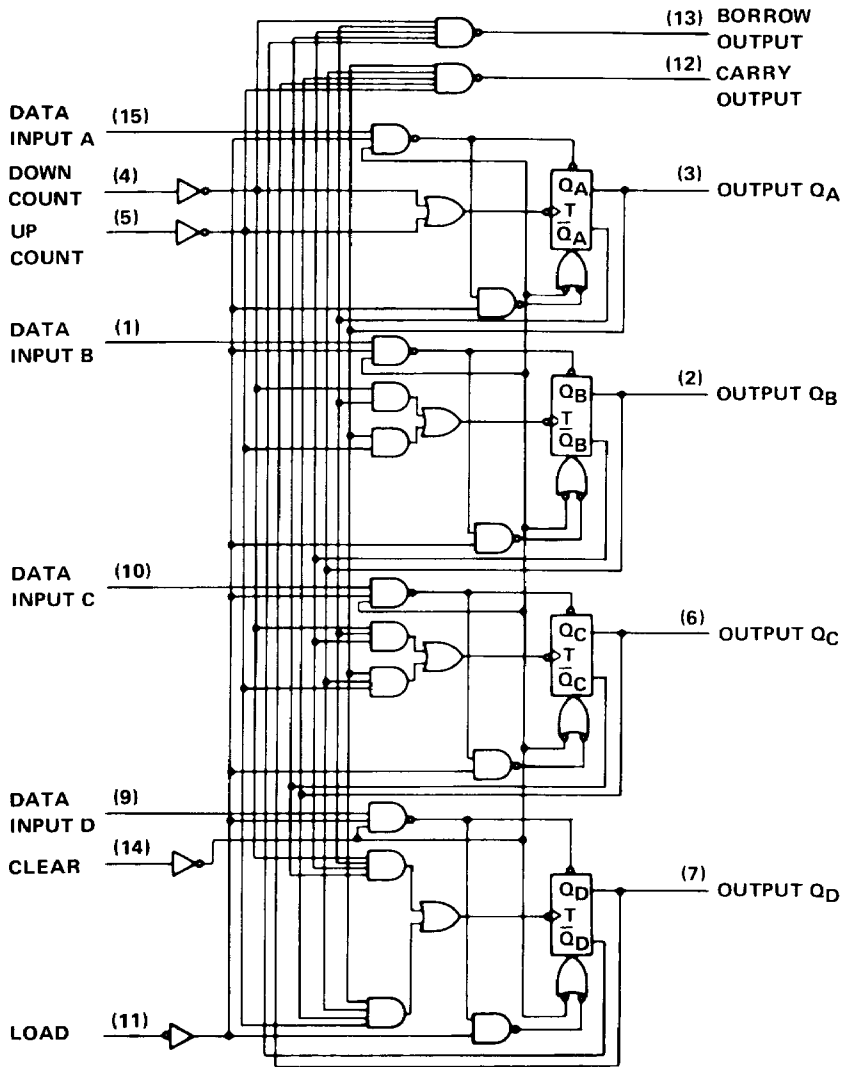
Switching Characteristics,  $V_{CC} = 5V$  Over Recommended Free-Air Temperature Range

Parameters	From (input)	To (output)	+25 $^{\circ}$ C			Unit
			Min	Typ	Max	
Test Conditions: $C_L = 15\text{pF}, R_L = 2k\Omega$ (See Fig. 1 & 2 on page 3-62 and 3-63 and Fig. A, page 2-174)						
$f_{max}$			25	35		MHz
$t_{PLH}$	Count-up	Carry		9	18	ns
$t_{PHL}$				17	24	
$t_{PLH}$	Count-down	Borrow		9	18	ns
$t_{PHL}$				17	24	
$t_{PLH}$	Either Count	Q		19	30	ns
$t_{PHL}$				20	32	
$t_{PLH}$	Load	Q		22	33	ns
$t_{PHL}$				29	40	
$t_{PHL}$	Clear	Q		23	33	ns

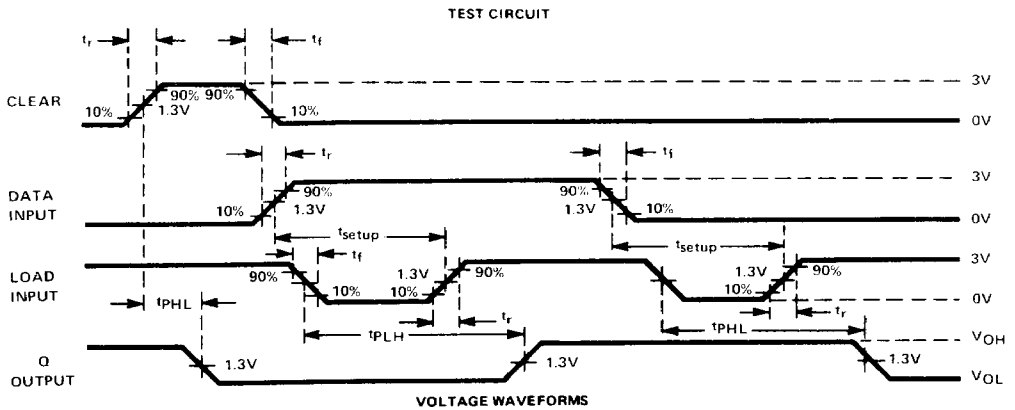
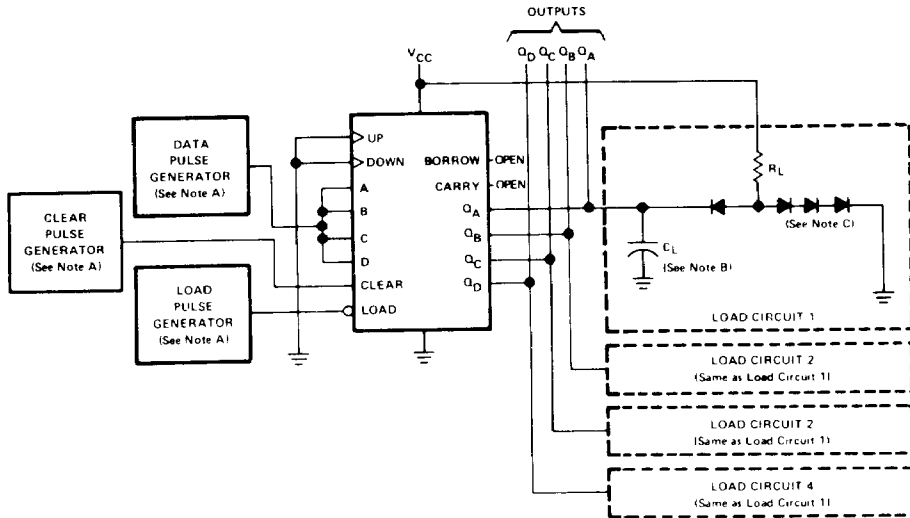
LOGIC DIAGRAM  
25LS192



LOGIC DIAGRAM  
25LS193



PARAMETER MEASUREMENT INFORMATION

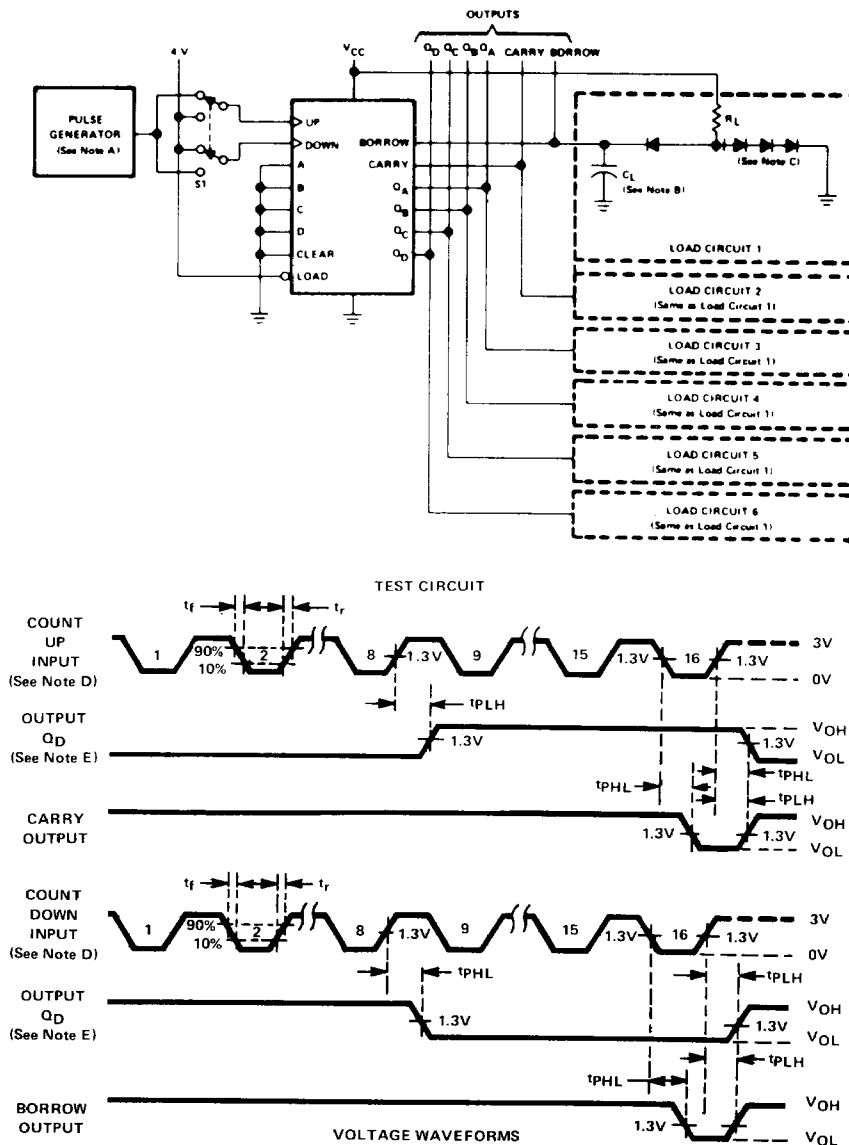


NOTES:

- A. The pulse generators have the following characteristics:  $Z_{out} = 50\Omega$  and for the data pulse generator PRR < 500KHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
- B.  $C_L$  includes probe and jig capacitance.
- C. Diodes are 1N3064.
- D.  $t_r$  and  $t_f \leq 7$  ns.

FIGURE 1 — CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION (Continued)



NOTES:

- A. The pulse generator has the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_{out} = 50\Omega$ , duty cycle = 50%.
- B.  $C_L$  includes probe and jig capacitance.
- C. Diodes are 1N3064.
- D. Count-up and count-down pulse shown is for the 25LS193 binary counter. Count cycle for 25LS192 decade counter is 1 through 10.
- E. Waveforms for outputs  $Q_A$ ,  $Q_B$ , and  $Q_C$  are omitted to simplify the drawing.
- F.  $t_r$  and  $t_f \leq 7\text{ns}$ .

FIGURE 2—PROPAGATION DELAY TIMES

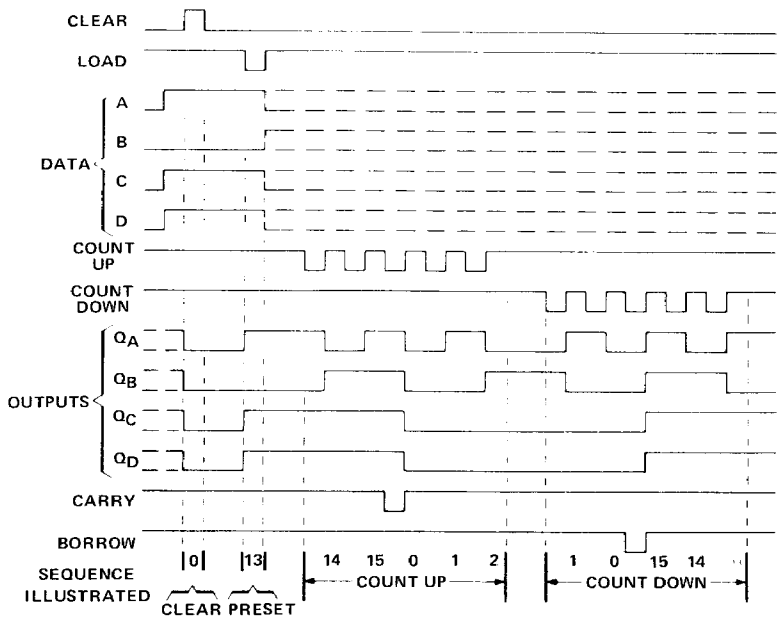


TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

25LS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES:

- A. Clear overrides load, data, and count inputs.
- B. When counting up, count-down input must be high; when counting down, count-up input must be high.