# HY512264 Series

## 128K x 16-bit CMOS DRAM with 2/CAS, Extended Data Out

**PRELIMINARY**

## DESCRIPTION

The HY512264 Series is a high performance CMOS fast dynamic RAM organized 131,072x16-bit config--uration. Independent read and write of upper and lower byte is controlled by 2 separate /CAS inputs. Refresh control is provided through /RAS-only, /CAS-before-/RAS, hidden refresh and self refresh modes. Multiplexed address inputs permit the HY512264 to be packaged in a 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

## ORDERING INFORMATION

| Part Number | Speed. | Power | Pkg. |
|---|---|---|---|
| HY512264JC | 50/60/70 | | SOJ |
| HY512264LJC | 50/60/70 | L-part | SOJ |
| HY512264SLJC | 50/60/70 | SL-part | SOJ |
| HY512264TC | 50/60/70 | | TSOP-II |
| HY512264LTC | 50/60/70 | L-part | TSOP-II |
| HY512264SLTC | 50/60/70 | SL-part | TSOP-II |

* Reverse TSOP-II packages are also available.

2M

## FEATURES

- Max. Active Power Dissipation

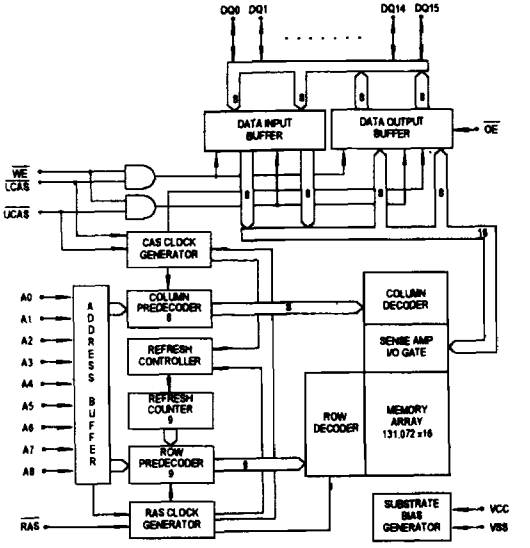
| Speed | Power |
|---|---|
| 50ns | 605.0mW |
| 60ns | 550.0mW |
| 70ns | 495.0mW |

- Fast access time and cycle time

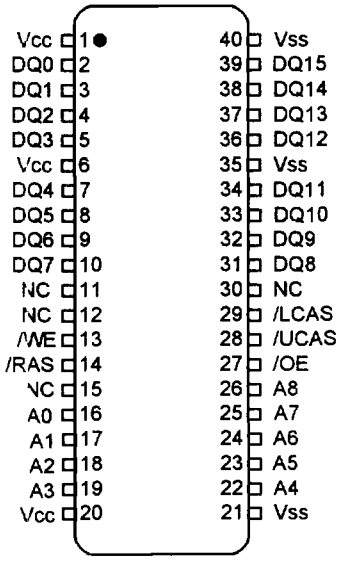
| Speed | tRAC | tCAC | tHPC |
|---|---|---|---|
| 50ns | 50ns | 15ns | 20ns |
| 60ns | 60ns | 17ns | 24ns |
| 70ns | 70ns | 20ns | 39ns |

- Extended Data Out Operation
- 2/CAS inputs for upper and lower byte control
- Single power supply of 5V ± 10%
- Read-Modify-Write Capability
- TTL compatible inputs and outputs
- /RAS-only, /CAS-before-/RAS,
  Hidden and Self Refresh Capability
- Refresh cycles
  512 refresh cycles / 8ms
  512 refresh cycles / 128ms (SL-part)
- JEDEC standard pinout
  40-pin SOJ (400 mil)
  40/44-pin TSOP-II (400 mil)

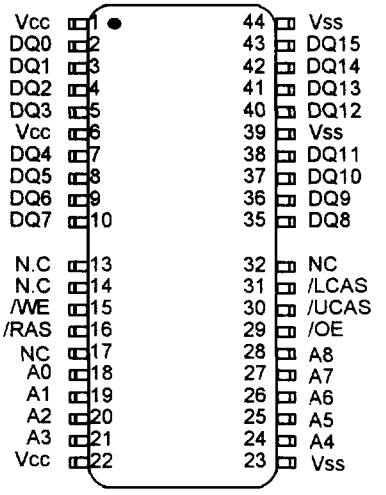
## BLOCK DIAGRAM



## PIN CONFIGURATION (Marking Side)




**40-pin Plastic SOJ(400mil)**




**40/44-pin Plastic TSOP-II (400mil)**

## PIN DESCRIPTION

| | |
|---|---|
| /RAS | Row Address Strobe |
| /CAS | Column Address Strobe |
| /WE | Write Enable |
| /OE | Output Enable |
| A0-A8 | Address Input |
| DQ0-DQ15 | Data In/Out |
| VCC | Power (5V) |
| VSS | Ground |
| NC | No Connection |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Ambient Temperature | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature | -55 to 150 | °C |
| $V_{IN}$, $V_{OUT}$ | Voltage on Any Pin relative to Vss | -1.0 to 7.0 | V |
| $V_{CC}$ | Voltage on Vcc relative to Vss | -1.0 to 7.0 | V |
| $I_{OS}$ | Short Circuit Output Current | 50 | mA |
| $P_D$ | Power Dissipation | 0.90 | W |
| $T_{SOLDER}$ | Soldering Temperature · Time | 260 · 10 | °C · sec |

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.



## RECOMMENDED DC OPERATING CONDITIONS

($T_A$=0 °C to 70 °C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.4 | - | $V_{CC}$+1.0 | V |
| $V_{IL}$ | Input Low Voltage | -1.3 | - | 0.8 | V |

Note: All voltages are referenced to Vss.

## DC CHARACTERISTICS

($T_A$=0 °C to 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Speed / Power | Min. | Max. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage current (Any Input Pins) | Vss ≤ $V_{IN}$ ≤ Vcc + 1.0, All other pins not under test = Vss | | -10 | 10 | uA | |
| $I_{LO}$ | Output Leakage current (High Impedance State) | Vss ≤ $V_{OUT}$ ≤ Vcc, /RAS & /CAS at $V_{IH}$ | | -10 | 10 | uA | |
| $I_{CC1}$ | Vcc Supply Current, Operating | tRC=tRC (min.) | 50<br>60<br>70 | -<br>-<br>- | 110<br>100<br>90 | mA | 1,2,3,7 |
| $I_{CC2}$ | Vcc Supply Current, TTL Standby | /RAS & /CAS at $V_{IH}$(min.) other inputs ≥ Vss | | - | 2 | mA | |
| $I_{CC3}$ | Vcc Supply Current, /RAS-only Refresh | tRC=tRC (min.) | 50<br>60<br>70 | - | 110<br>100<br>90 | mA | 1,3,7 |
| $I_{CC4}$ | Vcc Supply Current, EDO Mode | tPC=tPC (min.) | 50<br>60<br>70 | - | 110<br>100<br>90 | mA | 1,2,3,7 |
| $I_{CC5}$ | Vcc Supply Current, CMOS Standby | /RAS & /CAS ≥ Vcc - 0.2V | <br>L-part | - | 1<br>200 | mA<br>uA | 5 |
| $I_{CC6}$ | Vcc Supply Current, /CAS-before-/RAS Refresh | tRC=tRC (min.) | 50<br>60<br>70 | - | 120<br>110<br>100 | mA | 1,3,7 |
| $I_{CC7}$ | Vcc Supply Current Battery Back Up (L-part only) | tRC= 125us, tRAS ≤ 1us<br>/CAS = CBR cycling or 0.2V<br>/WE = Vcc - 0.2 V<br>A0-8 = Vcc - 0.2 V, or 0.2 V<br>DQ0-DQ15 = 0.2,<br>Vcc - 0.2 V, or open | | - | 400 | uA | 1,4,5 |
| $I_{CC8}$ | Vcc supply Current, Self Refresh (SL-part only) | /RAS & /CAS ≤ 0.2V<br>other pins same as $I_{CC7}$ | | | 400 | uA | 6 |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= 4.2mA | | - | 0.4 | V | |
| $V_{IH}$ | Output High Voltage | $I_{OH}$ = -5mA | | 2.4 | - | V | |

NOTE

1. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC6}$, and $I_{CC7}$ depend on cycle rates.
2. Icc1, Icc3, Icc4 and Icc6 are dependent on output loading. Specified values are obtained with the output open.
3. Icc is specified as an average current. In Icc1, Icc3, Icc6, Address can be changed maximum two times while /RAS=VIL. In Icc4, Address can be changed maximum once while /CAS=$V_{IH}$.
4. Only tRAS(max.) = 1us is applied to refresh of battery backup but tRAS(max.) = 10us is to applied to normal functional operation.
5. Icc5(max.)=200uA,Icc7 and Icc8 are applied to L-part.
6. Operating condition for 50ns part is Vcc = 5V ± 5%, Cout= 30 pF.

## AC CHARACTERISTICS

($T_A$=0 °C to 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.)

| # | SYMBOL | PARAMETER | HY512264 Series | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -50 | | -60 | | -70 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 1 | tRC | Random Read or Write Cycle Time | 84 | - | 104 | - | 124 | - | ns | |
| 2 | tRWC | Read-Modify-Write Cycle Time | 120 | - | 140 | - | 170 | - | ns | |
| 3 | tHPC | EDO Mode Cycle Time | 20 | - | 24 | - | 29 | - | ns | |
| 4 | tPRWC | EDOMode Read-Modify-Write Cycle Time | 61 | - | 68 | - | 83 | - | ns | |
| 5 | tRAC | Access Time from /RAS | - | 50 | - | 60 | - | 70 | ns | 4,9,10 |
| 6 | tCAC | Access Time from /CAS | - | 15 | - | 17 | - | 20 | ns | 4,9 |
| 7 | tAA | Access Time from Column Address | - | 25 | - | 30 | - | 35 | ns | 4,10 |
| 8 | tCPA | Access Time from Column Precharge | - | 30 | - | 35 | - | 40 | ns | 4,15 |
| 9 | tCLZ | /CAS to Output Low Impedance | 0 | - | 0 | - | 0 | - | ns | 4 |
| 10 | tDOH | Output Data Hold Time | 5 | - | 5 | - | 5 | - | ns | 5 |
| 11 | tT | Transition Time (Rise and Fall) | 2 | 50 | 2 | 50 | 2 | 50 | ns | 3 |
| 12 | tRP | /RAS Precharge Time | 30 | - | 40 | - | 50 | - | ns | |
| 13 | tRAS | /RAS Pulse Width | 50 | 10K | 60 | 10K | 70 | 10K | ns | |
| 14 | tRASP | /RAS Pulse Width (EDOMode) | 50 | 100k | 60 | 100k | 70 | 100k | ns | |
| 15 | tRSH | /RAS Hold Time | 15 | - | 15 | - | 20 | - | ns | |
| 16 | tCSH | /CAS Hold Time | 45 | - | 55 | - | 65 | - | ns | |
| 17 | tCAS | /CAS Pulse Width | 8 | 10K | 10 | 10K | 15 | 10K | ns | |
| 18 | tRCD | /RAS to /CAS Delay Time | 15 | 37 | 20 | 45 | 20 | 50 | ns | 9 |
| 19 | tRAD | /RAS to Column Address Delay Time | 10 | 25 | 15 | 30 | 15 | 35 | ns | 10 |
| 20 | tCRP | /CAS to /RAS Precharge Time | 5 | - | 5 | - | 5 | - | ns | |
| 21 | tCP | /CAS Precharge Time | 8 | - | 10 | - | 10 | - | ns | |
| 22 | tASR | Row Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 23 | tRAH | Row Address Hold Time | 8 | - | 10 | - | 10 | - | ns | |
| 24 | tASC | Column Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | 14 |
| 25 | tCAH | Column Address Hold Time | 8 | - | 10 | - | 15 | - | ns | |
| 26 | tAR | Column Address Hold Time from /RAS | 45 | - | 50 | - | 55 | - | ns | |
| 27 | tRAL | Column Address to /RAS Lead Time | 25 | - | 30 | - | 35 | - | ns | |
| 28 | tRCS | Read Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 29 | tRCH | Read Command Hold Time Referenced to /CAS | 0 | - | 0 | - | 0 | - | ns | 6 |
| 30 | tRRH | Read Command Hold Time Referenced to /RAS | 0 | - | 0 | - | 0 | - | ns | 6 |
| 31 | tWCH | Write Command Hold Time | 10 | - | 10 | - | 10 | - | ns | |
| 32 | tWCR | Write Command Hold Time from /RAS | 40 | - | 50 | - | 55 | - | ns | |
| 33 | tWP | Write Command Pulse Width | 10 | - | 10 | - | 10 | - | ns | |
| 34 | tRWL | Write Command to /RAS Lead Time | 15 | - | 15 | - | 20 | - | ns | |
| 35 | tCWL | Write Command to /CAS Lead Time | 8 | - | 10 | - | 15 | - | ns | |
| 36 | tDS | Data-In Set-up Time | 0 | - | 0 | - | 0 | - | ns | 7 |
| 37 | tDH | Data-In Hold Time | 10 | - | 10 | - | 15 | - | ns | 7 |
| 38 | tDHR | Data-In Hold Time Referenced to /RAS | 40 | - | 50 | - | 55 | - | ns | |
| 39 | tREF | Refresh Period (512 cycles)<br>Refresh Period (L-part) | 8<br>128 | - | 8<br>128 | - | 8<br>128 | - | ms | 11 |

## AC CHARACTERISTICS

(Continued)

| # | SYMBOL | PARAMETER | HY512264 | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -50 | | -60 | | -70 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 40 | tWCS | Write Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | 8 |
| 41 | tCWD | /CAS to /WE Delay Time | 34 | - | 36 | - | 44 | - | ns | 8 |
| 42 | tRWD | /RAS to /WE Delay Time | 69 | - | 79 | - | 94 | - | ns | 8 |
| 43 | tAWD | Column Address to /WE Delay Time | 44 | - | 49 | - | 59 | - | ns | 8 |
| 44 | tCSR | /CAS Set-up Time (CBR Cycle) | 5 | - | 5 | - | 5 | | ns | |
| 45 | tCHR | /CAS Hold Time (CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 46 | tRPC | /RAS to /CAS Precharge Time | 5 | - | 5 | - | 5 | - | ns | |
| 47 | tCPT | /CAS Precharge Time (CBR Counter) | 25 | - | 30 | - | 35 | - | ns | |
| 48 | tROH | /RAS Hold Time Reference to /OE | 0 | - | 0 | - | 0 | - | ns | |
| 49 | tOEA | /OE Access Time | - | 15 | - | 15 | - | 20 | ns | |
| 50 | tOED | /OE to Data Delay Time | 15 | - | 15 | - | 20 | - | ns | |
| 51 | tOEZ | Output Buffer turn Off Delay Time from /OE | 0 | 15 | 0 | 15 | 0 | 20 | ns | 5 |
| 52 | tOEH | /OE Command Hold Time | 15 | - | 15 | - | 20 | - | ns | |
| 53 | tCPWD | /WE Delay Time from /CAS Precharge | 49 | - | 54 | - | 64 | - | ns | 8 |
| 54 | tRHCP | /RAS Hold Time from /CAS Precharge | 30 | - | 35 | - | 40 | - | ns | |
| 55 | tRASS | /RAS Pulse Width (Self Refresh) | 100 | - | 100 | - | 100 | - | ns | |
| 56 | tRPS | /RAS Precharge Time(Self Refresh) | 100 | - | 100 | - | 100 | - | ns | |
| 57 | tCHS | /CAS Hold Time from /RAS(Self Refresh) | -50 | - | -50 | - | -50 | - | ns | |
| 58 | tOCH | /OE to /CAS Hold Time | 0 | - | 0 | - | 0 | - | ns | |
| 59 | tCHO | /CAS Precharge to /OE Precharge time | 10 | - | 10 | - | 10 | - | ns | |
| 60 | tOEP | /OE Pulse Width | 10 | - | 10 | - | 10 | - | ns | |
| 61 | tREZ | Output Buffer Turn off Delay from /RAS | 0 | 15 | 0 | 15 | 0 | 15 | ns | |
| 62 | tWEZ | Output Buffer Turn off Delay from /WE | 0 | 15 | 0 | 15 | 0 | 15 | ns | |
| 63 | tCEZ | Output Buffer Turn off Delay from /CAS | 0 | 15 | 0 | 15 | 0 | 15 | ns | |

NOTE

1. An initial pause of 200us is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up, the HY512264 could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min.) and $V_{IL}$(max.), and are assumed to be 2ns for all inputs.
4. Measured at $V_{OH}$=2.0V and $V_{OL}$=0.8V with a load equivalent to 2 TTL loads and 100pF for 60ns, 70ns part and measured at $V_{OH}$=2.0V and $V_{OL}$=0.8V with a load equivalent to 2 TTL loads and 30pF for 50ns.
5. tCEZ(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to /LCAS and /UCAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles and lately Write cycle.
8. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters.They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD ≥ tRWD(min.), tCWD ≥ tCWD(min.), tAWD ≥ tAWD(min.), and tCPWD ≥ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met.tRCD(max.) is specified as a reference point only.If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA$V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min.) and $V_{IL}$(max.).
11. tREF(max.)=128ms is applied to L-parts and SL-parts.
12. A burst of 512 /CAS-before-/RAS refresh cycles must be excuted within 8ms (128ms for SL-parts) after exciting self refresh
13. When both /LCAS and /UCAS go low at the same time, all 16-bits data are written into the device. /LCAS and /UCAS must be transited simultaneously whithin a same time read or write cycle.
14. These parameters are determined by the earlier falling edge of /LCAS or /UCAS.
15. These parameters are determined by the later rising edge of /LCAS or /UCAS.
16. tCWL must be satisfied by both /LCAS and /UCAS for 16-bits access cycles.
17. tCP and tCPT are measured when both /LCAS and /UCAS are high state.
18. Operating condition for 50ns part is Vcc=5V ± 5%, Cout=30pF.

## CAPACITANCE

($T_A$=0 °C to 70 °C, Vcc=5V ± 10%, Vss=0V, f = 1MHz, unless otherwise noted.)

| SYMBOL | PARAMETER | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN1}$ | Input Capacitance (A0 - A8) | - | 5 | pF |
| $C_{IN2}$ | Input Capacitance (/RAS, /CAS, /WE, /OE) | - | 7 | pF |
| $C_{DQ}$ | Data Input /Output Capacitance(DQ0 - DQ15) | - | 7 | pF |