Preliminary TOSHIBA CMOS Integrated Circuit Silicon Monolithic

T 6 K 4 4

Common Driver for Displaying Simple Dot Matrices

T6K44 is a common driver for displaying simple dot matrices. This common driver has 168 outputs and includes a power supply circuit with an electronic volume. An LCD system with a single power supply can be implemented by combining this common driver with segment driver S6B0023. Because this common driver has the built-in power supply circuit, there is no need to obtain a power supply IC for the system implementation.

Unit: mm

T6K44	User Area Pitch	
	IN	OUT

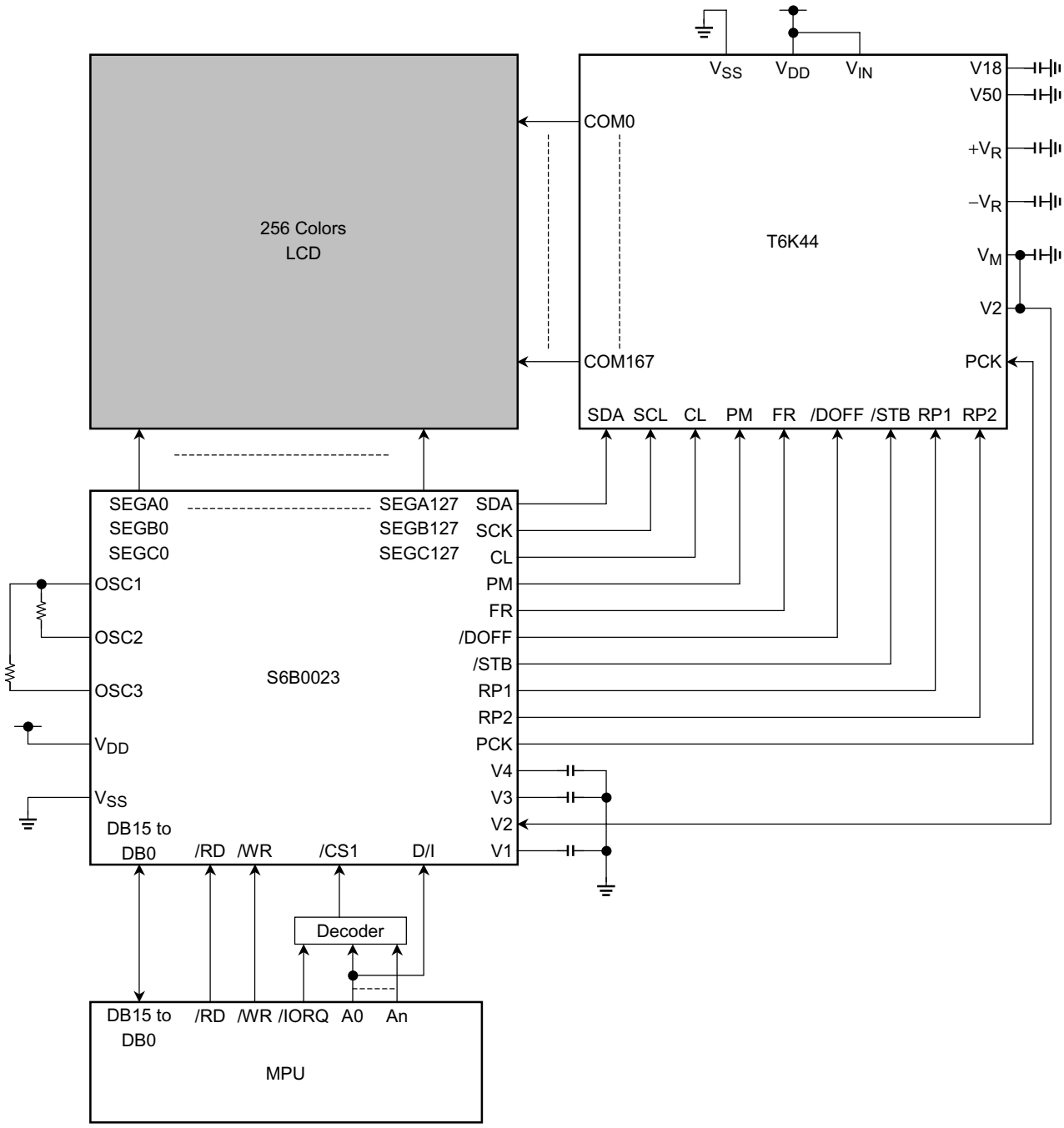
For the latest information about our TCP specifications and product portfolio, contact a Toshiba representative.

TCP (tape carrier package)

Features

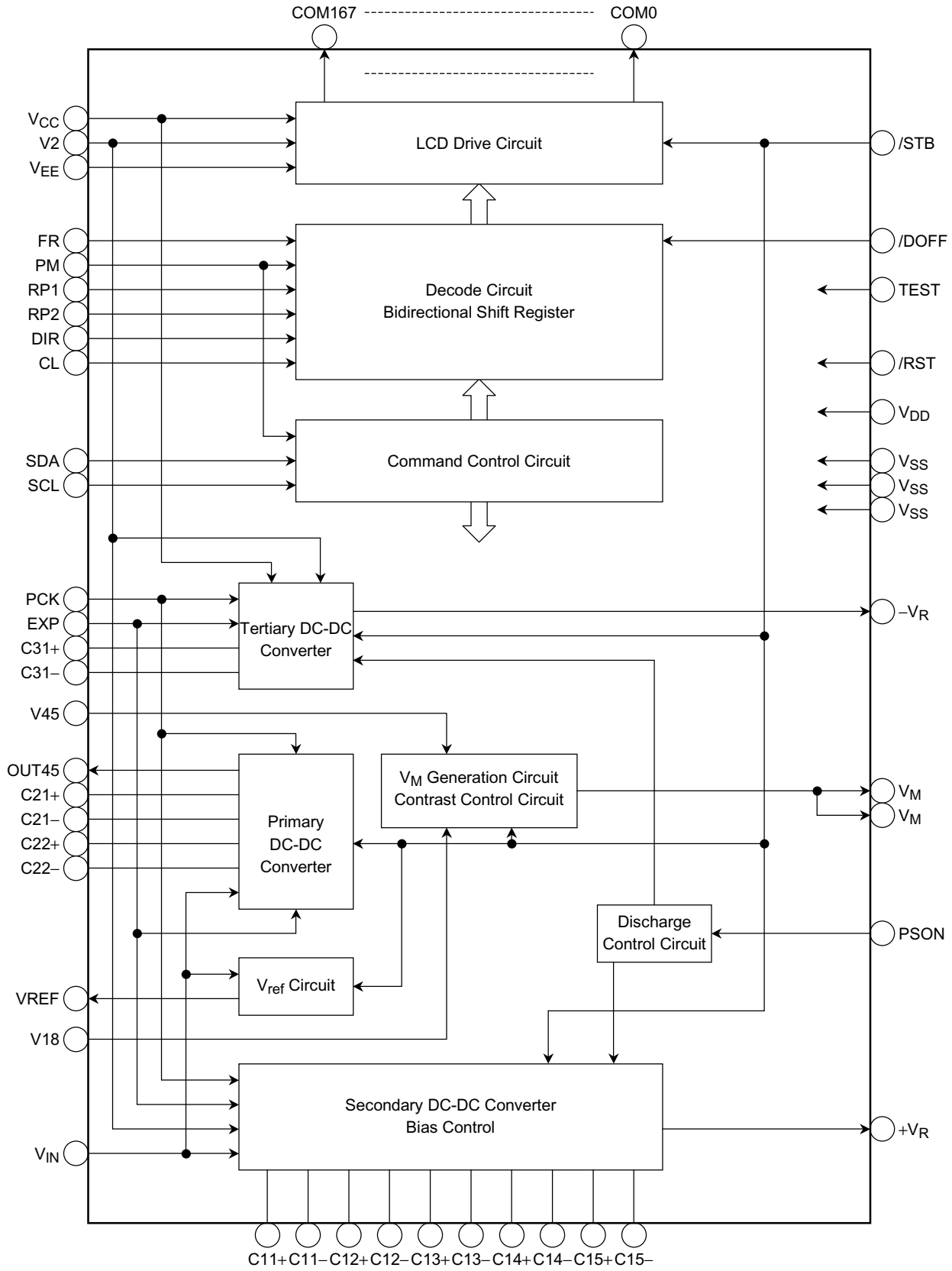
- Number of driver outputs : 168
- Operating voltage : V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V
  (*$V_{DD} \leqq V_{IN}$)
- LCD operating voltage : 28.8 V, max
- DC-DC converter : $V_{IN} \times 6$, max
- Contrast control : 256 steps, max
- Suitability to the partial display modes
- CMOS process
- Surrounding devices : Bump chip (COF), TCP
- Low power dissipation : I_{SS} = 100 μA (typ.) (design target value)
  Usage Conditions
  $V_{DD} = V_{IN}$ = 3.0 V, 5 × boost ON, 1/160 duty, 1/8 bias, Contrast = 7Fh, PCK = 5 kHz, No LCD load, Ta = 25°C
- Regulator output temperature inclination : 0.0%/°C (typ.) ±0.04%/°C

Example Configuration of the System



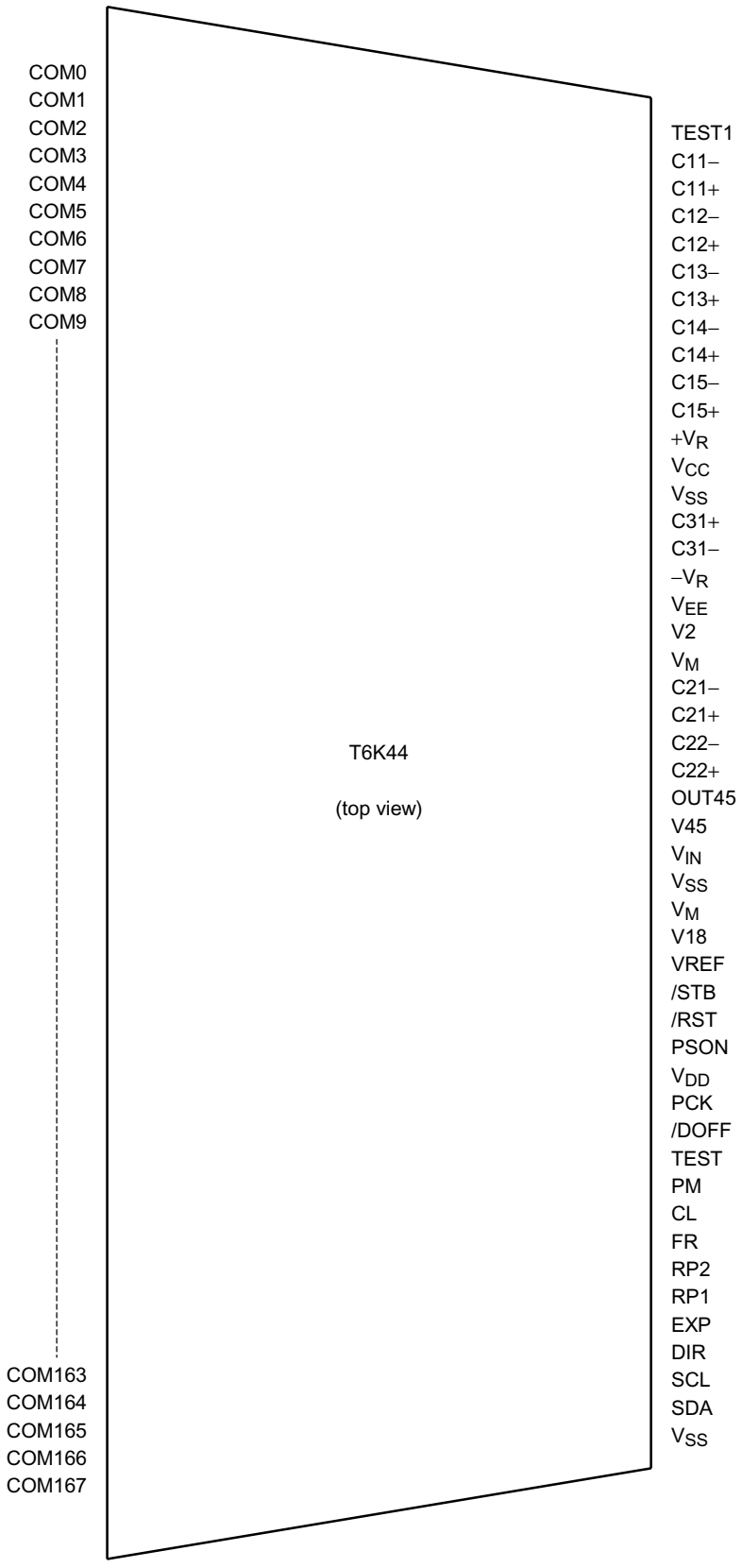
Note 1: For details about the power supply connection, see pages 10 through 13.

Block Diagram



Note 2: The figure above does not show the actual PAD arrangement.

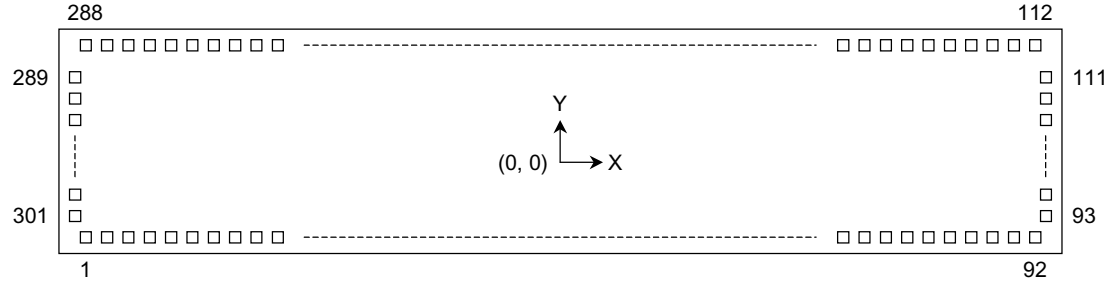
Pin Arrangement Diagram



Note 3: The figure above shows only the function terminals.

Chip Configuration

- Chip size 14600 × 2700 [μm]
- Pad layout



- Pad center coordinates [unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY1	–6935	–1210	31	DUMMY5	–4530	–1210	61	OUT45	1128	–1210
2	DUMMY2	–6850	–1210	32	DUMMY6	–4450	–1210	62	C22+	1354	–1210
3	DUMMY3	–6770	–1210	33	V_{SS}	–4226	–1210	63	C22–	1542	–1210
4	FUSE11	–6690	–1210	34	SDA	–4005	–1210	64	C21+	1768	–1210
5	FUSE12	–6610	–1210	35	SCK	–3817	–1210	65	C21–	1956	–1210
6	FUSE1G	–6530	–1210	36	DIR	–3591	–1210	66	DUMMY12	2129	–1210
7	FUSE13	–6450	–1210	37	EXP	–3403	–1210	67	V_M	2302	–1210
8	FUSE14	–6370	–1210	38	RP1	–3177	–1210	68	V2	2490	–1210
9	FUSE31	–6290	–1210	39	RP2	–2989	–1210	69	DUMMY13	2659	–1210
10	FUSE32	–6210	–1210	40	FR	–2763	–1210	70	DUMMY14	2838	–1210
11	FUSE33	–6130	–1210	41	CL	–2575	–1210	71	V_{EE}	3004	–1210
12	FUSE3G	–6050	–1210	42	PM	–2349	–1210	72	$-V_R$	3210	–1210
13	FUSE34	–5970	–1210	43	TEST	–2161	–1210	73	C31–	3401	–1210
14	FUSE35	–5890	–1210	44	/DOFF	–1935	–1210	74	C31+	3612	–1210
15	FUSE36	–5810	–1210	45	PCK	–1747	–1210	75	V_{SS}	3803	–1210
16	FUSE41	–5730	–1210	46	V_{DD}	–1571	–1210	76	DUMMY15	4014	–1210
17	FUSE42	–5650	–1210	47	PSON	–1383	–1210	77	V_{CC}	4205	–1210
18	FUSE43	–5570	–1210	48	/RST	–1157	–1210	78	$+V_R$	4416	–1210
19	FUSE4G	–5490	–1210	49	/STB	–969	–1210	79	C15+	4607	–1210
20	FUSE44	–5410	–1210	50	DUMMY7	–770	–1210	80	C15–	4818	–1210
21	FUSE45	–5330	–1210	51	DUMMY8	–650	–1210	81	C14+	5009	–1210
22	FUSE46	–5250	–1210	52	DUMMY9	–530	–1210	82	C14–	5220	–1210
23	FUSE51	–5170	–1210	53	DUMMY10	–380	–1210	83	C13+	5411	–1210
24	FUSE52	–5090	–1210	54	DUMMY11	–230	–1210	84	C13–	5622	–1210
25	FUSE53	–5010	–1210	55	VREF1	–57	–1210	85	C12+	5813	–1210
26	FUSE5G	–4930	–1210	56	V18	131	–1210	86	C12–	6024	–1210
27	FUSE54	–4850	–1210	57	V_M	357	–1210	87	C11+	6215	–1210
28	FUSE55	–4770	–1210	58	GND	508	–1210	88	C11–	6426	–1210
29	FUSE56	–4690	–1210	59	V_{IN}	731	–1210	89	TEST1	6617	–1210
30	DUMMY4	–4610	–1210	60	V45	937	–1210	90	DUMMY16	6839	–1210

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
91	DUMMY17	6939	−1210	136	COM21	5210	1155	181	COM66	1610	1155
92	DUMMY18	7024	−1210	137	COM22	5130	1155	182	COM67	1530	1155
93	DUMMY19	7145	−1030	138	COM23	5050	1155	183	COM68	1450	1155
94	DUMMY20	7145	−945	139	COM24	4970	1155	184	COM69	1370	1155
95	DUMMY21	7145	−865	140	COM25	4890	1155	185	COM70	1290	1155
96	DUMMY22	7145	−785	141	COM26	4810	1155	186	COM71	1210	1155
97	ENTEG4	7145	−603	142	COM27	4730	1155	187	COM72	1130	1155
98	ENTEG3	7145	−412	143	COM28	4650	1155	188	COM73	1050	1155
99	ENTEG2	7145	−201	144	COM29	4570	1155	189	COM74	970	1155
100	ENTEG1	7145	−10	145	COM30	4490	1155	190	COM75	890	1155
101	DUMMY23	7145	175	146	COM31	4410	1155	191	COM76	810	1155
102	DUMMY24	7145	255	147	COM32	4330	1155	192	COM77	730	1155
103	DUMMY25	7145	335	148	COM33	4250	1155	193	COM78	650	1155
104	DUMMY26	7145	415	149	COM34	4170	1155	194	COM79	570	1155
105	DUMMY27	7145	495	150	COM35	4090	1155	195	COM80	490	1155
106	DUMMY28	7145	575	151	COM36	4010	1155	196	COM81	410	1155
107	DUMMY29	7145	655	152	COM37	3930	1155	197	COM82	330	1155
108	DUMMY30	7145	735	153	COM38	3850	1155	198	COM83	250	1155
109	DUMMY31	7145	815	154	COM39	3770	1155	199	DUMMY37	100	1155
110	DUMMY32	7145	895	155	COM40	3690	1155	200	DUMMY38	0	1155
111	DUMMY33	7145	980	156	COM41	3610	1155	201	DUMMY39	−100	1155
112	DUMMY34	7135	1155	157	COM42	3530	1155	202	COM84	−250	1155
113	DUMMY35	7050	1155	158	COM43	3450	1155	203	COM85	−330	1155
114	DUMMY36	6970	1155	159	COM44	3370	1155	204	COM86	−410	1155
115	COM0	6890	1155	160	COM45	3290	1155	205	COM87	−490	1155
116	COM1	6810	1155	161	COM46	3210	1155	206	COM88	−570	1155
117	COM2	6730	1155	162	COM47	3130	1155	207	COM89	−650	1155
118	COM3	6650	1155	163	COM48	3050	1155	208	COM90	−730	1155
119	COM4	6570	1155	164	COM49	2970	1155	209	COM91	−810	1155
120	COM5	6490	1155	165	COM50	2890	1155	210	COM92	−890	1155
121	COM6	6410	1155	166	COM51	2810	1155	211	COM93	−970	1155
122	COM7	6330	1155	167	COM52	2730	1155	212	COM94	−1050	1155
123	COM8	6250	1155	168	COM53	2650	1155	213	COM95	−1130	1155
124	COM9	6170	1155	169	COM54	2570	1155	214	COM96	−1210	1155
125	COM10	6090	1155	170	COM55	2490	1155	215	COM97	−1290	1155
126	COM11	6010	1155	171	COM56	2410	1155	216	COM98	−1370	1155
127	COM12	5930	1155	172	COM57	2330	1155	217	COM99	−1450	1155
128	COM13	5850	1155	173	COM58	2250	1155	218	COM100	−1530	1155
129	COM14	5770	1155	174	COM59	2170	1155	219	COM101	−1610	1155
130	COM15	5690	1155	175	COM60	2090	1155	220	COM102	−1690	1155
131	COM16	5610	1155	176	COM61	2010	1155	221	COM103	−1770	1155
132	COM17	5530	1155	177	COM62	1930	1155	222	COM104	−1850	1155
133	COM18	5450	1155	178	COM63	1850	1155	223	COM105	−1930	1155
134	COM19	5370	1155	179	COM64	1770	1155	224	COM106	−2010	1155
135	COM20	5290	1155	180	COM65	1690	1155	225	COM107	−2090	1155

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
226	COM108	−2170	1155	252	COM134	−4250	1155	278	COM160	−6330	1155
227	COM109	−2250	1155	253	COM135	−4330	1155	279	COM161	−6410	1155
228	COM110	−2330	1155	254	COM136	−4410	1155	280	COM162	−6490	1155
229	COM111	−2410	1155	255	COM137	−4490	1155	281	COM163	−6570	1155
230	COM112	−2490	1155	256	COM138	−4570	1155	282	COM164	−6650	1155
231	COM113	−2570	1155	257	COM139	−4650	1155	283	COM165	−6730	1155
232	COM114	−2650	1155	258	COM140	−4730	1155	284	COM166	−6810	1155
233	COM115	−2730	1155	259	COM141	−4810	1155	285	COM167	−6890	1155
234	COM116	−2810	1155	260	COM142	−4890	1155	286	DUMMY40	−6970	1155
235	COM117	−2890	1155	261	COM143	−4970	1155	287	DUMMY41	−7050	1155
236	COM118	−2970	1155	262	COM144	−5050	1155	288	DUMMY42	−7135	1155
237	COM119	−3050	1155	263	COM145	−5130	1155	289	DUMMY43	−7145	980
238	COM120	−3130	1155	264	COM146	−5210	1155	290	DTEG1	−7145	790
239	COM121	−3210	1155	265	COM147	−5290	1155	291	DTEG3	−7145	599
240	COM122	−3290	1155	266	COM148	−5370	1155	292	DTEG2	−7145	388
241	COM123	−3370	1155	267	COM149	−5450	1155	293	DTEG4	−7145	197
242	COM124	−3450	1155	268	COM150	−5530	1155	294	ENTEG1	−7145	−15
243	COM125	−3530	1155	269	COM151	−5610	1155	295	ENTEG3	−7145	−206
244	COM126	−3610	1155	270	COM152	−5690	1155	296	ENTEG2	−7145	−417
245	COM127	−3690	1155	271	COM153	−5770	1155	297	ENTEG4	−7145	−608
246	COM128	−3770	1155	272	COM154	−5850	1155	298	DUMMY44	−7145	−785
247	COM129	−3850	1155	273	COM155	−5930	1155	299	DUMMY45	−7145	−865
248	COM130	−3930	1155	274	COM156	−6010	1155	300	DUMMY46	−7145	−945
249	COM131	−4010	1155	275	COM157	−6090	1155	301	DUMMY47	−7145	−1030
250	COM132	−4090	1155	276	COM158	−6170	1155				
251	COM133	−4170	1155	277	COM159	−6250	1155				

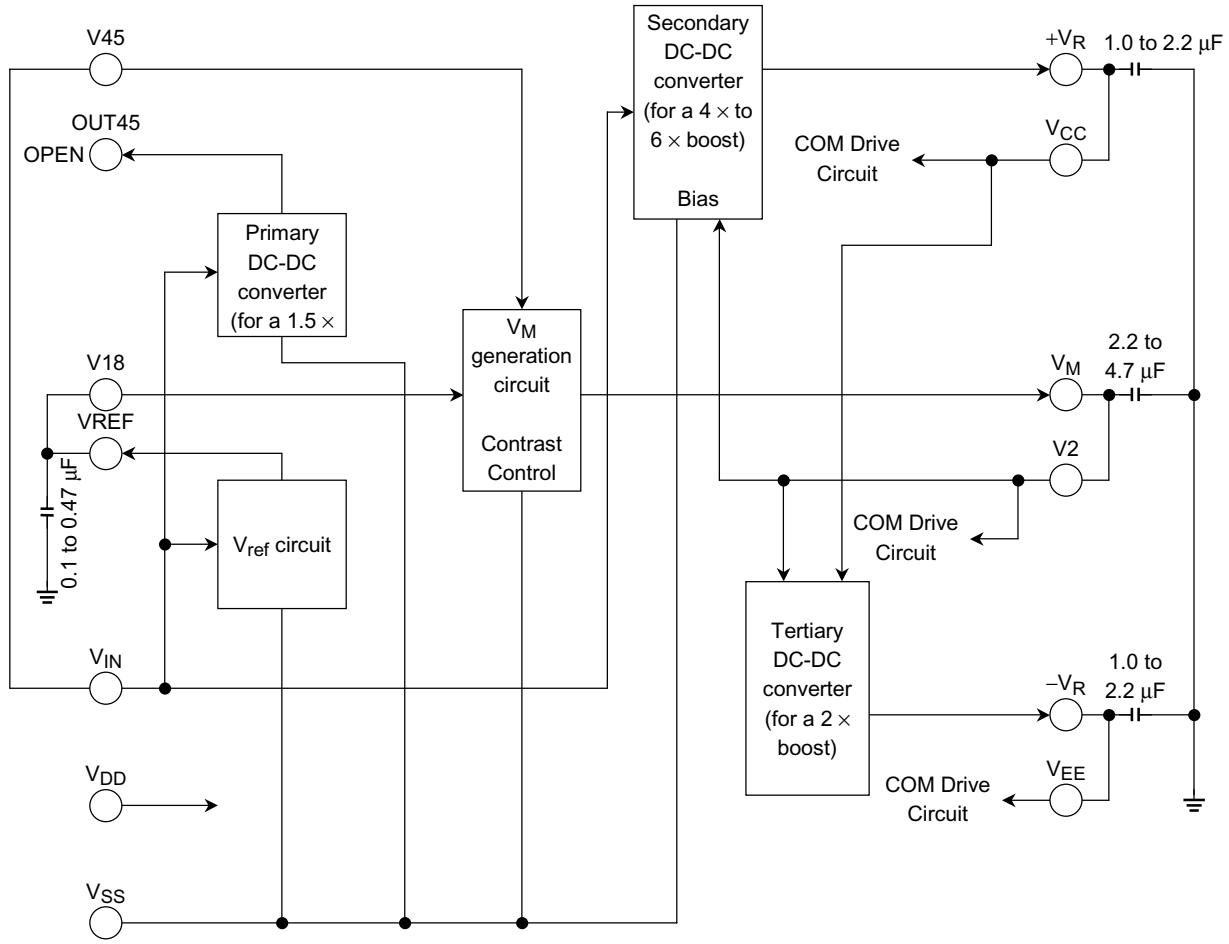
- Bump specifications

Item	Pad No.	Size	Unit
Pad pitch	33 to 89 (input)	150 (min)	μm
	115 to 285 (COM)	80 (min)	
	(NC, dummy, DTEG)	80 (min)	
Bump size	2-91, 94-110, 113-287, 290-300	65 × 65 (typ.) ±5	
	1, 92, 93, 111, 112, 288, 289, 301	70 × 65 (typ.) ±5	
Bump height	—	15 (typ.) ±2 (intra-chip: typ. ±2)	
Bump hardness	—	30 to 80	Hv
Bump strength (shearing rigidity)	—	20 (min)	gf

Terminal Description

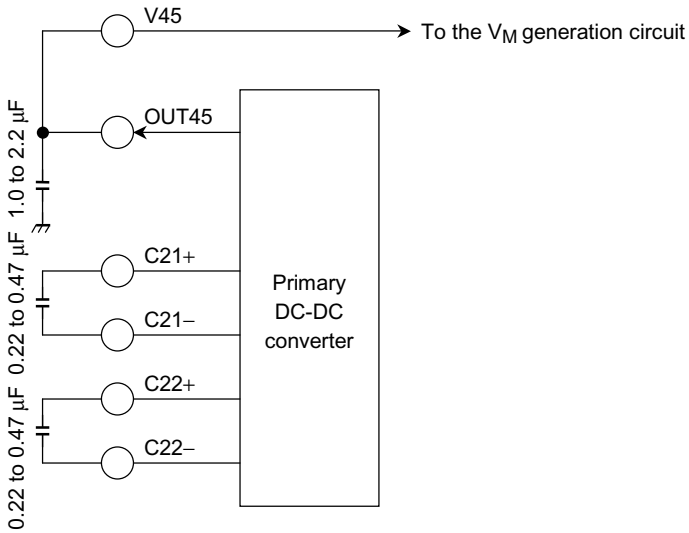
Terminal Name	I/O	Description
COM0 to COM167	O	Output terminal for common signals
/RST	I	Input terminal for reset signals
/STB	I	Input terminal for standby signals ・ This terminal should be normally connected to the /STB terminal for S6B0023. ・ T6K44 goes into the standby state while /STB = "L." The LCD drive signal is set at the V_{SS} level, stopping the boost.
/DOFF	I	Input terminal for display OFF signals ・ /DOFF = "H"・・・Produces normal COM output. ・ /DOFF = "L"・・・Produces all COM output at the V_M level.
CL	I	Input terminal for shift clock pulses
PM	I	Input terminal for frame signals
FR	I	Input terminal for AC generation signals for display
SDA. SCL	I	Command interface with the SEG driver (S6B0023)
RP1, RP2	I	Input terminal for row parameters
PCK	I	Input terminal for clock signals for a boost. Used to input 5 KHz (typ.) clock signals for a boost from the SEG driver.
DIR	I	Terminal for selecting a COM scan direction. DIR = 0: COM0 → COM167 DIR = 1: COM167 → COM0
EXP	I	Terminal for selecting a power supply mode EXP = 0: Selects the internal power supply circuit. EXP = 1: Selects the external power supply. (stops generation of V_{ref}, V_M, $+V_R$, and $-V_R$.)
PSON	I	Terminal for turning on/off the discharge function when switching the partial display 1 mode PSON = 0: Turns the function off. PSON = 1: Turns the function on.
V_M, $+V_R$, $-V_R$	—	Output terminal for LCD drive power supply
V2	—	Input terminal for the reference voltage (V_M). Connected to V2 for the SEG driver. <EXP = 0> <EXP = 1> V2: Connected to V_M Used for V_M-level external input.
V_{CC}, V_{EE}	—	Input terminal for LCD drive power supply <EXP = 0> <EXP = 1> V_{CC}: Connected to $+V_R$ Used for $+V_R$-level external input V_{EE}: Connected to $-V_R$ Used for $-V_R$-level external input
V_{IN}	—	Power supply terminal for a boost
V18	—	Terminal for V_{ref} connection
VREF	—	Output terminal for the Ref voltage (V_{ref})
OUT45	—	Output terminal for the primary boost voltage
V45	—	Input terminal for the primary boost voltage. Connected to the OUT45 terminal.
C21–, C21+ C22–, C22+	—	Terminals for connection to the external capacitor for a primary boost
C11–, C11+, C12–, C12+, C13–, C13+, C14–, C14+, C15–, C15+	—	Terminals for connection to the external capacitor for a secondary boost
C31–, C31+	—	Terminals for connection to the external capacitor for a tertiary boost
V_{DD}, V_{SS}	—	Power supply terminal
TEST, TEST1	—	Terminals for testing by Toshiba. Normally connected to V_{SS}.

Power Supply Circuit Block Diagram



Note 4: The figure above shows the circuits for $V_M \leqq V_{IN} - 0.2$ V.

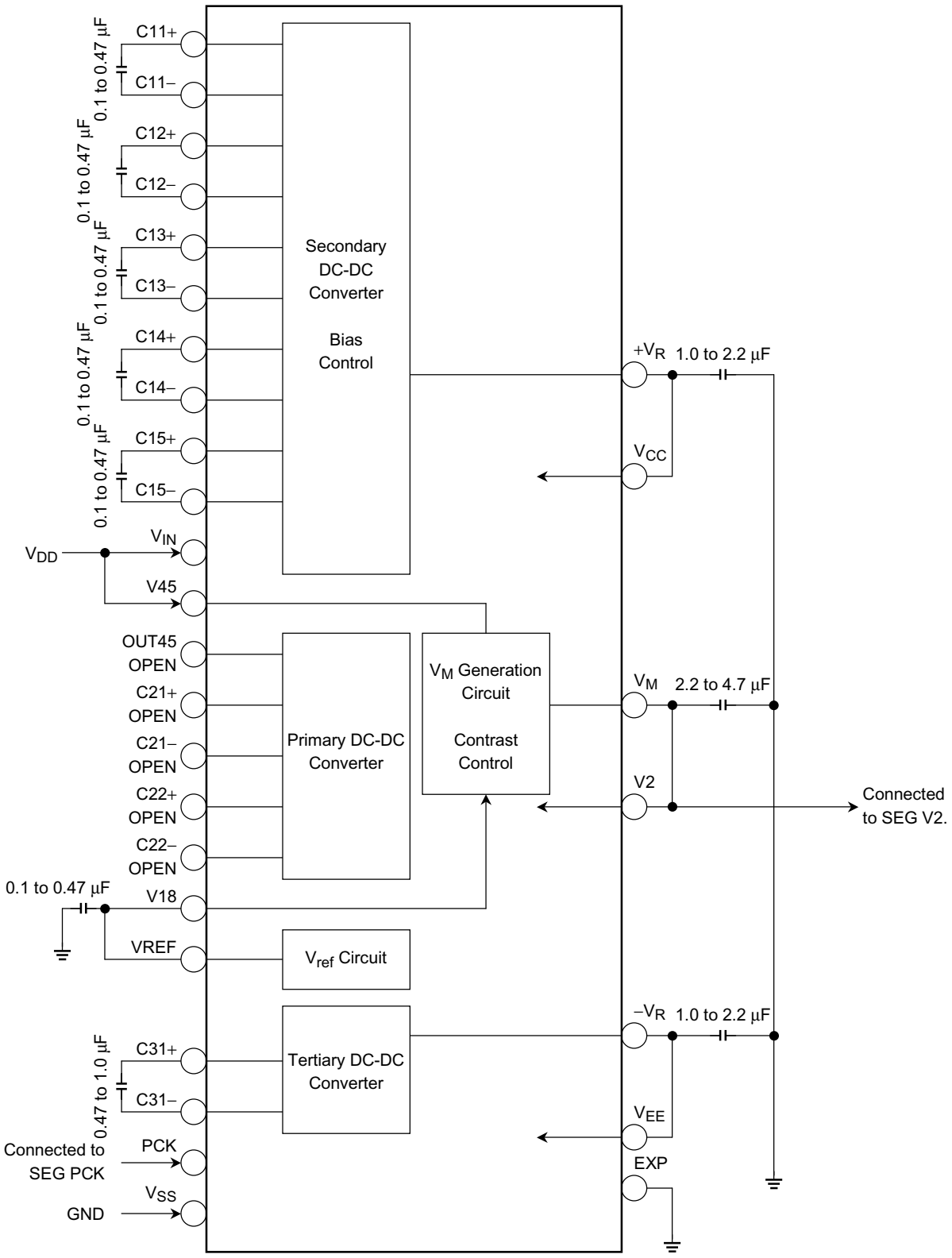
Note 5: If $V_M > V_{IN} - 0.2$ V, the primary boost terminal (OUT45) should be connected to the V45 terminal as shown in the figure below.



Example Connection of the Power Supply Circuit Components

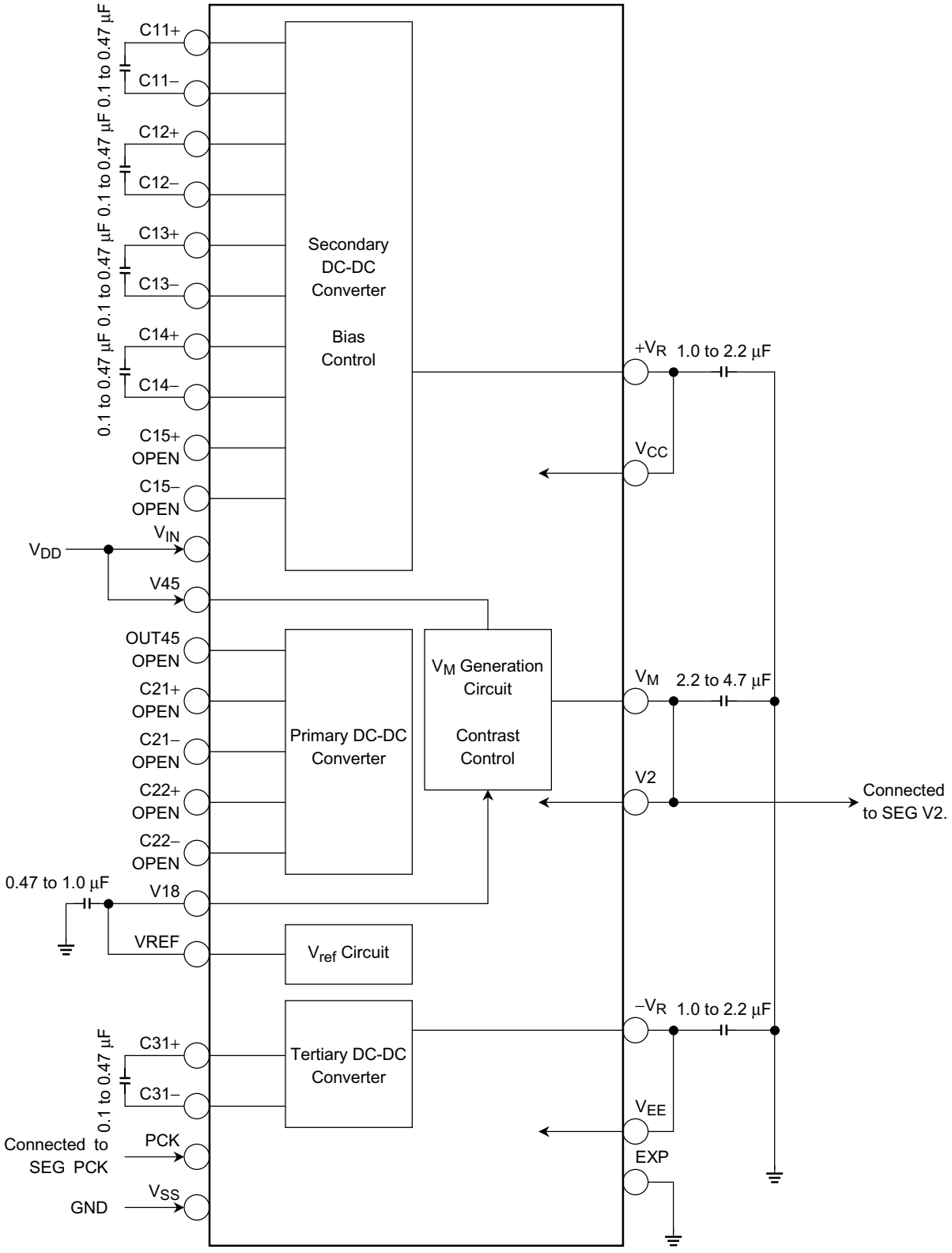
(1) Internal power supply mode (EXP = L) for (Note 6) $V_M \leqq V_{IN} - 0.2$ V

- For a 6 × boost



Note 6: Be sure to check the capacitance in the actual machine.

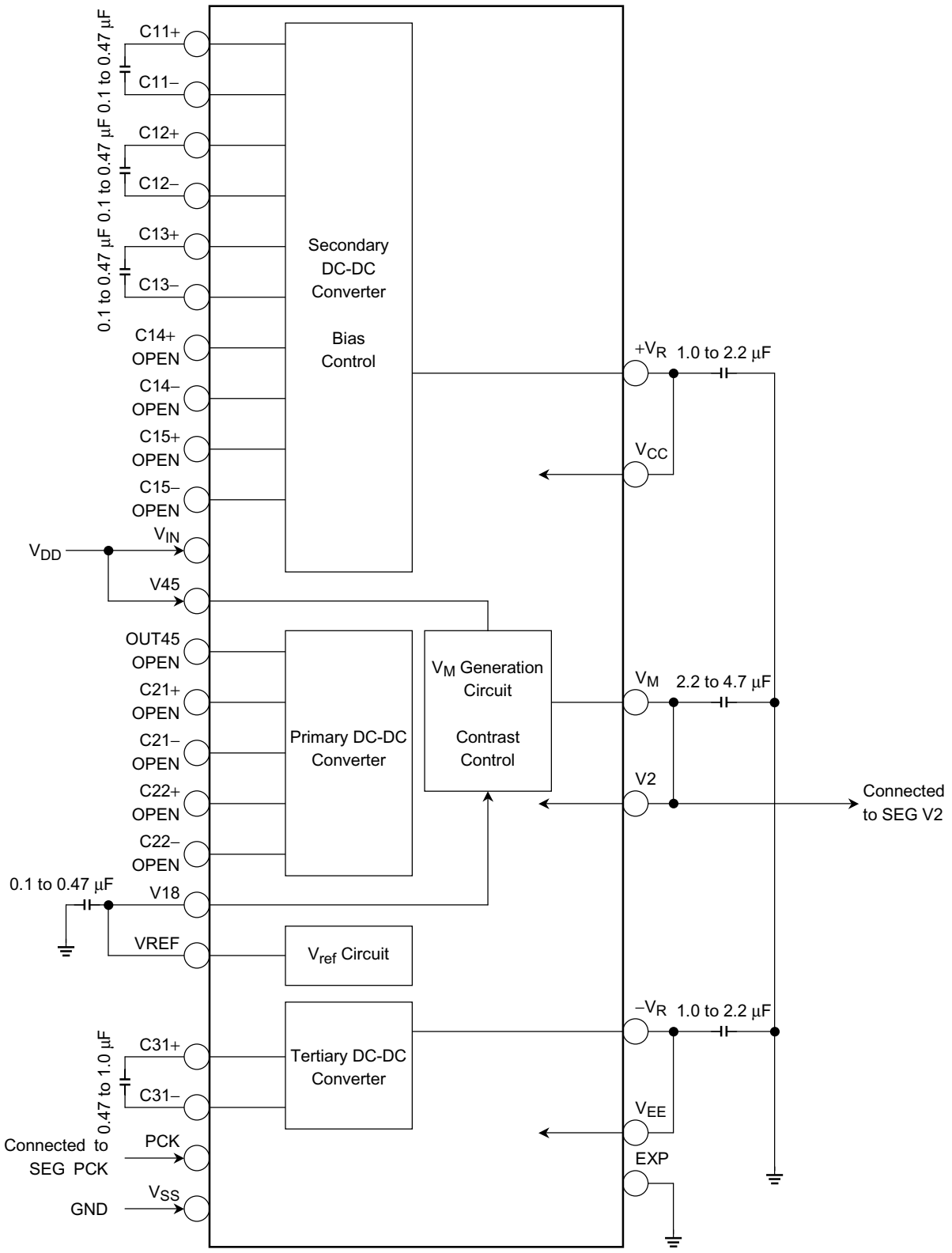
- For a 5 × boost



Note 7: Be sure to check the capacitance in the actual machine.

Note 8: For the circuits connected as shown above, do not specify the 6× boost in the command settings.

- For a 4 × boost



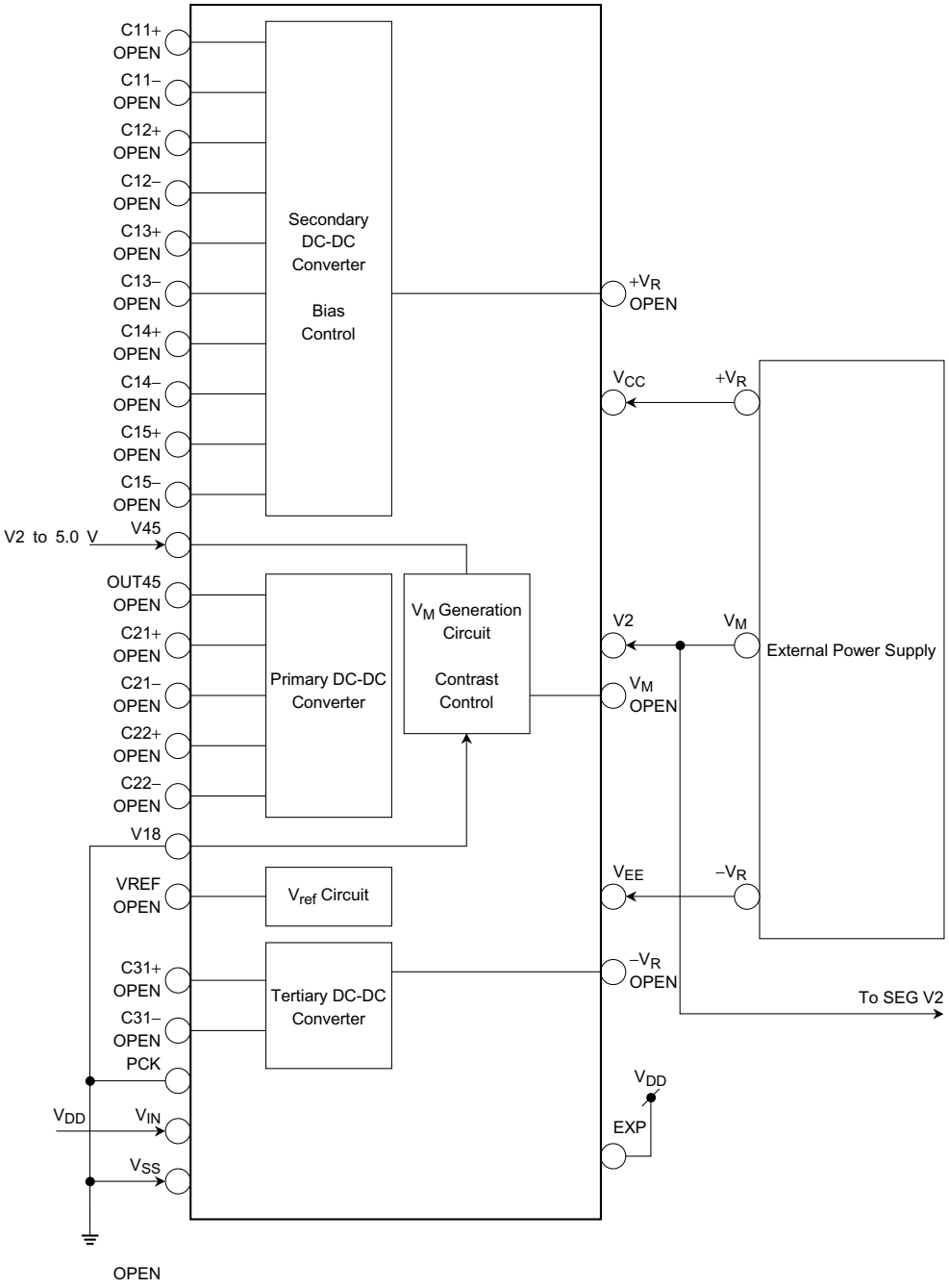
Note 9: Be sure to check the capacitance in the actual machine.

Note 10: For the circuits connected as shown above, do not specify the 6× or 5× boost in the command settings.

(2) External power supply mode (EXP = H)

If the EXP terminal is set to H for T6K44, a power supply unit for display can be installed outside of T6K44 and connected to it.

Example Connections for an External Power Supply Unit



If T6K44 operates in external power supply mode (EXP = H), the built-in power supply circuit in T6K44 goes into the following state:

- V_{ref} generation OFF
- Primary boost OFF
- V_M-AMP OFF
- Secondary/Tertiary boost OFF ($+V_R$/$-V_R$ OFF)
- V_M/$+V_R$/$-V_R$ output (OPEN)

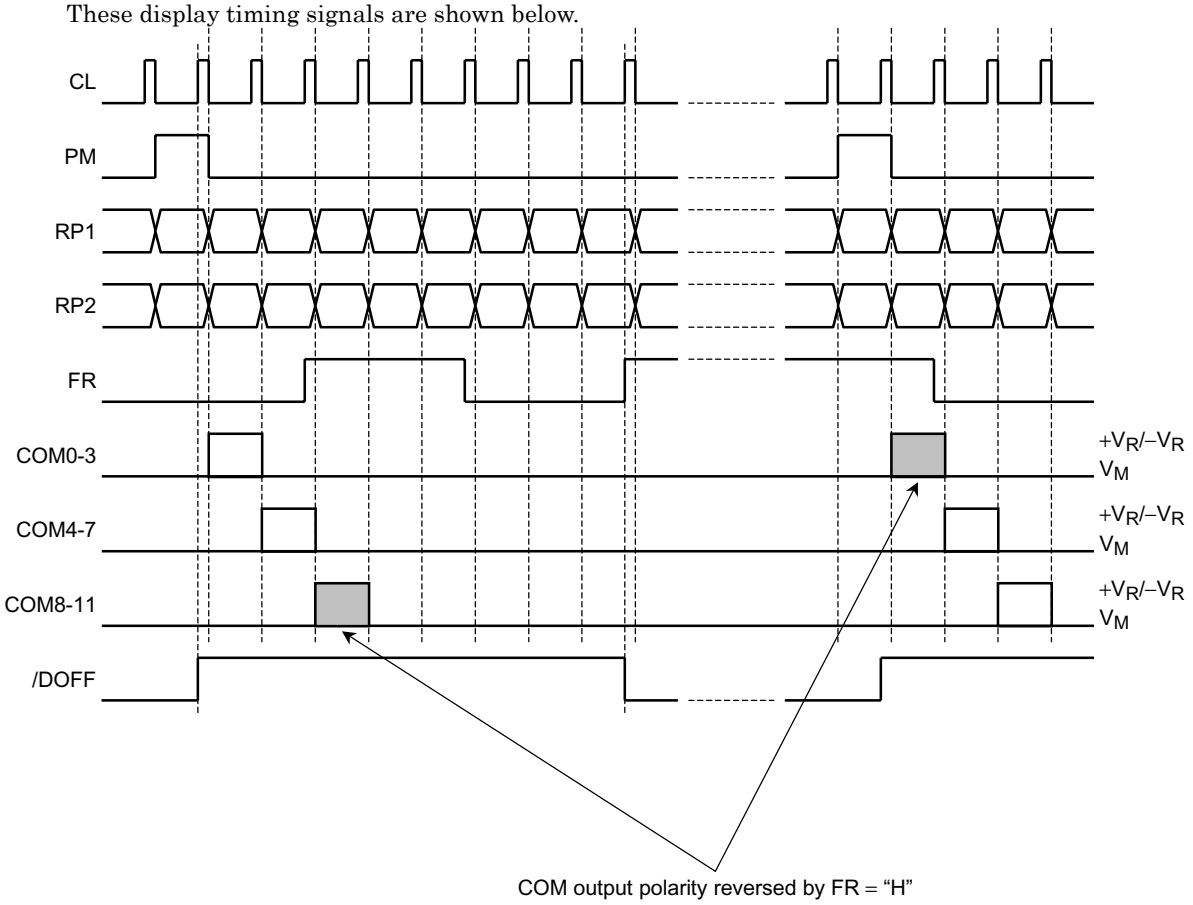
Therefore, Contrast Control and Bias Control should be controlled from the external power supply.

The V45 terminal should be used for an input voltage between V2 and 5.0 V.

Display Control Signals

T6K44 generates display waveform timing signals by using PM, FR, CL, RP1, and RP2 which are all supplied from the SEG driver (S6B0023).

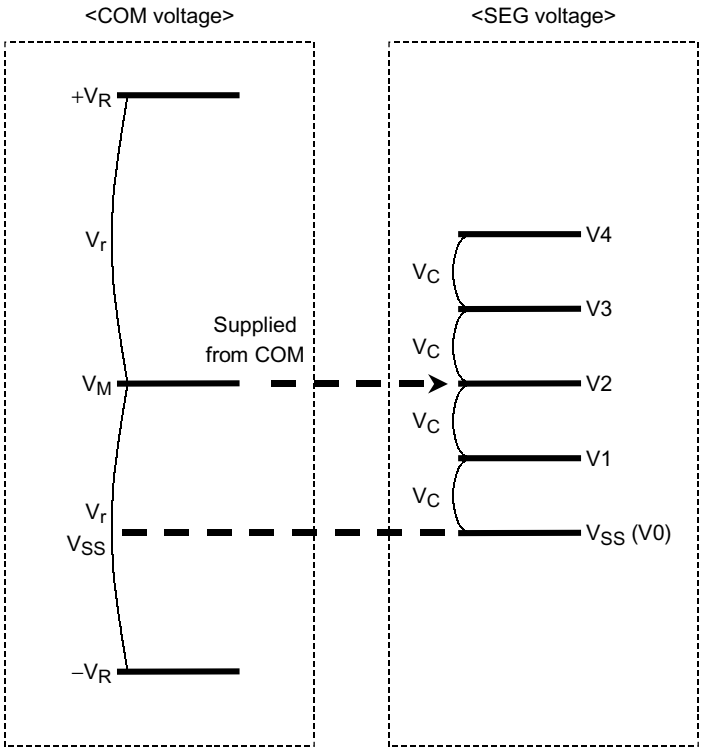
These display timing signals are shown below.



- CL : Shift clock. The common driver controls the COM output by responding to the falling edges of the CL signal.
- PM : First line marker signal
- RP1, 2 : Drive pattern signals for the common driver. Input at the rising edges of PM.
- FR : AC generation signal (which reverses the COM output polarity). Input at the rising edge of the CL signal.
- /DOFF : Display OFF signal. Input at the rising edges of the CL signal.

LCD Voltages

Relation between Display Voltages



<COM voltage>

- The COM voltage is varied ±V_R with respect to V_M.
- V_M is generated by COM and supplied to SEG.
- Contrast control is provided by changing voltage V_M.
- Voltage V_r is calculated as follows.

  $\underline{V_r = V_c \times n}$ *1/n Bias = 1/6, 1/8, 1/10

  $V_c = 1/2 \times V_M$

<SEG voltage>

- $V4 - V3 = V3 - V2 = V2 - V1 = V1 - V_{SS}$ (V0) = V_c
  (each voltage should always be V_c which is one-fourth V4)
- When the contrast is changed, the bias ratio is constant. Thus, the SEG voltage is varied with respect to V2, and its variations from the reference are equal.

Display Power Supply and Output Status for Each Mode

With T6K44, display power supply control (boost ON/OFF control) and display output ON/OFF control are provided by terminal inputs (/STB and /DOFF) from the SEG driver (S6B0023).

- Standby mode

/STB terminal input	L
/DOFF terminal input	L
PCK input	Stop
Boost (primary, secondary, and tertiary)	OFF
COM output	V_{SS}

Note 11: When this common driver operates in standby mode, V_M/+V_R/–V_R is in the following output status:
V_M: V_{SS} level
+V_R: V_{SS} level
–V_R: V_{SS} level

Note 12: When this common driver in standby mode uses the external power supply (EXP = H), the driver requires the following input voltages:

V2 input	V_{SS}
V_{CC} input	V_{SS}
V_{CC} input	V_{SS}
COM output	V_{SS} (V2)

- Display OFF

/STB terminal input	H
/DOFF terminal input	L
PCK input	Clock (5 to 7 kHz)
Boost (primary, secondary, and tertiary)	ON
COM output	V_M

- Display ON

/STB terminal input	H
/DOFF terminal input	H
PCK input	Clock (5 to 7 kHz)
Boost (primary, secondary, and tertiary)	ON
COM output	–V_R or V_M or +V_R

Note 13: After turning the power-on, be sure to initialize both the SE and COM drivers (with /RST = L), and then make necessary settings. If this initialization is not done, an abnormal display might appear after power-up.

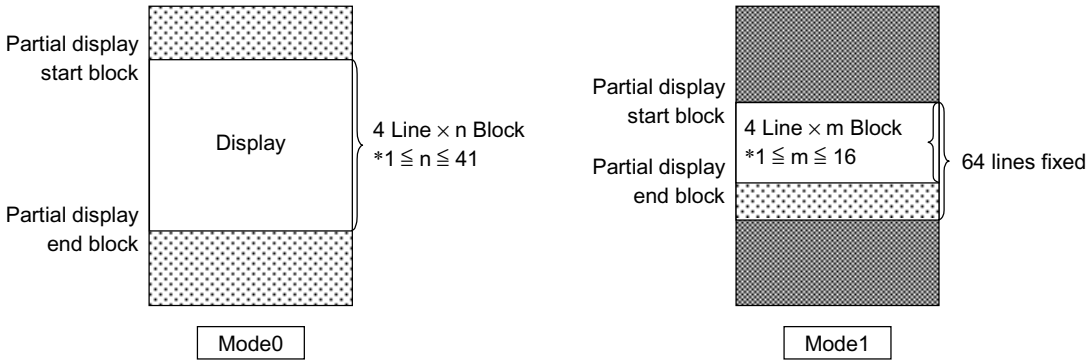
After the SEG driver (S6B0023) is initialized, it is in the following status (when the standby mode is ON):

/STB terminal input	L
/DOFF terminal input	L
PCK input	Stop
Boost (primary, secondary, and tertiary)	OFF
SEG output	V_{SS}

Note 14: Turning the power-off while a display is provided might cause the display to become abnormal. Thus, be sure to carry out a predetermined power-down procedure, and then turn the power-off.

Partial Display Mode

By using the /DOFF terminal, T6K44 can function with the SEG driver S6B0023 in partial display mode. The SEG driver has two partial display modes. T6K44 can suit either of the two modes.



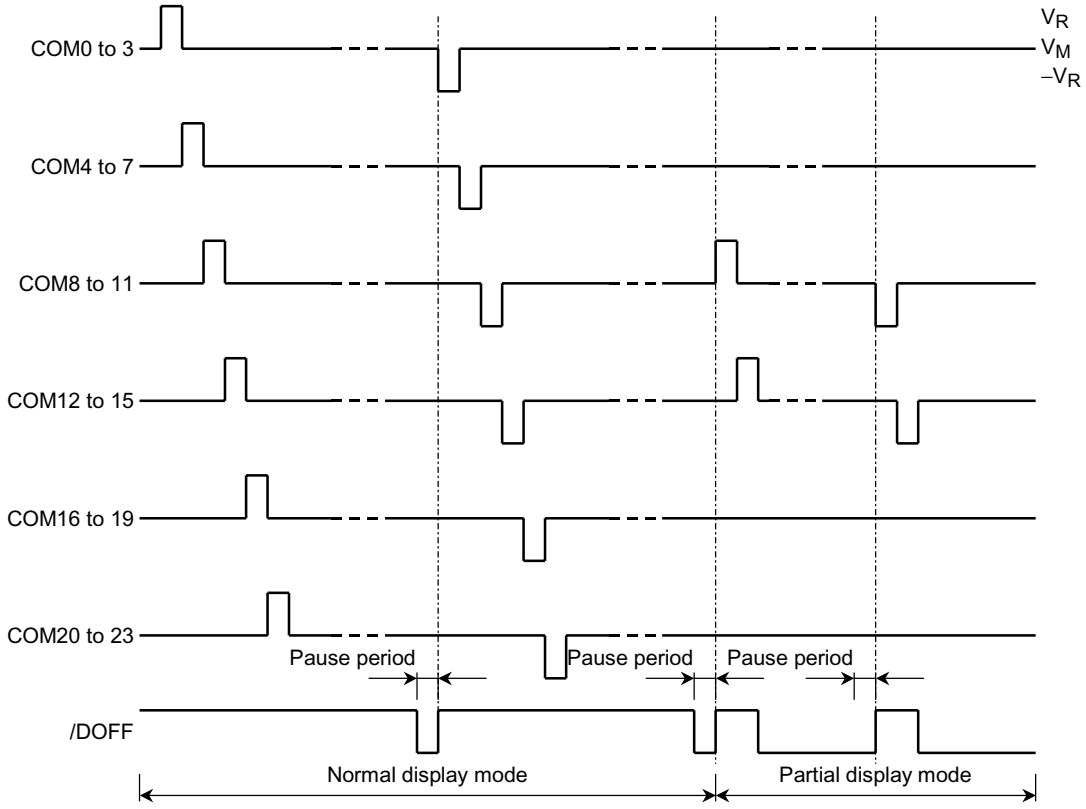
	Undisplayable area	: Not scanned by COM (COM = V2 fixed)
	Other than the partial display area	: Although COM timing is provided, display output = V2 fixed (/DOFF = L).
	Partial display area	: Portion which is actually displayed

- Partial display mode 0

  While the input at the /DOFF terminal is "L," the outputs at all the COM terminals can be set at the Vm level, and the outputs at all the SEG terminals at the V3 or V1 level. By using the outputs at these levels, only part of the screen is displayed. So, the display device can offer lower power requirements than it does in normal display mode.

  While the device draws less power, its display duty, contrast setting, and bias setting are the same as those for the normal display mode.

  Example: Partial Display for Block 1 (COM8 to COM15)



	Partial Display Area	Other than the Partial Display Area
Display duty	Same as the setting for normal mode	
Display bias	Same as that for normal mode (bias (1) setting)	
Contrast	Same as that for normal mode (contrast (1) setting)	
Oscillation circuit	Same as that for normal mode (between OSC1 and OSC2)	
SEG output level	Same as that for normal mode (V0, V1, V2, V3, V4)	V1 or V3
/DOFF terminal	H	L
COM output level	Same as that for normal mode ($+V_R$, V_M, $-V_R$)	V_M fixed

- Partial display mode 1

  Still lower power consumption is possible with partial display mode 1 which uses up to 64 lines. For this mode, a reduced number of lines are displayed by inputting /DOFF = L from the SEG driver in the same manner as that for mode 0.

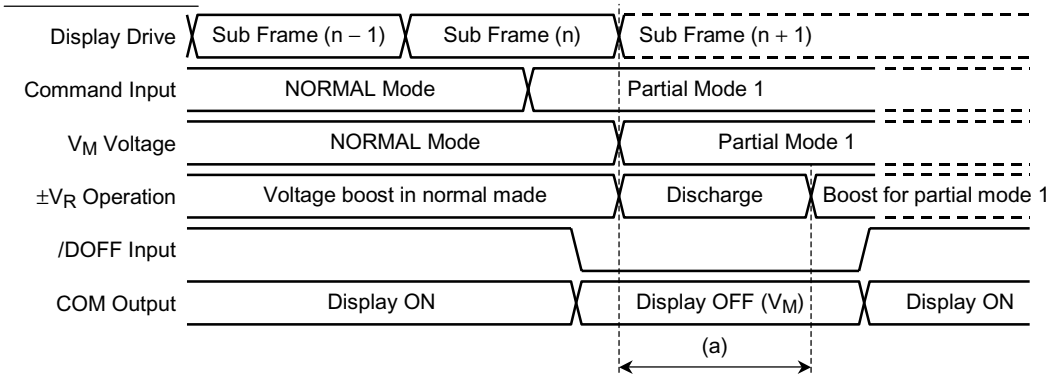
	Partial Display Area	Other than the Partial Display Area	Other than the Display Area
Display duty	1/64 duty (display area: 16 blocks) *		
Display bias	Bias (2) setting		
Contrast	Contrast (2) setting		
Oscillation circuit	Between OSC1 and OSC3		
SEG output level	Same as that for normal mode (V0, V1, V2, V3, V4)	V1 or V3	—
/DOFF terminal	H	L	—
COM output level	Same as that for normal mode ($+V_R$, V_M, $-V_R$)	V_M fixed	V_M fixed

- Discharge function for reducing the boost voltage for switching from the normal mode to partial mode 1

  To expedite the screen switching from the normal mode to partial mode 1, the boost voltage can be reduced at mode switching.

  The discharge function means that after the command for switching to partial mode 1 is issued, the $\pm V_R$ boost is forcibly reduced ($+V_R$: V45, $-V_R$: V_{SS}) during the period <a> from the start of the next subgroup. After the discharge, the reduced voltage increases to the level set for partial mode 1. The discharge period (a) is set at about 100 ms (at PCK = 5 kHz).

  To use this function, specify the display OFF period longer than the period (a) in the Display ON/OFF command.

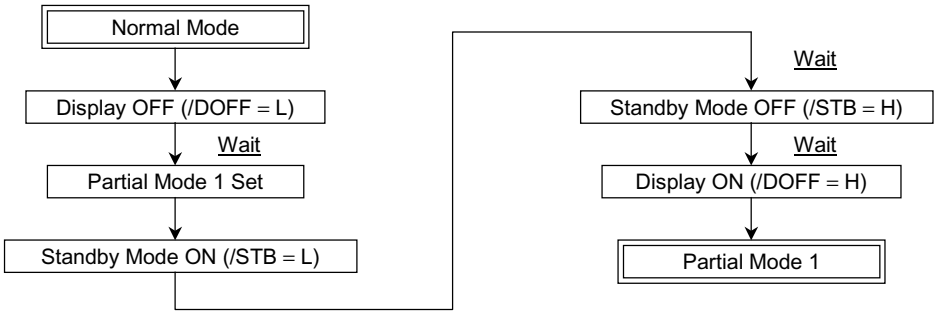


  This function can be set to ON/OFF by using the PSON terminal.

  PSON = H: Discharge function ON

  PSON = L: Discharge function OFF

  To use partial mode 1 with PSON = L, follow the command setting procedure shown below.

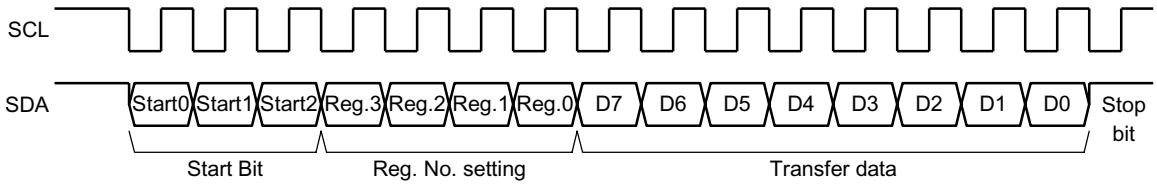


Note 15: Each period of wait time varies with the usage condition. Set these periods after thoroughly checking them.

Data Interface with the Segment Driver

To set data in the common driver (T6K44), the data is transferred from the segment driver to the common driver through serial interface (SCL and SDA) between them. T6K44 recognizes the serial data (SDA) by the rising edges of SCL.

<Specifications for Data Transfer from the SEG Driver (S6B0023)>



Start bits:

The COM driver receives data only when the three bits, start bits 0 through 2, are “L.”

Reg. Nos.:

The four bits, Reg.0, Reg.1, Reg.2, and Reg.3, specify the type of transfer command.

Reg.3	Reg.2	Reg.1	Reg.0	Transfer Data
0	0	0	0	(NOP)
0	0	0	1	Contrast set (1)
0	0	1	0	Contrast set (2)
0	0	1	1	Bias data
0	**1**	0	0	Partial mode
0	1	0	1	Partial area
0	1	1	0	Duty set
0	1	1	1	DC-DC select
1	x	x	x	TSB TEST mode

x: No problem

Transfer data:

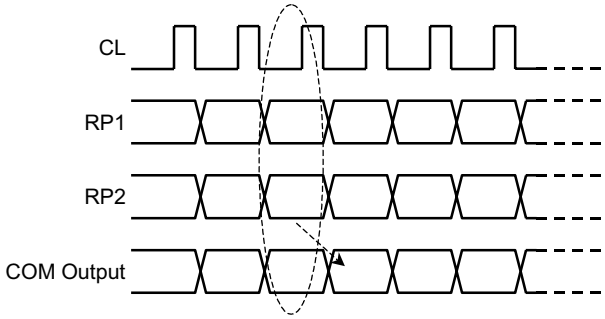
Parameter data (DB7-DB0) set in the SEG driver

Stop bit:

16 th clock signal (SDA = H) which stops data transfer

- Transfer of the row function

  T6K44 receives data from the SEG driver via the RP1 and RP2 terminals each time a rising edge of the CL signal occurs. Then, T6K44 produces display output with the specified row vector according to the following COM timing:



- Row function

RP2	RP1	Row Function
0	0	R1
0	1	R2
1	0	R3
1	1	R4

- For FR = L

	R1	R2	R3	R4
L1	0	1	1	1
L2	1	1	0	1
L3	1	0	1	1
L4	1	1	1	0

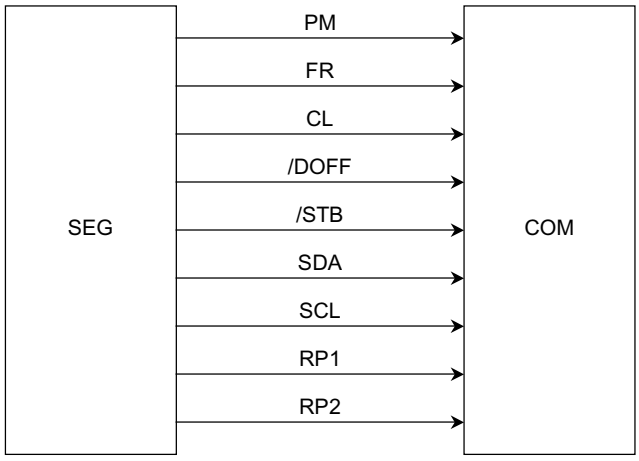
1: $+V_R$
0: $-V_R$

- For FR = H

	R1	R2	R3	R4
L1	1	0	0	0
L2	0	0	1	0
L3	0	1	0	0
L4	0	0	0	1

1: $+V_R$
0: $-V_R$

- Example connection (interface) between SEG and COM



Command Specifications

The following describes the specifications for the commands transferred from the SEG driver (S6B0023).

- Contrast control (1): (reg No.: 0001)

  This command specifies the contrast control value for normal/partial mode 0 which was set for the SEG driver (S6B0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Contrast Control (1) (00h to FFh)							

- Contrast control (2): (reg No.: 0010)

  This command specifies the contrast control value for normal/partial mode 1 (1/64 duty fixed) which was set for the SEG driver (S6B0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Contrast Control (2) (00h to FFh)							

- V_M for each contrast setting is shown below for reference.

Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)
0	00h	1.600	28	1Ch	1.820	56	38h	2.039	84	54h	2.259	112	70h	2.478
1	01h	1.608	29	1Dh	1.827	57	39h	2.047	85	55h	2.267	113	71h	2.486
2	02h	1.616	30	1Eh	1.835	58	3Ah	2.055	86	56h	2.275	114	72h	2.494
3	03h	1.624	31	1Fh	1.843	59	3Bh	2.063	87	57h	2.282	115	73h	2.502
4	04h	1.631	32	20h	1.851	60	3Ch	2.071	88	58h	2.290	116	74h	2.510
5	05h	1.639	33	21h	1.859	61	3Dh	2.078	89	59h	2.298	117	75h	2.518
6	06h	1.647	34	22h	1.867	62	3Eh	2.086	90	5Ah	2.306	118	76h	2.525
7	07h	1.655	35	23h	1.875	63	3Fh	2.094	91	5Bh	2.314	119	77h	2.533
8	08h	1.663	36	24h	1.882	64	40h	2.102	92	5Ch	2.322	120	78h	2.541
9	09h	1.671	37	25h	1.890	65	41h	2.110	93	5Dh	2.329	121	79h	2.549
10	0Ah	1.678	38	26h	1.898	66	42h	2.118	94	5Eh	2.337	122	7Ah	2.557
11	0Bh	1.686	39	27h	1.906	67	43h	2.125	95	5Fh	2.345	123	7Bh	2.565
12	0Ch	1.694	40	28h	1.914	68	44h	2.133	96	60h	2.353	124	7Ch	2.573
13	0Dh	1.702	41	29h	1.922	69	45h	2.141	97	61h	2.361	125	7Dh	2.580
14	0Eh	1.710	42	2Ah	1.929	70	46h	2.149	98	62h	2.369	126	7Eh	2.588
15	0Fh	1.718	43	2Bh	1.937	71	47h	2.157	99	63h	2.376	127	7Fh	2.596
16	10h	1.725	44	2Ch	1.945	72	48h	2.165	100	64h	2.384	128	80h	2.604
17	11h	1.733	45	2Dh	1.953	73	49h	2.173	101	65h	2.392	129	81h	2.612
18	12h	1.741	46	2Eh	1.961	74	4Ah	2.180	102	66h	2.400	130	82h	2.620
19	13h	1.749	47	2Fh	1.969	75	4Bh	2.188	103	67h	2.408	131	83h	2.627
20	14h	1.757	48	30h	1.976	76	4Ch	2.196	104	68h	2.416	132	84h	2.635
21	15h	1.765	49	31h	1.984	77	4Dh	2.204	105	69h	2.424	133	85h	2.643
22	16h	1.773	50	32h	1.992	78	4Eh	2.212	106	6Ah	2.431	134	86h	2.651
23	17h	1.780	51	33h	2.000	79	4Fh	2.220	107	6Bh	2.439	135	87h	2.659
24	18h	1.788	52	34h	2.008	80	50h	2.227	108	6Ch	2.447	136	88h	2.667
25	19h	1.796	53	35h	2.016	81	51h	2.235	109	6Dh	2.455	137	89h	2.675
26	1Ah	1.804	54	36h	2.024	82	52h	2.243	110	6Eh	2.463	138	8Ah	2.682
27	1Bh	1.812	55	37h	2.031	83	53h	2.251	111	6Fh	2.471	139	8Bh	2.690

Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)	Contrast (hex)		V_M (V)
140	8Ch	2.698	164	A4h	2.886	188	BCh	3.075	212	D4h	3.263	236	ECh	3.451
141	8Dh	2.706	165	A5h	2.894	189	BDh	3.082	213	D5h	3.271	237	EDh	3.459
142	8Eh	2.714	166	A6h	2.902	190	BEh	3.090	214	D6h	3.278	238	EEh	3.467
143	8Fh	2.722	167	A7h	2.910	191	BFh	3.098	215	D7h	3.286	239	EFh	3.475
144	90h	2.729	168	A8h	2.918	192	C0h	3.106	216	D8h	3.294	240	F0h	3.482
145	91h	2.737	169	A9h	2.925	193	C1h	3.114	217	D9h	3.302	241	F1h	3.490
146	92h	2.745	170	AAh	2.933	194	C2h	3.122	218	DAh	3.310	242	F2h	3.498
147	93h	2.753	171	ABh	2.941	195	C3h	3.129	219	DBh	3.318	243	F3h	3.506
148	94h	2.761	172	ACh	2.949	196	C4h	3.137	220	DCh	3.325	244	F4h	3.514
149	95h	2.769	173	ADh	2.957	197	C5h	3.145	221	DDh	3.333	245	F5h	3.522
150	96h	2.776	174	AEh	2.965	198	C6h	3.153	222	DEh	3.341	246	F6h	3.529
151	97h	2.784	175	AFh	2.973	199	C7h	3.161	223	DFh	3.349	247	F7h	3.537
152	98h	2.792	176	B0h	2.980	200	C8h	3.169	224	E0h	3.357	248	F8h	3.545
153	99h	2.800	177	B1h	2.988	201	C9h	3.176	225	E1h	3.365	249	F9h	3.553
154	9Ah	2.808	178	B2h	2.996	202	CAh	3.184	226	E2h	3.373	250	FAh	3.561
155	9Bh	2.816	179	B3h	3.004	203	CBh	3.192	227	E3h	3.380	251	FBh	3.569
156	9Ch	2.824	180	B4h	3.012	204	CCh	3.200	228	E4h	3.388	252	FCh	3.576
157	9Dh	2.831	181	B5h	3.020	205	CDh	3.208	229	E5h	3.396	253	FDh	3.584
158	9Eh	2.839	182	B6h	3.027	206	CEh	3.216	230	E6h	3.404	254	FEh	3.592
159	9Fh	2.847	183	B7h	3.035	207	CFh	3.224	231	E7h	3.412	255	FFh	3.600
160	A0h	2.855	184	B8h	3.043	208	D0h	3.231	232	E8h	3.420			
161	A1h	2.863	185	B9h	3.051	209	D1h	3.239	233	E9h	3.427			
162	A2h	2.871	186	BAh	3.059	210	D2h	3.247	234	EAh	3.435			
163	A3h	2.878	187	BBh	3.067	211	D3h	3.255	235	EBh	3.443			

Note 16: Contrast and V_M values in the blank field must not be set for 1/10 bias.

- Bias set: (reg No.: 0011)

  This command specifies the bias ratio for normal/partial mode 0 or partial mode 1 which was set for the SEG driver (S6B0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
*	*	Bias (2)		0	0	Bias (1)	

<bias (2)>
: For partial mode 1

DB5	DB4	Bias
0	0	1/6
0	1	1/8
1	0	1/10
1	1	—

Note 17: Initial setting: 1/6 bias

<bias (1)>
: For normal/partial mode 0

DB1	DB0	Bias
0	0	1/6
0	1	1/8
1	0	1/10
1	1	—

Note 17: Initial setting: 1/6 bias

- Bias (1)

  Bias settings for normal mode/partial display mode 0.
  The settings are changed automatically when normal mode/partial display mode 0 is set. (initial setting)

- Bias (2)

  Bias settings for partial display mode 1 (1/64 duty fixed).
  The settings are changed automatically when partial display mode 1 is set.

- Bias definition

  $\underline{\text{Bias ratio} = V_c/V_r}$ (*$V2 = V_M$)
  V_c: V4 – V3 = V3 – V2 = V2 – V1 = V1 – V0 (V_{SS}) ..... SEG voltage
  V_r: $|+V_R|-V_M = |-V_R|+V_M$..... COM voltage

*Display voltages (typ.) for each bias setting

Contrast		1/6 Bias		1/8 Bias		1/10 Bias	
V_M		$+V_R$	$-V_R$	$+V_R$	$-V_R$	$+V_R$	$-V_R$
min	1.6	6.4	–3.2	8.0	–4.8	9.6	–6.4
typ.	2.6	10.4	–5.2	13.0	–7.8	15.6	–10.4
max	3.6	14.4	–7.2	18.0	–10.8	—	—

Note 18: The voltage range might be unusable depending on the V_{IN} voltage and boost multiplier settings.

Note 19: V_M = 2.88 V or more (contrast setting: A4h to FFh) must not be set for 1/10 bias.

- Partial mode set: (reg No.: 0100)

  This command specifies the partial display mode which was set for the SEG driver (S6B0023) by MPU.
  When this command is executed, the contrast setting, bias setting, and DC-DC Select are changed automatically according to the mode selected (normal/partial mode 0/partial mode 1).

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
*	*	0	0	0	0	Mode	PT

PT: Partial Display ON/OFF
PT = 0・・・Partial Display OFF = Normal Mode (initial setting)
PT = 1・・・Partial Display ON

Mode: Partial Mode Set
Mode = 0・・・Partial Mode 0: Duty fixed
Mode = 1・・・Partial Mode 1: Duty changed (64 lines fixed) <low power consumption mode>

Mode	PT	Display Mode
0	0	Normal mode
0	1	Partial mode 0
1	0	Setting prohibited
1	1	Partial mode 1

- Partial area set: (reg No.: 0101)

  This command specifies the partial display start block parameter for the partial display IN command which was set for the SEG driver (SB0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
*	*	Partial display start block					

- Duty set: (reg No.: 0110)

  This command specifies the duty set which was set for the SEG driver (SB0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
*	*	0	0	0	0	Display duty	

DB1	DB0	Display Duty
0	0	1/128
0	1	1/144
1	0	1/160
1	1	1/168

(initial setting: 1/128 duty)

- DC-DC select: (reg No.: 0111)

  This command specifies the boost multiplier for normal/partial display mode 0 or partial mode 1 which was set for the SEG driver (S6B0023) by MPU.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
*	*	DC-DC (2)		0	0	DC-DC (1)	

<DC-DC (2)>
: For partial mode 1

DB5	DB4	DC-DC (2)
0	0	×4
0	1	×5
1	0	×6
1	1	Prohibited

Note 20: Initial setting: 4×

<DC-DC (1)>
: For normal/partial mode 0

DB1	DB0	DC-DC (1)
0	0	×4
0	1	×5
1	0	×6
1	1	Prohibited

Note 20: Initial setting: 4×

  - DC-DC (1)

    Multiplier settings for normal mode/partial display mode 0.
    The settings are changed automatically when normal mode/partial display mode 0 is set.

  - DC-DC (2)

    Multiplier settings for partial display mode 1 (1/64 duty fixed).
    The settings are changed automatically when partial display mode 1 is set.

- NOP: (reg No.: 0000)

  When receiving this command from the SEG driver, T6K44 performs no operation (i.e., it continues to be in the current state).

- TSB TEST mode: (reg No.: 1xxxx)

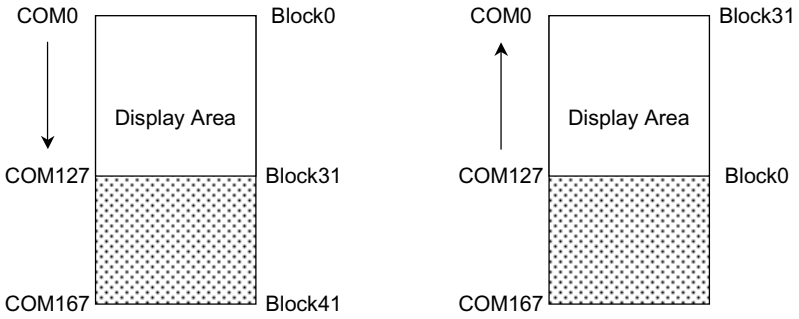
  The commands with Reg. 0 = 1 are used for testing by Toshiba.
  These commands must not be accessed from the SEG driver (S6B0023).

COM Direction

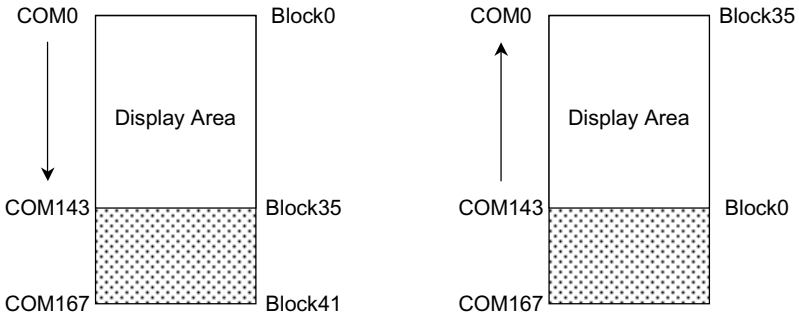
T6K44 can change the direction by using the DIR terminal.
The following shows the COM scan directions (up/down) and display duty block numbers.

<DIR = L> <DIR = H>

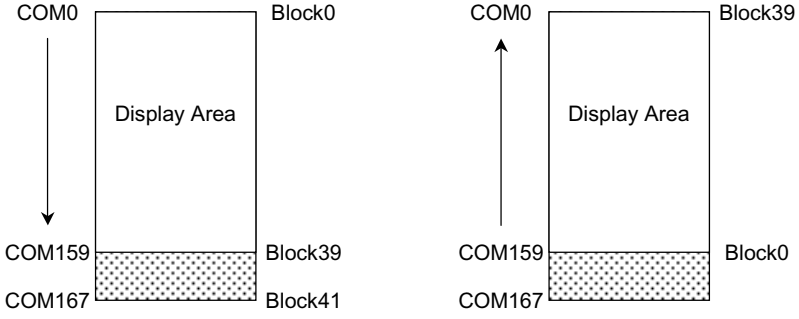
- For 1/128 duty



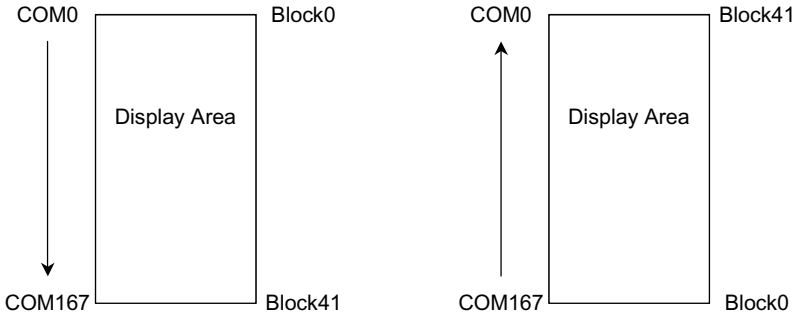
- For 1/144 duty



- For 1/160 duty



- For 1/168 duty



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage (1)	V_{DD} (Note 21)	−0.3 to 6.0	V
Power supply voltage (2)	ΔV_R (Note 22)	40.0 max	V
Input voltage	V_{in}	−0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 125	°C

Note 21: Value referenced from V_{SS} = 0 V

Note 22: $\Delta V_R = |+V_R| + |-V_R|$

Electrical Characteristics of T6K44

DC Characteristics (1):

(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = −20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
Operating voltage (1)	V_{DD}	—	—	1.8	3.0	3.3	V	V_{DD}
Operating voltage (2)	V_{IN}	—	—	2.7	3.0	3.6	V	V_{IN}
Input voltage (1) for display	V_M	—	(Note 23)	1.6	—	3.6	V	V2
Input voltage (2) for display	V_{CC}	—	(Note 23)	4.8	—	18.0	V	V_{CC}
Input voltage (3) for display	V_{EE}	—	(Note 23)	−12.0	—	−3.2	V	V_{EE}
High-level input voltage	V_{IH}	—	—	V_{DD} × 0.8	—	V_{DD}	V	(Note 24)
Low-level input voltage	V_{IL}	—	—	V_{SS}	—	V_{DD} × 0.2	V	(Note 24)
Input leakage	I_{IL}	—	(Note 25)	−1	—	1	μA	(Note 24)
Common output resistance	R_{on}	—	(Note 26)	—	1.3	2.0	kΩ	COM0-167
Consumed current (1)	I_{ss1}	—	(Note 27)	—	TBD	TBD	μA	V_{SS}
Consumed current (2)	I_{ss2}	—	(Note 28)	—	TBD	TBD	μA	V_{SS}
Consumed current (3)	I_{ssstb}	—	(Note 29)	−1	—	1	μA	V_{SS}

Note 23: External power supply mode (EXP = H)

Note 24: /RST, /STB, /DOFF, CL, PM, FR, SDA, SCK, RP1, RP2, PCK, DIR, EXP, PSON

Note 25: Vinput = V_{SS} to V_{DD}

Note 26: 1/8 bias, V_{CC} = 14.0 V, V_{EE} = −8.4 V, V2 = 2.8 V, external power supply (EXP = H), I_{Load} = 100 μA

Note 27: V_{DD} = 3.0 V, V_{IN} = 3.0 V, contrast = 99h (V_M = 2.8 V), normal mode, 1/168 duty, 1/8 bias, 6× boost, f_{FR} = 70 Hz, no data access (SDA, SCK = H), internal power supply mode (EXP = L), primary DC-DC converter OFF (V_{IN} = V45), display ON (/DOFF = H), dummy subgroup = +1, PCK = 5 kHz, C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, $\pm V_R$ hold C = 1.0 μF, no load on display

Note 28: V_{DD} = 3.0 V, V_{IN} = 3.0 V, contrast = 33h (V_M = 2.0 V), partial mode 1, 1/64 duty, 1/10 bias, 5× boost, f_{FR} = 70 Hz, no data access (SDA, SCK = H), internal power supply mode (EXP = L), primary DC-DC converter OFF (V_{IN} = V45), display ON (/DOFF = H), dummy subgroup = +1, PCK = 5 kHz, C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, $\pm V_R$ hold C = 1.0 μF, no load on display

Note 29: V_{DD} = 3.0 V, V_{IN} = 3.0 V, standby mode (/STB = L), PCK = OFF, CL/PM/FR = OFF, RP1/RP2 = OFF, no load on display

DC Characteristics (2): Power Supply Circuit

(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
–Boost output voltage level	NVRLO	—	(Note 30)	–5.6	—	–5.5	V	$-V_R$
+Boost output voltage level	PVRLO	—	(Note 30)	11.1	—	11.2	V	$+V_R$
–Boost offset	ΔNVRLO	—	(Note 31)	—	—	100	mV	$-V_R$
+Boost offset	ΔPVRLO	—	(Note 32)	–100	—	—	mV	$+V_R$
Boost output voltage level balance	ΔV_R	—	(Note 33)	—	—	100	mV	$-V_R$, $+V_R$
AMP output voltage level	V_{MO}	—	(Note 34)	2.75	2.8	2.85	V	V_M
AMP offset	ΔV_M	—	(Note 35)	–50	—	50	mV	V_M
AMP output temperature inclination	VMT	—	(Note 36)	–0.04	0.00	0.04	%/°C	V_M

Note 30: V_{DD} = 3.0 V, V_{IN} = 3.0 V, DC - DC = × 5, 1/6 bias, normal mode, V_M = 2.8 V, I_{Load} = 0.0 μA, Ta = 25°C
C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, ±V_R hold C = 1.0 μF

Note 31: V_{DD} = 3.0 V, V_{IN} = 3.0 V, DC - DC = × 5, 1/6 bias, normal mode, V_M = 2.8 V, I_{Load} = 60.0 μA, Ta = 25°C
C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, ±V_R hold C = 1.0 μF, PCK = 5 kHz
ΔNVRLO = |NVRLO| – |NVRLO'| *NVRLO': NVRLO for the system under load (I_{load} = 60 μA)

Note 32: V_{DD} = 3.0 V, V_{IN} = 3.0 V, DC - DC = × 5, 1/6 bias, normal mode, V_M = 2.8 V, I_{Load} = –60.0 μA, Ta = 25°C
C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, ±V_R hold C = 1.0 μF, PCK = 5 kHz
ΔPVRLO = |PVRLO| – |PVRLO'| *PVRLO': PVRLO for the system under load (I_{load} = –60 μA)

Note 33: V_{DD} = 3.0 V, V_{IN} = 3.0 V, DC - DC = × 5, 1/8 bias, normal mode, V_M = 2.8 V,
I_{Load} (+V_R) = –60.0 μA, I_{load} (–V_R) = 60 μA, Ta = 25°C
C11 - C15 = 0.1 μF, C31 = 0.47 μF, V_M hold C = 2.2 μF, ±V_R hold C = 1.0 μF, PCK = 5 kHz
ΔV_R = | (+V_R –V_M) – |–V_R –V_M| |

Note 34: V_{DD} = 3.0 V, V_{IN} = 3.0 V, V45 = V_{IN} (3.0 V), contrast = 99h, normal mode, V_M hold C = 2.2 μF,
I_{Load} = 0.0 μA, Ta = 25°C

Note 35: V_{DD} = 3.0 V, V_{IN} = 3.0 V, V45 = V_{IN} (3.0 V), contrast = 99h, normal mode, V_M hold C = 2.2 μF,
I_{Load} = ±330 μA. , Ta = 25°C
$\Delta V_M = V_{MO} - V_{MO}'$ *V_{MO}': V_{MO} for the system under load (I_{load} = ±330 μA)

Note 36: V_{DD} = 3.0 V, V_{IN} = 3.0 V, V_{ref} hold C = 0.1 μF, I_{Load} = 0.0 μA ,Ta = –20 to 60°C

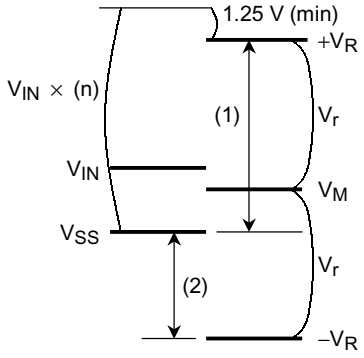
Recommended Operating Conditions:

(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
+Boost voltage (4×)	PVR4	—	4× boost (Note 37)	—	—	$V_{IN} \times 4$ –1.25	V	$+V_R$
+Boost voltage (5×)	PVR5	—	5× boost (Note 37)	—	—	$V_{IN} \times 5$ –1.25	V	$+V_R$
+Boost voltage (6×)	PVR6	—	6× boost (Note 37)	—	—	$V_{IN} \times 6$ –1.25	V	$+V_R$
–Boost voltage (4×)	NVR4	—	4× boost (Note 37)	$2 \times V_M$ – PVR4	—	—	V	$-V_R$
–Boost voltage (5×)	NVR5	—	5× boost (Note 37)	$2 \times V_M$ – PVR5	—	—	V	$-V_R$
–Boost voltage (6×)	NVR6	—	6× boost (Note 37)	$2 \times V_M$ – PVR6	—	—	V	$-V_R$
V_M set voltage (1)	V_{M1}	—	(Note 38)	—	—	V_{IN} – 0.2	V	V_M
V_M set voltage (2)	V_{M2}	—	(Note 39)	—	—	V_{IN} – 0.25 V	V	VM

Note 37: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = 25°C, I_{Load} = 0.0 μA,

*: When this common driver runs from its internal power supply, the bias and contrast for $V_R = V_{IN} \times$ (boost multiplier) – 1.25 [V] can be used. If the bias and contrast for $+V_R$ exceeding the limit are used, the driver operation is unpredictable.



(1): PVRn = $V_{IN} \times n$ – 1.25 (V) * n = Boost multiplier

(2): NVRn = $V_M - V_r = 2 \times V_M$ – PVRn (V)

- Acceptable $+V_R$ (typ.) by V_{IN} /boost multiplier

V_{IN}	×4 Boost	×5 Boost	×6 Boost
2.70 V	9.55 V	12.25 V	14.95 V
2.80 V	9.95 V	12.75 V	15.55 V
2.90 V	10.35 V	13.25 V	16.15 V
3.00 V	10.75 V	13.75 V	16.75 V
3.10 V	11.15 V	14.25 V	17.35 V
3.20 V	11.55 V	14.75 V	17.95 V
3.30 V	11.95 V	15.25 V	18.55 V
3.40 V	12.35 V	15.75 V	19.15 V
3.50 V	12.75 V	16.25 V	19.75 V
3.60 V	13.15 V	16.75 V	20.35 V

Note 38: For more information, see the table of V_{IN}s vs. maximum contrast settings (reference values) for each boost multiplier.

Note 39: V_{DD} = 1.8 to 3.0 V, V_{IN} = 3.0 V, $V_{DD} \leqq V_{IN}$, primary boost OFF (V_{IN} = V45), Ta = 25°C, I_{Load} = ±330 μA,
*These conditions should be verified for detailed assessment of the characteristics.

Note 40: V_{DD} = 1.8 to 2.7 V, V_{IN} = 2.7 V, $V_{DD} \leqq V_{IN}$, primary boost OFF (V_{IN} = V45), Ta = 25°C, I_{Load} = ±330 μA,
*These conditions should be verified for detailed assessment of the characteristics.

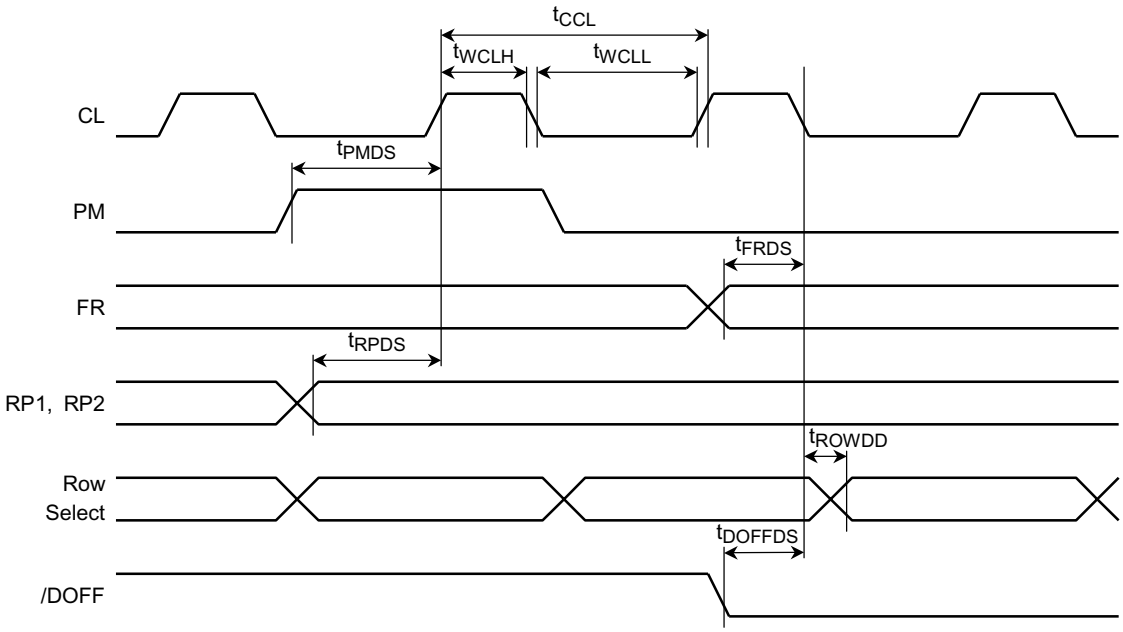
- Table of V_{IN}s vs. Maximum Contrast Settings (reference values) for Each Boost Multiplier (Note 41) DC-DC converter used: Primary (1.5×)

Boost Setting	V_{IN} Voltage (V)	Maximum Contrast Setting		
		1/6 Bias	1/8 Bias	1/10 Bias
×4 boost	2.7	64h	27h	Unusable
	2.8	71h	31h	07h
	2.9	7Dh	3Bh	0Fh
	3.0	8Ah	46h	18h
	3.1	97h	50h	20h
	3.2	A4h	5Ah	29h
	3.3	B0h	64h	31h
	3.4	BDh	6Eh	3Ah
	3.5	CBh	79h	42h
	3.6	D7h	83h	4Bh
×5 boost	2.7	BAh	6Ch	38h
	2.8	CAh	79h	42h
	2.9	DAh	85h	4Dh
	3.0	EAh	92h	57h
	3.1	FAh	9Fh	62h
	3.2	FFh	ACh	6Dh
	3.3	FFh	B8h	78h
	3.4	FFh	C5h	82h
	3.5	FFh	D2h	8Dh
	3.6	FFh	DFh	97h
×6 boost	2.7	FFh	B1h	71h
	2.8	FFh	C0h	7Eh
	2.9	FFh	CFh	8Ah
	3.0	FFh	DFh	97h
	3.1	FFh	EEh	A3h
	3.2	FFh	FDh	A3h
	3.3	FFh	FFh	A3h
	3.4	FFh	FFh	A3h
	3.5	FFh	FFh	A3h
	3.6	FFh	FFh	A3h

Note 41: The range of contrast settings when the primary DC-DC converter is OFF (V_{IN} = V45). is restricted by the V_{IN} voltage used.

AC Characteristics:

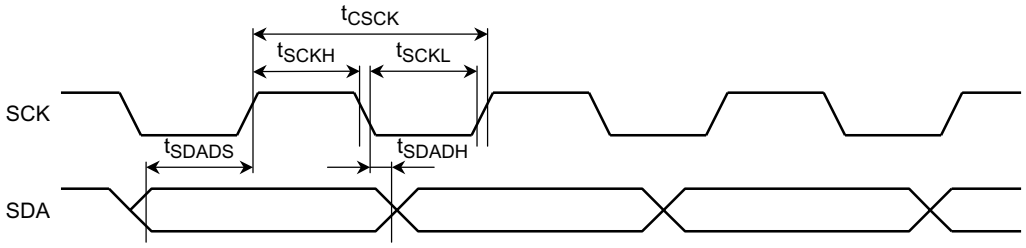
- Driver timing



(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
CL cycle time	t_{CCL}	—	—	25	—	—	µs	CL
CL high pulse width	t_{WCLH}	—	—	3	—	—	µs	CL
CL low pulse width	t_{WCLL}	—	—	18	—	—	µs	CL
PM setup time	t_{PMDS}	—	—	1	—	—	µs	PM
FR setup time	f_{FRDS}	—	—	1	—	—	µs	FR
Row parameter set up time	t_{RPDS}	—	—	1	—	—	µs	RP1 RP2
Row select delay time	t_{ROWDD}	—	—	—	—	0.5	µs	COM0 to COM167
/DOFF setup time	t_{DOFFDS}	—	—	1	—	—	µs	/DOFF

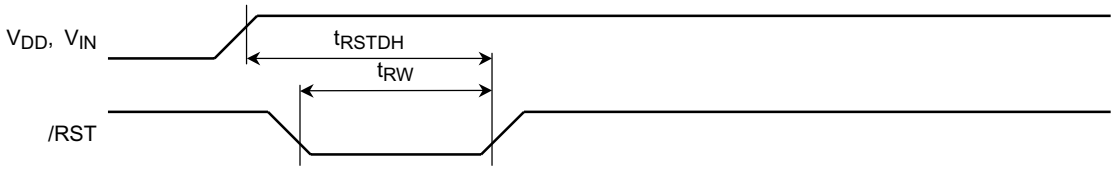
- Serial data interface



(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
SCK cycle time	t_{CSCK}	—	—	2000	—	—	ns	SCK
SCK high pulse width	t_{WSCKH}	—	—	800	—	—	ns	SCK
SCK low pulse width	t_{WSCKL}	—	—	800	—	—	ns	SCK
SDA setup time	t_{SDADS}	—	—	500	—	—	ns	SDA
SDA hold time	t_{SDADH}	—	—	0	—	—	ns	SDA

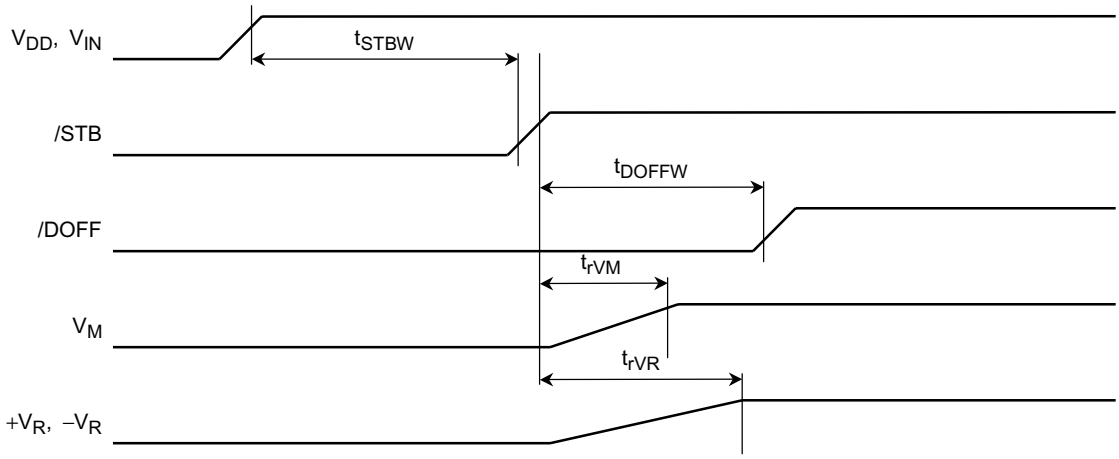
- Reset Function



(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
/RST pulse width	t_{RW}	—	—	1	—	—	μs	/RST
/RST hold time	t_{RSTDH}	—	—	1	—	—	μs	/RST

- /STB, /DOFF

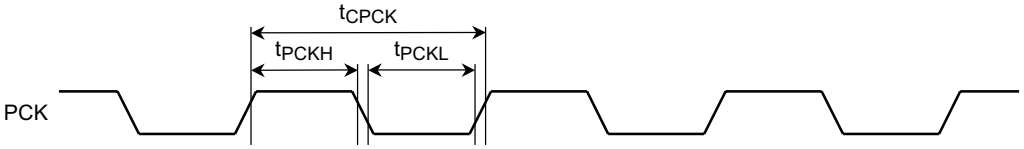


(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
/STB L → H wait time	t_{STBW}	—	—	10	—	—	ms	/STB
/DOFF = L → H wait time	t_{DOFFW}	—	—	200	—	—	ms	/DOFF
V_M rise time	t_{rVM}	—	V_{IN} = 3.0 V Contrast = 99h	—	—	200	ms	V_M
$+V_R$/$-V_R$ rise time	t_{rVR}	—	V_{IN} = 3.0 V 6× boost	—	—	200	ms	$+V_R$ $-V_R$

Note 42: C11 - C15 = 0.1 μF, $+V_R$ hold C = 1.0 μF, C31 = 0.47 μF, $-V_R$ hold C = 1.0 μF, V_M hold C = 2.2 μF, PCK = 5 kHz

- PCK



(test circuit: V_{DD} = 1.8 to 3.3 V, V_{IN} = 2.7 to 3.6 V, $V_{DD} \leqq V_{IN}$, Ta = –20 to 60°C unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Terminal
PCK cycle time	t_{CPCK}	—	—	67	—	200	μs	PCK
PCK high pulse width	t_{PCKH}	—	—	30	—	—	μs	PCK
PCK low pulse width	t_{PCKL}	—	—	30	—	—	μs	PCK

- Precautions in design and usage

  The following shows the usage precautions. They should be considered in the system design stage.

  (1) This product is guaranteed to normally operate at V_{DD} within a predetermined range of power supply voltages.
  If V_{DD} falls out of the range or it is open, the proper operation is not ensured.

  (2) To turn the power-off (i.e., set V_{DD} equal to 0 V or open), follow these steps:
  (a) Place an "L" input at the /DOFF terminal. (display OFF mode)
  (b) Place an "L" input at the /STB terminal. (standby mode)
  (c) Wait long enough for discharge to be completed.
  (the discharge time should be checked in an actual machine.)
  (d) Turn the power-off.
  Even if you turn the power-off as describe above, abnormal display might appear. Therefore, the system should be carefully configured and assessed.

  (3) Be sure to set V_{DD} equal to or less than V_{IN}.

  (4) If light is shone on the semiconductor chip, a photoelectric effect occurs, generating a voltage which might cause its malfunction. If the front, back, and side of the semiconductor chip in a device are visible from outside the device, this chip is highly susceptible to a photoelectric effect. Therefore, the device should have a design which prevents diffused light from entering it. The evil photoelectric effect describe above should be considered not only when the chip is put into practical use but also when it undergoes the inspection procedures.

RESTRICTIONS ON PRODUCT USE

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- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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