Am6112

Microprocessor Compatible 12-Bit A/D Converter

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

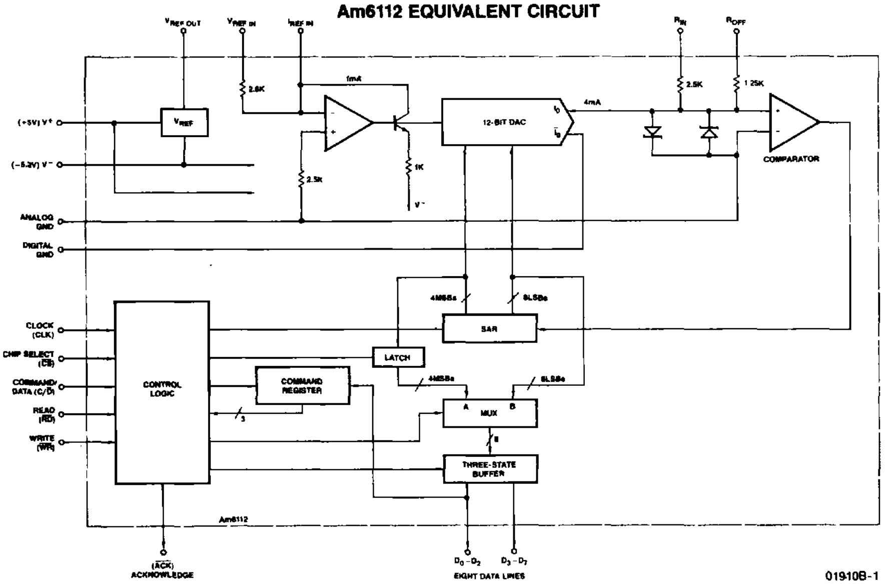
- First totally monolithic, high-speed 12-bit ADC
- 3μs typical conversion time
- Internal precision voltage reference
- No missing codes
- Easy interfacing with 8- and 16-bit microprocessors
- Internal command register for programmable modes of operation
- Offset binary or two's complement output code
- 0 to 10V, or ± 5V input range
- 24-pin package

FUNCTIONAL DESCRIPTION

The Am6112 is the first fully monolithic microprocessor compatible 12-bit high-speed analog-to-digital converter. The Am6112 high-speed A/D contains a precision reference, DAC, comparator, SAR, scale resistors, output three-state buffers and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The Am6112 is capable of completing a 12-bit conversion in typically three microseconds and can handle input voltage ranges of 0 to 10V, and ±5V without external components.

The Am6112 has four modes of microprocessor operation, and a stand-alone mode. These modes are software programmable, except for the stand-alone mode which is pin selectable. Applications include analog I/O subsystems, servo-control and high-speed digital signal processing of analog events.

Am6112 EQUIVALENT CIRCUIT



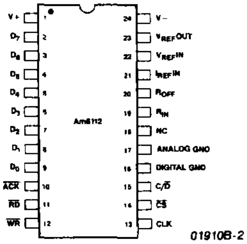
01910B-1

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type	Temperature Range
AM6112DC	Hermetic DIP	0 to +70°C
AM6112XC	Dice	0 to +70°C
AM6112DM	Hermetic DIP	–55 to +125°C

CONNECTION DIAGRAM – Top View
D-24-1



01910B-2

Note: Pin 1 is marked for orientation.

01910B-ANA

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at R_{IN}, R_{OFF}	±12V
V− to D GND	+0.3 to −7.0V	Open Collector Current	20mA
Max Differential V+ to V−	±12V	Operating Temperature	0 to +70°C
Digital Inputs to D GND	−0.5 to +6.0V	Storage Temperature	−65 to +150°C
A GND to D GND	±1V	Lead Temperature (Soldering 60 sec)	300°C
V_{REF} Max Output Current	15mA	Minimum Operating Voltage	9.7V
Max Input Current at REF_{IN}	2mA	Max Package Dissipation	1W
Voltage at GAIN R, REF_{IN}	V− to V+		

2

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected per connection diagram, T_A = 25°C, F_{Clock} = 150kHz, 0 to +10V input range, R_{OFF} open, stand-alone mode, unless otherwise stated)

PRELIMINARY

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		12	12		Bits
	Monotonicity				12	Bits
	Differential Nonlinearity				±1	LSB
	Linearity			±1		LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error			±2		LSB
	Unipolar Offset Error			±1/2		LSB
	Bipolar Gain Error	V_{IN} = −5V to +5V		±4		LSB
	Bipolar Offset Error			±2		LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.005		%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.005		%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1mA	2.490	2.5	2.510	Volts
V_{REF}/T_A	Reference Voltage Tempco			8		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.005		$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	$V^+ = +5V \pm 5\%$, $-5.2 \pm 5\%$		0.005		$\%V_{REF}$
	Noise, N = 10kHz to 1MHz					μV_{RMS}
Analog Inputs						
R_{IN}	**Input Resistance**					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
C_{IN}	**Input Capacitance**					
	R_{IN}, R_{OFF}, REF_{IN}, GAIN R			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7V			40	μA
I_{IL}	Logic 0	V_{IN} = 0.4V			10	μA

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	Off-State Output Current					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			40	80	mA
$I-$	Negative Supply Current			−60	−80	mA
	Power Dissipation			500	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time R_{OFF} connected to A_{GND} or $V_{REF\ OUT}$ (Bipolar)		[illegible]		μs
	R_{OFF} Open (Unipolar)		10		μs
t_{CL}	CLK Low		125		ns
t_{CH}	CLK High		125		ns

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as either the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): *Monotonicity is a property of* the DAC within a successive approximation ADC. Each increment in the digital code to the DAC is accompanied by an analog *output that is greater than or equal to that of the proceeding code.* Monotonicity of the DAC is a necessary requirement for a successive approximation ADC to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input which produces a given digital output code. An ideal value of a code width is equivalent to $FSR/2^n$, where in is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages *within a given range are represented by a single digital output* code. There is, therefore, an *inherent* ±1/2 LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2 LSB.

Unipolar Offset Error: Difference between the ideal (+1/2 LSB) and the actual analog input level required to produce the *first digital code transition (00 .... 00 to 00 .... 01) over the* complete temperature range.

Bipolar Offset Error: Difference between the ideal (1/2 FSR − 1/2 LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 .... 11 to 10 .... 00).

Power Supply Sensitivity: A measure of the change in gain and offset of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: *The measure of how long it takes for the A/D* to arrive at the correct digital output code. It is the time between the clock edge that starts a conversion after receiving a start *command and the edge of the status line ($\overline{CC}$) which signifies that* the conversion is completed.

THEORY OF OPERATION

The Am6112 is a fully μP-compatible programmable 12-bit A/D converter. The device is initialized by writing a 3-bit word into the internal command register via the bidirectional data pins $D_0 - D_2$; in this operation, bits D_1 and D_2 configure the converter into one of four modes, while D_0 provides the choice of either offset-binary or two's complement output code. A fifth mode is pin selectable and is a unique stand-alone mode in which the internal command register is programmed whenever the control inputs READ ($\overline{RD}$) and WRITE ($\overline{WR}$) are LOW together.

The Am6112 has the standard μP peripheral control lines, CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), READ ($\overline{RD}$), plus one non-standard line, COMMAND/DATA ($C/\overline{D}$). The $C/\overline{D}$ control qualifies both the read and write operations. It defines a write operation as either an initialization or an external start conversion command, and during read cycles it steers either the upper or lower data byte to the data outputs.

The Am6112 requires an external clock (CLK) to control the conversion speed. The status output acknowledge ($\overline{ACK}$) is derived from the internal Conversion Complete ($\overline{CC}$) line, which indicates whether a conversion is in progress or completed.

The Successive Approximation Register performs the analog-to-digital conversion by sequentially testing the effect of removing the bit currents (B_{11} to B_0) of the D/A converter, which are all steered to the A/D summing node. The bit currents are binarily scaled versions of the reference current flowing into the D/A converter reference amplifier, and the voltage comparator decides whether the bit currents should be removed or retained. The reference current is obtained from the internal reference voltage source using the scale resistor connected to V_{REF}OUT. The Am6112 contains the necessary gain and range selection resistors enabling bipolar signals between −5V and +5V, and unipolar signals from 0 to +10V to be digitized. The device operates from +5 and −5.2V supplies.

Am6112 FUNCTIONAL PIN DESCRIPTION

V_{REF}OUT 2.5V internal voltage reference output.

V_{REF}IN Connected to an external voltage reference (V_{REF}OUT) to establish a reference current for the DAC bit currents.

I_{REF}IN External reference current input for ratiometric operation.

R_{IN} Analog voltage input.

R_{OFF} When connected to V_{REF}OUT, 1/2 scale offset is generated to accomodate bipolar analog input signals.

$D_0 - D_7$ Three-state data lines. $D_0 - D_2$ are bidirectional data lines, while $D_3 - D_7$ are strictly output data lines. Data is loaded into the internal COMMAND register via $D_0 - D_2$ to select one of four modes of operation. $D_0 - D_7$ are used to output the 8 LSBs ($B_0 - B_7$). $D_0 - D_3$ are used to output the 4 MSBs ($B_8 - B_{11}$) of the 12-bit data, while $D_4 - D_7$ output the sign bit (B_{11}).

$\overline{WR}$ Active low input used to reset the SAR and start a conversion cycle (Modes 0 and 3). This input line is also used to load data into the command register along with $C/\overline{D}$ line held high.

$\overline{RD}$ Active low input used to read the SAR data. SAR data is read in two bytes. The reading of the high byte ($B_8 - B_{11}$) or low byte is user selectable except during Mode 2 via the $C/\overline{D}$ line (see Status Truth Table).

$C/\overline{D}$ Used in loading the COMMAND register with an active $\overline{WR}$ or outputting the HIGH and LOW data bytes with an active $\overline{RD}$ (see Status Truth Table).

$\overline{CS}$ Active low input allows the Am6112 to be involved in I/O operations (see Status Truth Table).

$\overline{ACK}$ Open collector, active low output indicating the status of the Am6112.

CLK Clock input synchronizing and controlling the operation of the Am6112.

V+ +5V power supply input.

V− −5.2 power supply input.

AGND Analog ground.

DGND Digital ground.

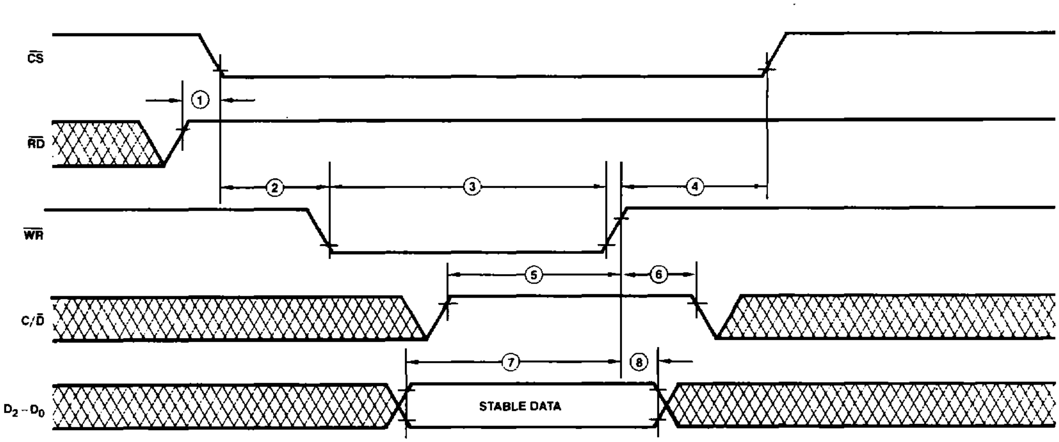
Am6112 Control Signal Decoding

STATUS TRUTH TABLE				
Control Logic Inputs				Am6112 Status
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	$C/\overline{D}$	
1	X	X	X	Output Data Lines ($D_7 - D_0$) in High Impedance State
0	0	0	X	Forced to STAND-ALONE MODE Operation
0	1	0	1	Write into Command Register to Select Mode of Operation
0	0	1	0	Read 8 LSBs (Low Byte), Except in MODE 2
0	0	1	1	Read 4 MSBs (High Byte), Except in MODE 2
0	1	0	0	Start Conversion (MODES 0, 3 and Stand-Alone)
0	0	1	0	Start Conversion, MODE 1

Am6112
INITIALIZATION TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{RD}-\overline{CS}}$	$\overline{RD}$ HIGH to $\overline{CS}$ LOW ($\overline{RD}$ Setup)	10			ns
2	$t_{\overline{SCS}-\overline{WR}}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW ($\overline{CS}$ Setup)	10			ns
3	$t_{\overline{WR}}$	$\overline{WR}$ Pulse Width	100			ns
4	$t_{\overline{WR}-\overline{CS}}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW ($\overline{WR}$ Hold)	10			ns
5	$t_{SC/\overline{D}-\overline{WR}}$	C/$\overline{D}$ HIGH to $\overline{WR}$ HIGH (C/$\overline{D}$ Setup)	100	30		ns
6	$t_{HC/\overline{D}-\overline{WR}}$	$\overline{WR}$ HIGH to C/$\overline{D}$ HIGH (C/$\overline{D}$ Hold)	10			ns
7	$t_{SD-\overline{WR}}$	Data Setup Time	100			ns
8	$t_{HD-\overline{WR}}$	Data Hold Time	20			ns

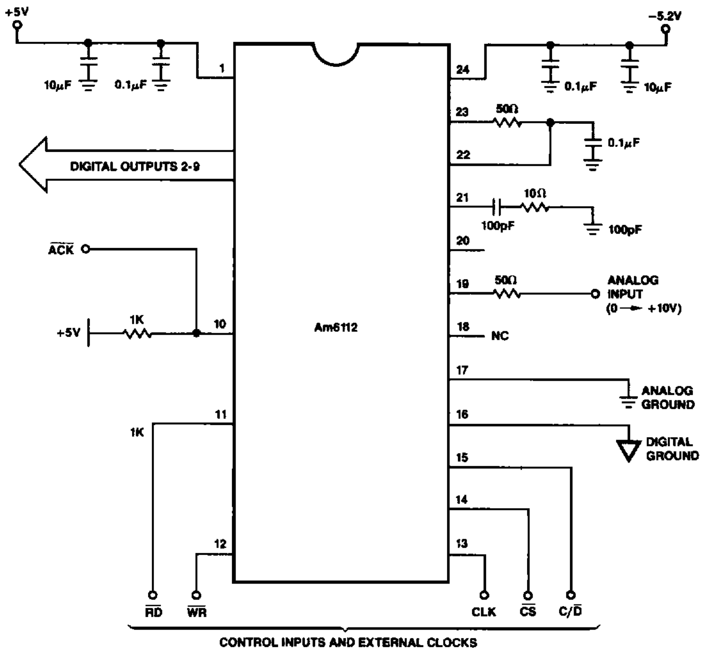
INITIALIZATION TIMING DIAGRAM



Am6112 COMMAND REGISTER DECODING

Mode/Coding Format Truth Tables			
Command Register Bits			
D_2	D_1	D_0	Mode Description
X	X	0	Offset binary output
X	X	1	Two's complement output code (except stand-alone mode).
0	0	X	MODE 0 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{WR}$. Internal status ($\overline{CC}$) gated with $\overline{RD}$ and $\overline{CS}$.
0	1	X	MODE 1 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{RD}$. Internal status ($\overline{CC}$) gated with $\overline{RD}$ and $\overline{CS}$.
1	0	X	MODE 2 – Am6112 under DMA control (such as the Am9517A). Conversion cycles started by active $\overline{RD}$. Data outputted as 8 LSBs first and then the 4 MSBs. Output data control is done internally and not accessible by the user.
1	1	X	MODE 3 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{WR}$. Internal status ($\overline{CC}$) gated with $\overline{CS}$ only.

TEST CIRCUIT – Top View



01910B-3

CALIBRATION TEXT

Unipolar Configuration (Figure 1)

The Am6112 contains all the active components required to perform a complete 12-bit A/D conversion. All that is necessary, in most situations, is the connection of the power supplies (+5V and −5.2V), analog input, and conversion initiation command, discussed later. The Am6112 has a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of the code. If no trims are used, the Am6112 has a typical zero offset error of ±1/2 LSB, and gain error of ±2 LSB. When no trims are required R_{OFF} should be left open for the best DNL specification (refer to accuracy versus DNL curve). If the gain error (full-scale) trim is not required, potentiometer R_4 should be replaced with 50Ω precision resistor matched to R_5.

Unipolar Calibration

Connecting R_{OFF} to R_1 and R_2, the initial offset error can be trimmed by R_3. The first A/D transition (0000 0000 0000 to 0000 0000 0001) should occur for an input level of +1/2 LSB (1.22mV).

The gain error (full-scale) trim is done by applying a signal 1/2 LSB's below the nominal full-scale (9.9964V). R_4 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

Bipolar Configuration (Figure 2)

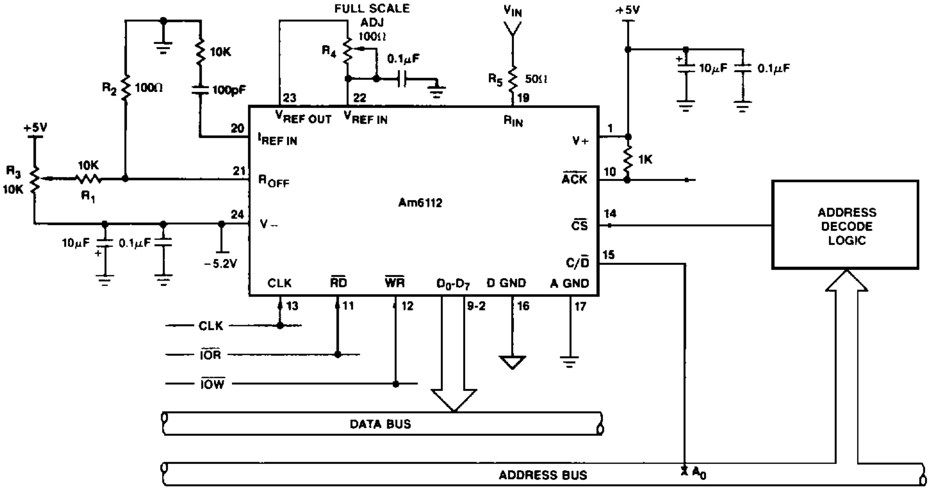
If the offset and gain errors are acceptable, potentiometers R_1 and R_2 should be replaced by precision 25 and 50Ω resistors respectively.

Bipolar Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2 LSB above negative full scale (−4.9988V for the ±5V input range) is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full-scale (4.9963V) is applied and potentiometer R_2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

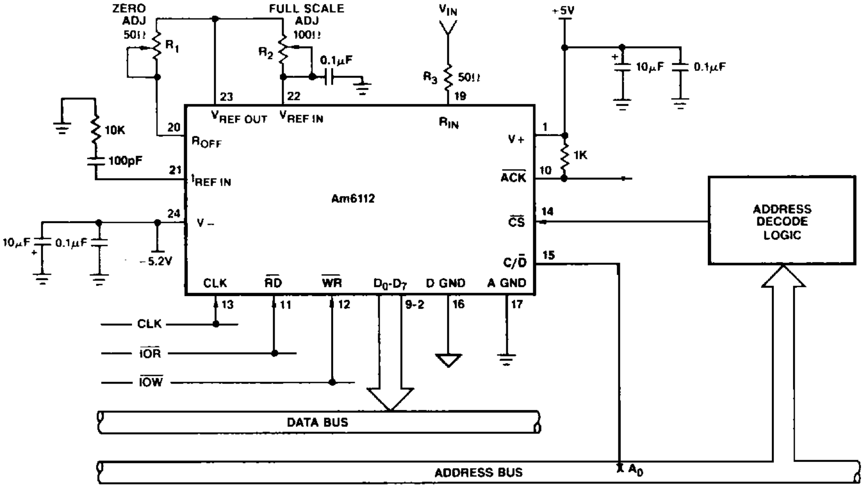
Offset and gain calibration can be more accurately trimmed by summing a small triangular wave voltage to the analog input signal, and the digital outputs monitored to determine the center point of the code transition.

Figure 1. Am6112 Unipolar Configuration



01910B-4

Figure 2. Am6112 Bipolar Configuration



01910B-5

APPLICATIONS INFORMATION

Depending on the processor used and throughput rate required, the user can select up to five operating modes.

In MODE 0, the conversion cycle is started by an active write ($\overline{WR}$) and the next two read ($\overline{RD}$) commands send the data out. The status of the command/data (C/$\overline{D}$) line determines whether the output data consists of the eight LSBs or four MSBs. In this mode, as well as Modes 1 and 2, the $\overline{ACK}$ line reflects the ADC's status during an active read period. For example, if conversion complete ($\overline{CC}$) is high during the entire read period, $\overline{ACK}$ is also high. $\overline{ACK}$ can then be used to extend the I/O read cycle if desired.

In MODE 1, a conversion cycle is started by an active read. Reading of the 12-bit data and the action of the $\overline{ACK}$ output is similiar to Mode 0. This mode is well suited to microprocessors such as the Z80 and Z8000 which have data-block transfer as part of their repertoire. The first 12-bit data output is invalid in this mode because the conversion cycle does not start until the positive transition of the second read pulse.

MODE 2 puts the A/D converter under control of a DMA controller such as the Am9517A. During DMA transfer, the microprocessor is disabled, and the Am9517A provides all the signals to control the conversion process. In Mode 2, the A/D converter internally controls the output of the data bytes. The first read signal sends out the 8 LSBs and simultaneously saves the four MSBs into an internal latch.

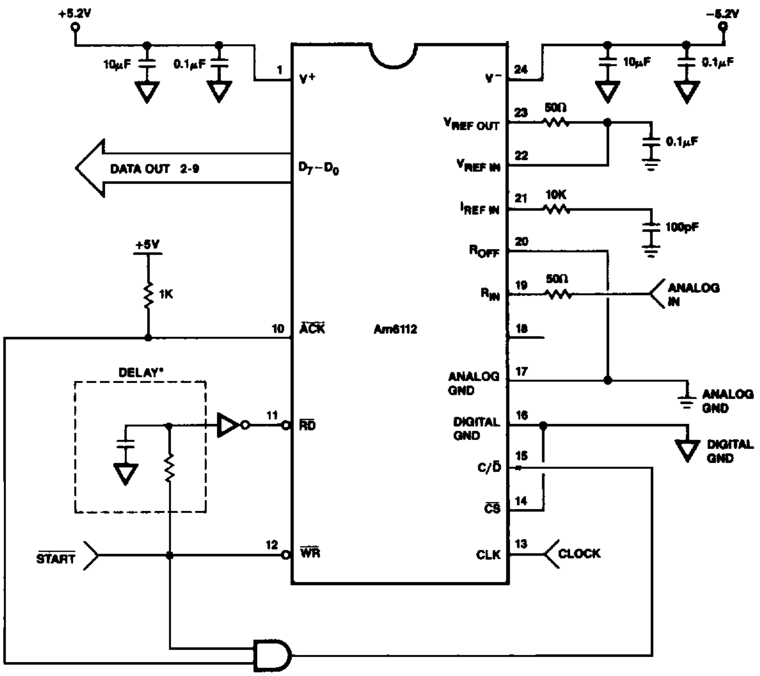
The LOW-to-HIGH transition of the first read initiates another conversion cycle. A second read cycle sends out the latched MSBs at the same time the A/D converter is performing the next conversion. The $\overline{ACK}$ output is internally masked so that the conversion complete ($\overline{CC}$) does not extend the second read cycle.

MODE 3 is similar to Mode 0 except that the $\overline{ACK}$ line reflects the A/D converter's true status. This difference in the decoding of the $\overline{ACK}$ line provides flexibility in the microprocessor handshaking. Although tying the $\overline{ACK}$ line to the microprocessor's Wait input pin might reduce throughput, by adding additional Wait states, it does guarantee full 12-bit conversion cycles.

MODE 4 is a unique stand-alone mode, in which the internal command register is preprogrammed to operate with offset binary data output format. Mode 4 is programmed whenever RD and $\overline{WR}$ are low together. This situation is an illegal state with any microprocessor-based system.

In Figure 3, CS can be grounded at all times. Applying a start pulse to the $\overline{WR}$ pin initiates two events. First, because the pulse at $\overline{RD}$ is actually a delayed write signal, sometime after the start signal is applied, both $\overline{RD}$ and $\overline{WR}$ are low at the same time, and the Am6112 is forced to Mode 4 operation. Secondly, $\overline{WR}$ going high after this delay starts the A/D conversion cycle, as long as C/$\overline{D}$ is LOW. The data can be read as soon as $\overline{RD}$ returns low. The $\overline{ACK}$ line acts as a conversion complete signal which provides a simple means of steering the data bytes to the data outputs. $\overline{ACK}$ is gated with $\overline{WR}$ so that C/$\overline{D}$ will always be low whenever a conversion cycle is required.

Figure 3. Stand-Alone Mode



01910B-11

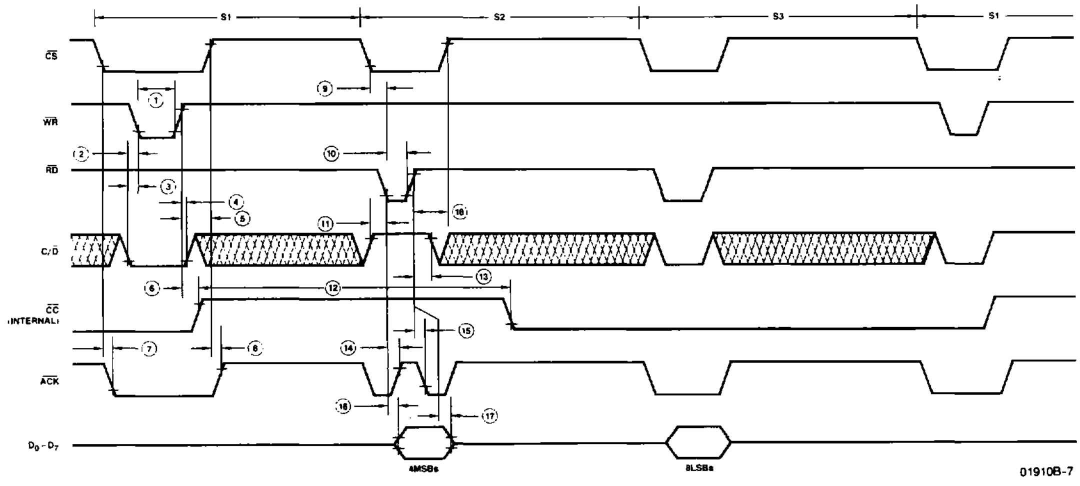
*Delay can be implemented with logic gates.

Am6112
MODE 0 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{WR}L}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}L-WL}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-WL}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold	20			
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
8	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay	20	50	100	ns
9	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW	20			ns
10	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
11	$t_{C/\overline{D}-RL}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	20			ns
12	t_{CONV}	Conversion Time	14 CLK			
13	$t_{RH-C/D}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
14	$t_{RL-\overline{ACK}H}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		50	100	ns
15	$t_{RH-\overline{ACK}L}$	$\overline{RD}$ HIGH to $\overline{ACK}$ LOW Delay		50	100	ns
16	$t_{RL-DTVLD}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
17	$t_{\overline{CS}H-DTVLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns
18	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to CS HIGH	20			

*Note: t_{CLK} = 1 Clock Period.

MODE 0 TIMING DIAGRAM



S_1 – Start a conversion cycle with an active WR.

S_2 – Read first data byte. The 4 MSBs become valid 6 clock periods after $\overline{CC}$ goes high. Therefore, the 4 MSBs may be read during S_2 while the conversion cycle is in progress. If conversion is done ($\overline{CC}$ going low) prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 and S_3 is the same as during S_1. If the conversion time is longer than S_1 + S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2.

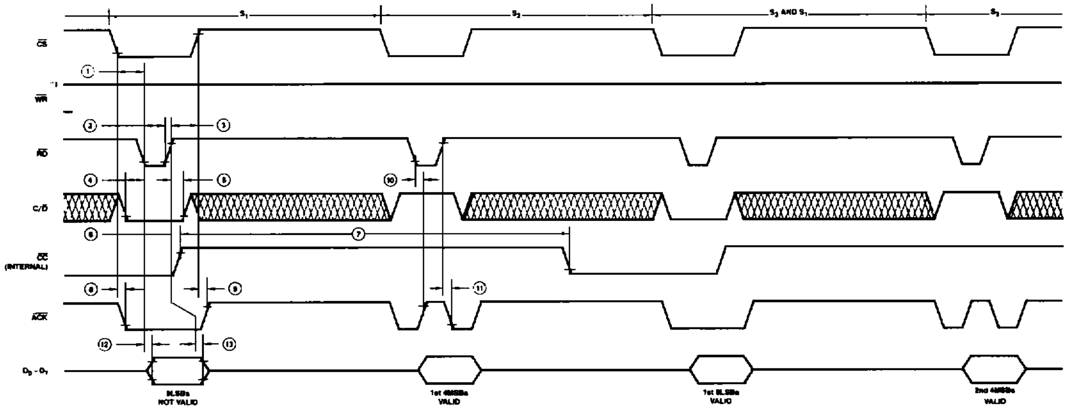
S_3 – Read second data byte.

MODE 1 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	20			ns
2	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
3	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	20			ns
4	$t_{C/\overline{D}-\overline{CS}L}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	10			ns
5	$t_{RH-C/\overline{D}}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
6	$t_{RH-\overline{CC}H}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time	14 CLK			
8	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
10	$t_{RL-\overline{ACK}H}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		50	100	ns
11	$t_{RH-\overline{ACK}L}$	$\overline{RD}$ HIGH to $\overline{ACK}$ LOW Delay		50	100	ns
12	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
13	$t_{RH-DTHLD}$	RD HIGH to Data Hold	20			ns

*Note: t_{CLK} = 1 Clock Period.

MODE 1 TIMING DIAGRAM



01910B-8

S_1 – Start the first conversion cycle with an active RD. The 8 LSBs read are not valid.

S_2 – Read the first valid 4 MSBs. The 4 MSBs become valid 6 clock periods after CC goes high. Therefore, the 4 MSBs may be read during S_2 while the conversion cycle is in progress. If conversion ends prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 is the same as during S_1. If the converison time is longer than S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2.

S_3 and S_1 – Read the first valid 8 LSBs and start the next conversion cycle.

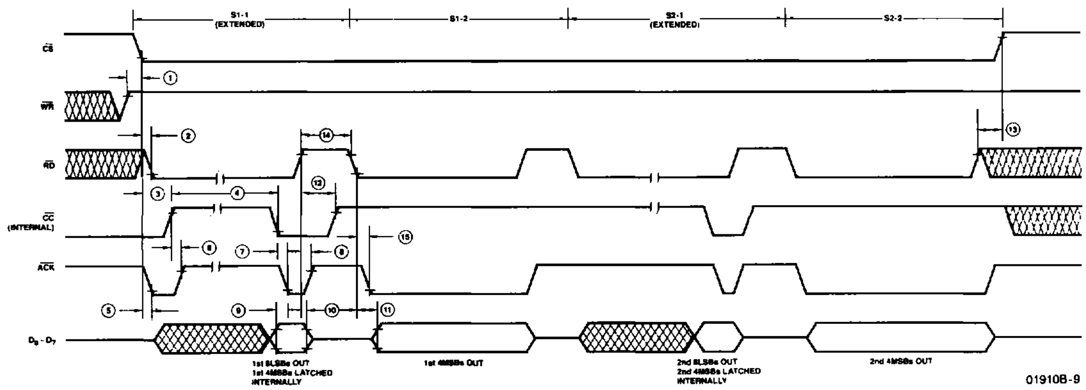
Am6112

MODE 2 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{WH-\overline{CS}L}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW Setup	10			ns
2	$t_{\overline{CS}L-\overline{RD}L}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-\overline{CC}H}$	$\overline{CS}$ LOW to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
4	t_{CONV}	Conversion Time	14 CLK			
5	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
6	$t_{\overline{CC}H-\overline{ACK}H}$	$\overline{CC}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
7	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
8	$t_{RH-\overline{ACK}H}$	$\overline{RD}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
9	$t_{LB-\overline{ACK}L}$	Data to $\overline{ACK}$ LOW	20	50		ns
10	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20	35		ns
11	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
12	$t_{RH-\overline{CC}H}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
13	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	10			ns
14	t_{RH}	$\overline{RD}$ HIGH	50			ns
15	$t_{RL-\overline{ACK}L}$	$\overline{RD}$ LOW to $\overline{ACK}$ LOW		50	100	ns

*Note: t_{CLK} = 1 Clock Period.

MODE 2 TIMING DIAGRAM



01910B-9

S_{1-1} – Start first conversion with $\overline{CS}$ going LOW. First 4 MSBs are latched internally. First 8 LSBs are valid when $\overline{CC}$ goes LOW. Note that S_{1-1} cycle is extended by the insertion of wait states using the $\overline{ACK}$ signal. Second conversion starts after $\overline{RD}$ goes HIGH.

S_{1-2} – Read first 4 MSBs. Note that this cycle is not extended.

S_{2-1} – This cycle is similar to the S_{1-1} cycle.

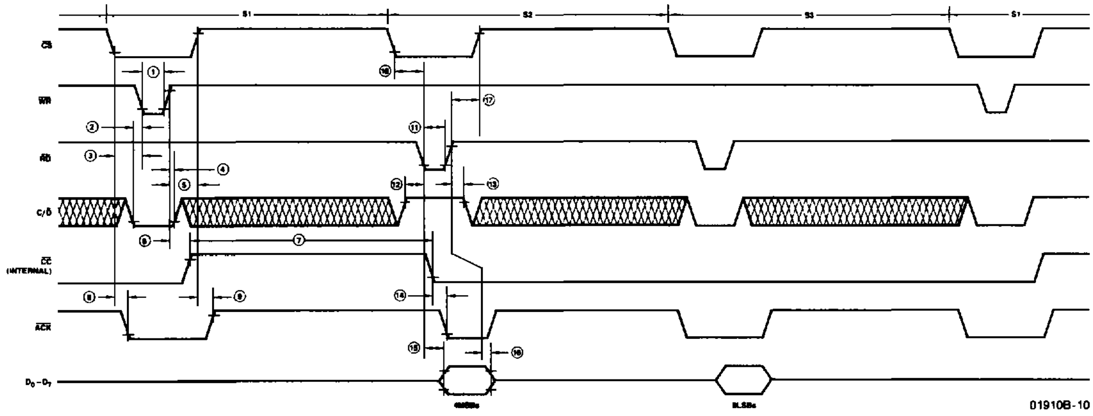
S_{2-2} – This cycle is similar to the S_{1-2} cycle except that conversion cycles are inhibited after $\overline{CS}$ goes HIGH.

MODE 3 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{WR}L}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}-WL}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-WL}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Setup	20			
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time	14 CLK			
8	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
10	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	10			ns
11	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
12	$t_{C/\overline{D}H-RL}$	C/$\overline{D}$ HIGH to $\overline{RD}$ LOW Setup	10			ns
13	$t_{RH-C/\overline{D}H}$	$\overline{RD}$ HIGH to C/$\overline{D}$ HIGH Hold	10			ns
14	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay				ns
15	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
16	$t_{\overline{CS}H-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns
17	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH				

*Note: t_{CLK} = 1 Clock Period.

MODE 3 TIMING DIAGRAM



S_1 – Start a conversion cycle with an active $\overline{WR}$.

S_2 – Read first data byte. The 4 MSBs become valid 6 clock periods after $\overline{CC}$ goes high. Therefore, the 4 MSBs may be read during S_2 while conversion cycle is in progress. If conversion is done ($\overline{CC}$ has gone low) prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 and S_3 is the same as during S_1. If conversion ends during active part of S_2 ($\overline{CS}$ low) $\overline{ACK}$ output is as shown above. If the conversion time is longer than S_1 + S_2, then the ACK output can be used to extend the active part of S_2.

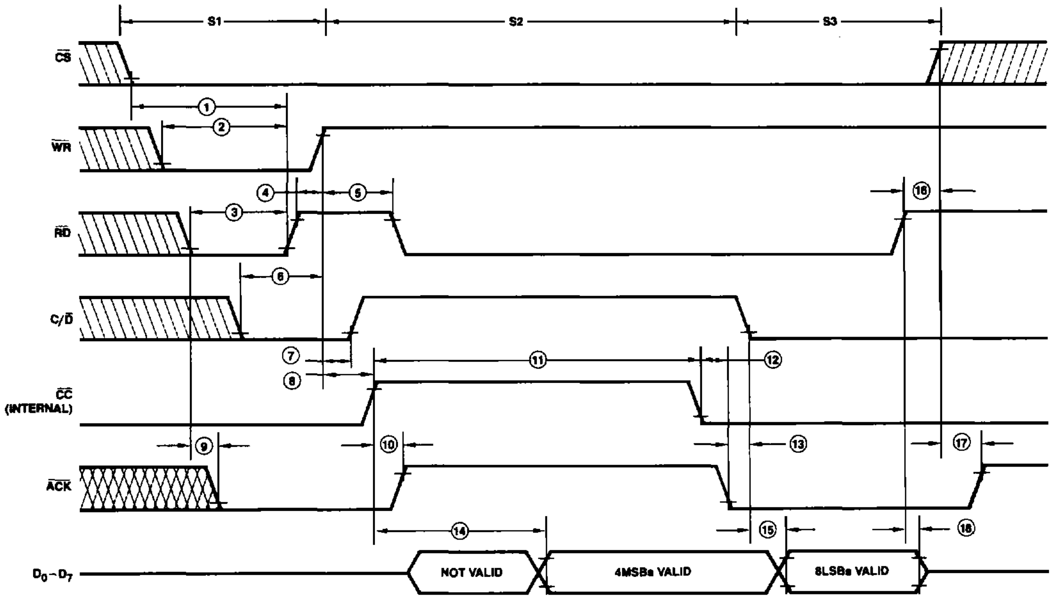
S_3 – Read second data byte.

Am6112
STAND-ALONE MODE TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	100			ns
2	t_{WL-RL}	$\overline{WR}$ LOW to $\overline{RD}$ LOW Setup	100			ns
3	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
4	t_{RH-WH}	$\overline{RD}$ HIGH to $\overline{WR}$ HIGH Setup	10			ns
5	t_{WH-RH}	$\overline{WR}$ HIGH to $\overline{RD}$ HIGH Hold	20			ns
6	$t_{C/\overline{D}L-WH}$	C/$\overline{D}$ LOW to $\overline{WR}$ HIGH Setup	110			ns
7	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
8	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
9	$t_{RL-\overline{ACK}L}$	$\overline{RD}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
10	$t_{\overline{CC}H-\overline{ACK}H}$	$\overline{CC}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
11	t_{CONV}	Conversion Time	14 CLK			
12	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW		50	100	ns
13	$t_{\overline{ACK}L-C/\overline{D}L}$	$\overline{ACK}$ LOW to C/$\overline{D}$ LOW	0			ns
14	$t_{\overline{CC}H-UBVLD}$	$\overline{CC}$ HIGH to Upper Byte Valid (Note 1)		4.5	t_{CLK} + 50*	ns
15	$t_{C/\overline{D}L-LBVLD}$	C/$\overline{D}$ LOW to Lower Byte Valid		50	100	ns
16	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH Setup	10			ns
17	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
18	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns

*Note: t_{CLK} = 1 Clock Period.

STAND-ALONE TIMING DIAGRAM



01910B-12

S_1 – Initialize Am6112 to stand-alone mode and start conversion cycle.

S_2 – Read valid 4 MSBs.

S_3 – Read valid 8 LSBs.

Microprocessor Interfacing

The Am6112 provides a variety of interfacing options. For example, Mode 0 is suitable for microprocessor-based systems with low throughput and the conversion process is directly under microprocessor control. This approach results in a minimum of hardware. In operation, the microprocessor initiates a conversion and is then forced into a Wait state which prevents the processor from performing other tasks until the conversion is complete and the A/D converter's data can be read.

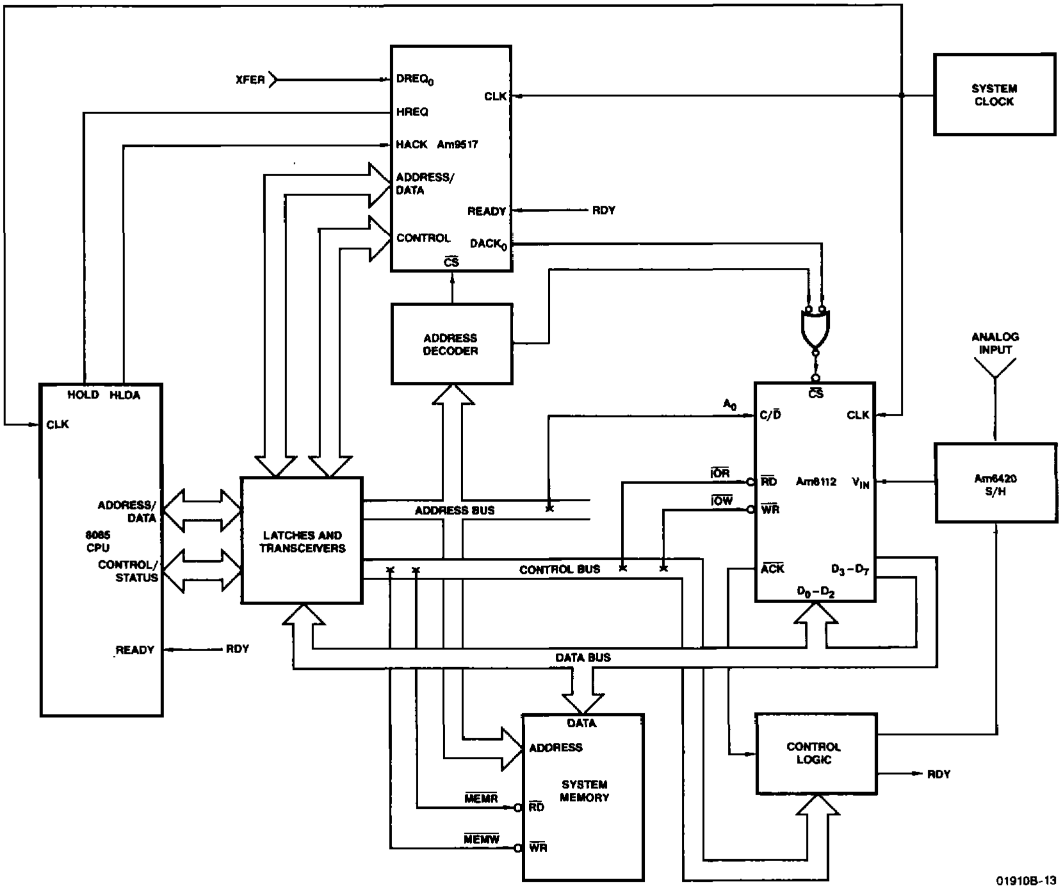
Am6112 with DMA in an 8-Bit System

The 8-bit output data structure of the Am6112 enables it to be easily designed into 8-bit CPU systems. In minimum system configuration with DMA capability, the 8085 CPU programs the Am6112 to operate in Modes 0, 1, 2 or 3 (Figure 4). Except for Mode 2, the CPU controls the conversion cycles and the transfer of data, which can then be stored in the internal register for immediate processing or in system memory for the case of data collection.

The $\overline{ACK}$ of the A/D converter is fed into the CONTROL LOGIC and controls the READY input of the 8085 and the Am9517A DMA controller. This is done to insert Wait states when the Am6112 conversion cycle is longer than the 8085 I/O instruction cycle. The $\overline{ACK}$ signal also controls the Am6420 Sample (track) and Hold (S/H) so that while it is HIGH the S/H is in the HOLD mode, and when it goes LOW the S/H is set to the tracking or sampling mode.

Whenever a DMA transfer is requested on channel 0, the Am9517A responds by setting the HREQ line HIGH to tell the 8085 that it wants to control the bus. The microprocessor relinquishes its control of the bus by making the Hold Acknowledge (HLDA) active. The microprocessor is then basically disabled, and the Am9517A provides all the signals necessary to control the DMA transfer process.

Figure 4. Am6112 In Minimum 8-Bit System Configuration with DMA Capability



01910B-13

Am6112 data transfer may be controlled by CPU (mode 0, -1, -3) or by the Am9517 DMA controller (mode 2) for faster throughput rate.

The DMA controller has four channels ($DREQ_0 - DRE_3$) where four peripheral devices may request service. Each channel has four 16-bit registers (base and current address, and base and current word count) and a mode register accessible via address lines $A_0 - A_3$. The base registers allow the channels to be automatically reinitialized at the end of a DMA transfer, and DMA requests may be either hardware- or software-generated. Auto-initialization is selected by programming the mode register. Other internal registers are programmed to set the desired operations and options.

Among the Am9517 operating modes are two called Single Transfer and Block Transfer. In the Single Transfer mode, a word is transferred for each DMA request, while Block Transfer allows the Am9517A to make continuous transfer until the word count for the active channel goes to zero.

High-Speed Analog I/O Processing

Because the Am9517A cannot control the buses concurrently with the 8085 microprocessor, the microprocessor is idle while DMA transfer is in progress. For large data block transfers, this period can be very significant even though the transfer rate is extremely fast.

The limitation associated with the shared-bus structured can be solved by dedicating a device, such as another microprocessor, to deal with the Am6112 and other I/O devices in conjunction with the main microprocessor. However, most general purpose microprocessor's are not really suited for the task of I/O device control and processing will probably still need a DMA controller to provide DMA capability.

A more powerful and attractive solution uses a dedicated device such as the Am8089 I/O processor (IOP). The Am8089 IOP contains two independent channels with high-speed DMA capability, and its instruction set is extensively I/O-oriented. The bus organization of the IOP is flexible so that data transaction is possible between 8-bit organized I/O devices and 16-bit wide memory or vice versa.

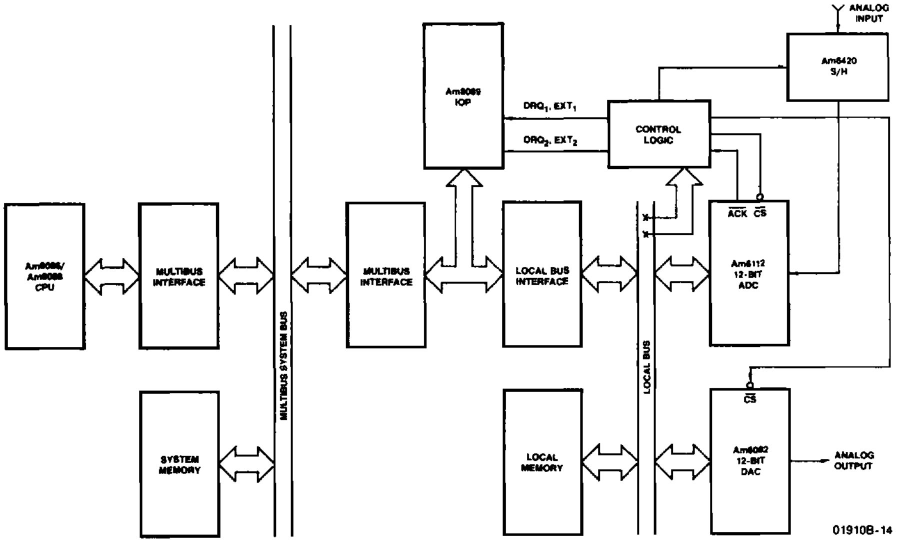
Figure 5 illustrates such a system architecture for high-speed analog I/O processing. Before being able to perform I/O tasks, the Am8089 must be initialized by the Am8086/88 microprocessor, configured in MAXIMUM mode. The system bus is separated from the local bus to allow for parallel processing, and the IOP's channel program may reside in the local memory space to further reduce system bus contention. The Am6112 may be initialized by the IOP, and data transactions from the Am6112, Am6082 and local memory is then confined by the Am8089 to the local bus. DMQ_1 and DMQ_2 are DMA request lines associated with the Am6112 and the Am6082. DMA transfers may be terminated externally via EXT_1 and EXT_2.

High-Resolution System Design Guidelines

The design of high-resolution or low-level analog/digital systems must include a thorough analysis of conditions that can degrade overall system accuracy. Consider the source impedance of the device driving the input of the Am6112. The input impedance of the converter is modulated during the conversion cycle because currents of different values appear at the node where the ADC presents itself as a load to the S/H device. The output impedance of the S/H must be sufficiently low at all operating frequencies to avoid errors and, in addition, the S/H device output must settle to the required voltage level before a bit current comparison can be made. This means that the output transient response of the S/H must be able to cope with the 1/2 clock period settling time requirement for each bit current comparison.

Additional system errors can be caused by improper placement of the circuit components. Analog and digital components must be isolated from each other with lots of ground plane. Analog circuits must be as close together as possible to make the signal paths as short as possible. Ground loops within the analog section must be avoided.

Figure 5. High-Speed Analog I/O Processing



Separate local bus for the analog I/O devices allows for high throughput without sacrificing CPU capabilities. Am8089 does all I/O related routine in parallel with CPU tasks and eliminates system bus contention due to I/O servicing.