HN624416N Series

1048576-word × 16-bit/2097152-word × 8-bit CMOS Mask Programmable ROM

HITACHI

ADE-203-465A (Z)
Rev. 1.0
May 22, 1997

Description

The Hitachi HN624416N series is a 16-Mbit CMOS mask-programmable ROM organized either as 1048576-word × 16-bit or 2097152-word × 8-bit. As it has realized high speed normal access 120 ns and page mode access 50 ns, it is the most suitable to the program and data memory for micro computer system. It has package variations of standard 42-pin plastic DIP, standard 44-pin plastic SOP and standard 44-pin plastic TSOP.

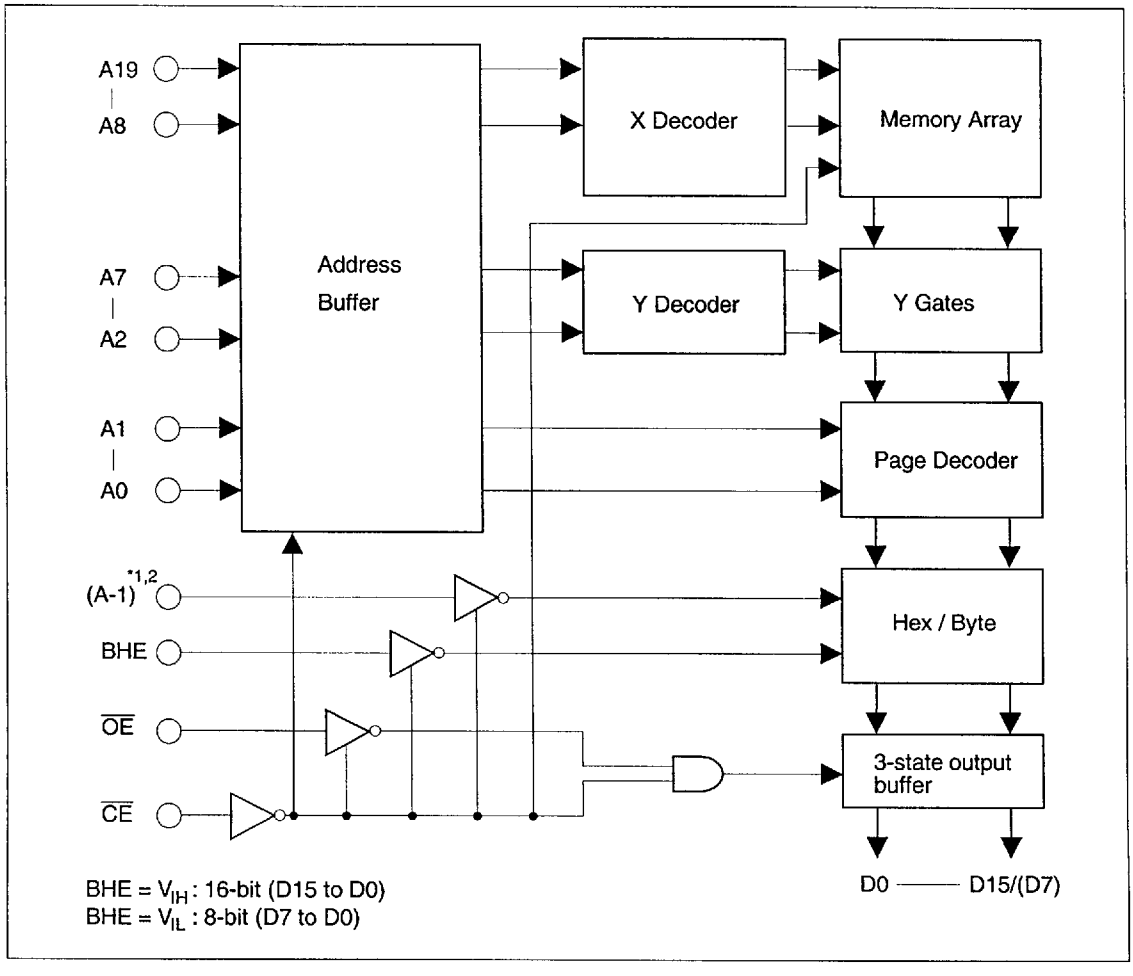
Features

- Single 5 V supply: 5.0 V ± 10%
- Access time:
  - — Normal access time: 120 ns (max)
  - — Page access time: 50 ns (max)
- Power dissipation
  - — Active: 660 mW (max)
  - — Standby: 165 µW (max)
- Byte-wide or word-wide data organization with byte/word selection (BHE)
- 4-word page access on word-wide mode
- 8-byte page access on byte-wide mode
- Three-state data output for wired or-tying
- Directly TTL compatible all inputs and outputs

Ordering Information

Type No.	Access time	Package
HN624416NP-12	120 ns	600mil 42-pin plastic DIP (DP-42)
HN624416NFB-12	120 ns	600mil 44-pin plastic SOP (FP-44D)
HN624416NTT-12	120 ns	400mil 44-pin plastic TSOP II (TTP-44D)

Pin Arrangement

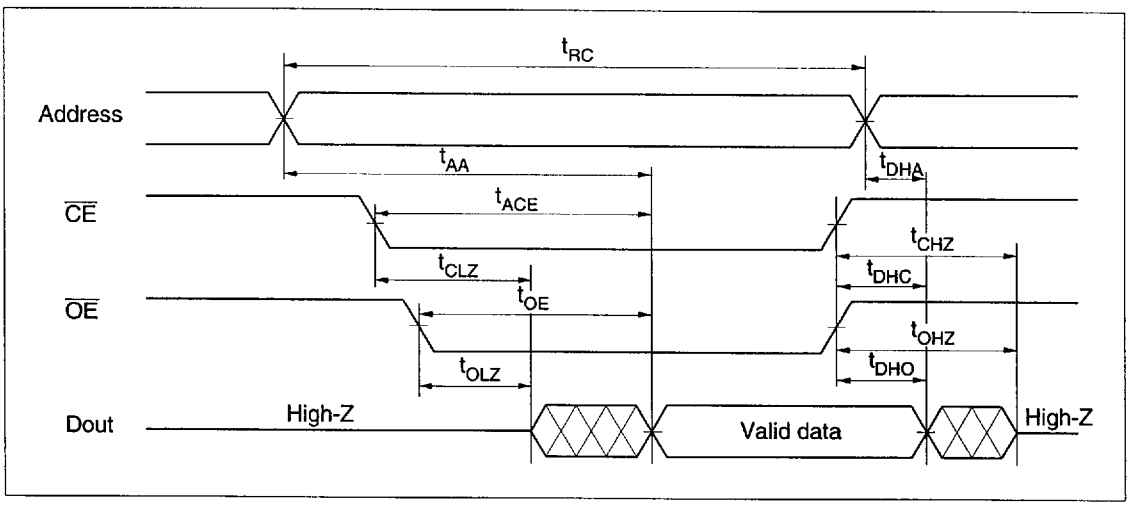


Pin Description

Pin name	Function
A2 to A19	Address input
A-1, A0, A1	Page address input
D0 to D15	Data output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

Block Diagram

Notes: 1. A-1 is least significant address.
2. When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.



Operation Table

Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	Data output D0-D7	Data output D8-D15	Address input LSB	Address input MSB
Standby	H	×*1	×	×	High-Z	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Note: 1. ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.3 to +7.0	V
All input and output voltage relative to V_{SS}	Vin, Vout	–0.3 to V_{CC} +0.3	V
Operating temperature range	Topr	0 to 70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–20 to +85	°C

DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Operating V_{CC} current	I_{CC}	—	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 120 ns
Standby V_{CC} current	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE}$ = 2.2 V
Input leakage current	$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output high voltage	V_{OH}	2.4	—	V	I_{OH} = –205 µA
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance	Cin	—	10	pF
Output capacitance	Cout	—	15	pF

AC Characteristics (V_{CC} = 5.5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Condition

- Input pulse levels: 0.4 to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1TTL + C_L = 100 pF (including jig)

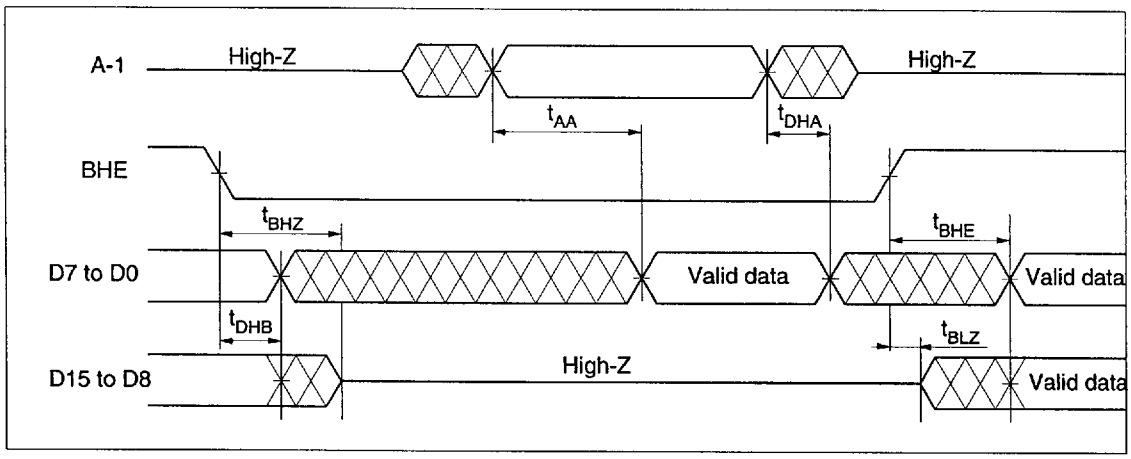
Read Cycle

Parameter	Symbol	HN624416N-12 Min	HN624416N-12 Max	Unit	Note
Read cycle time	t_{RC}	120	—	ns	
Page read cycle time	t_{PC}	50	—	ns	
Address access time	t_{AA}	—	120	ns	3
Page address access time	t_{PA}	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	ns	3
$\overline{OE}$ access time	t_{OE}	—	50	ns	3
BHE access time	t_{BHE}	—	120	ns	
Output hold time from address change	t_{DHA}	5	—	ns	2
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	2
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	4
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	ns	

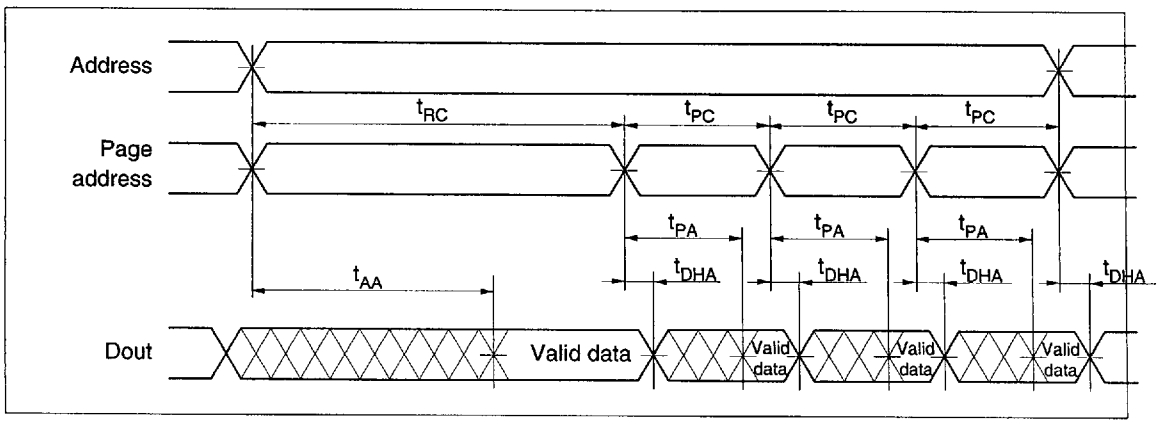
Notes:
1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
2. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
3. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
4. t_{CLZ}, t_{OLZ}: Determined by slower.
5. $\overline{CE}$ and $\overline{OE}$ are enable A19 to A0 are valid.
6. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must be applied to them.
7. Page address is determined as below.
   Word mode (BHE = 'V_{IH}'): A0, A1
   Byte mode (BHE = 'V_{IL}'): A-1, A0, A1
8. $\overline{CE}$ and $\overline{OE}$ are enable.
9. This device is used ATD (Address Transient Detector). Therefore, transfer either $\overline{CE}$ or address (A2 to A19) after power up to 4.5 V.

Timing Waveforms

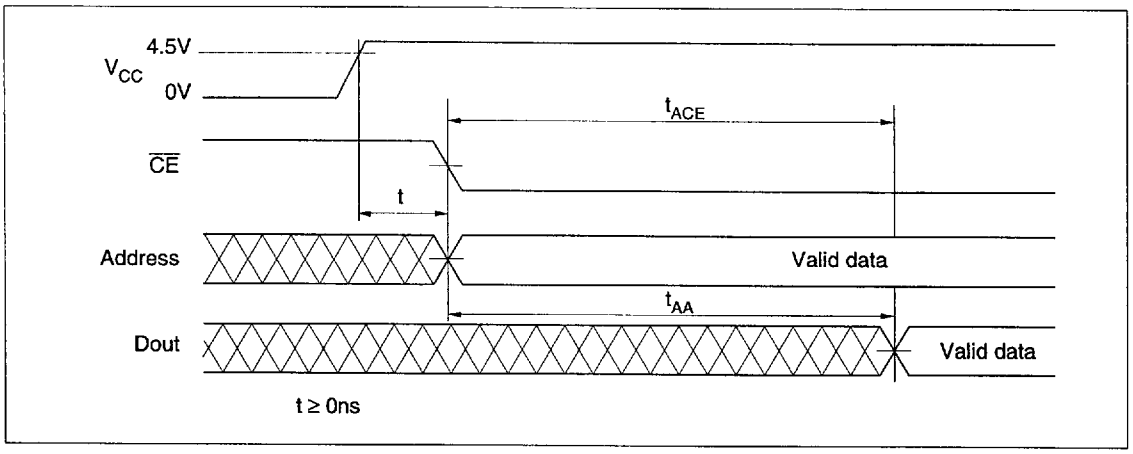
Word Mode (BHE = 'V_{IH}') **or Byte Mode** (BHE = 'V_{IL}')*[2, 3, 4]



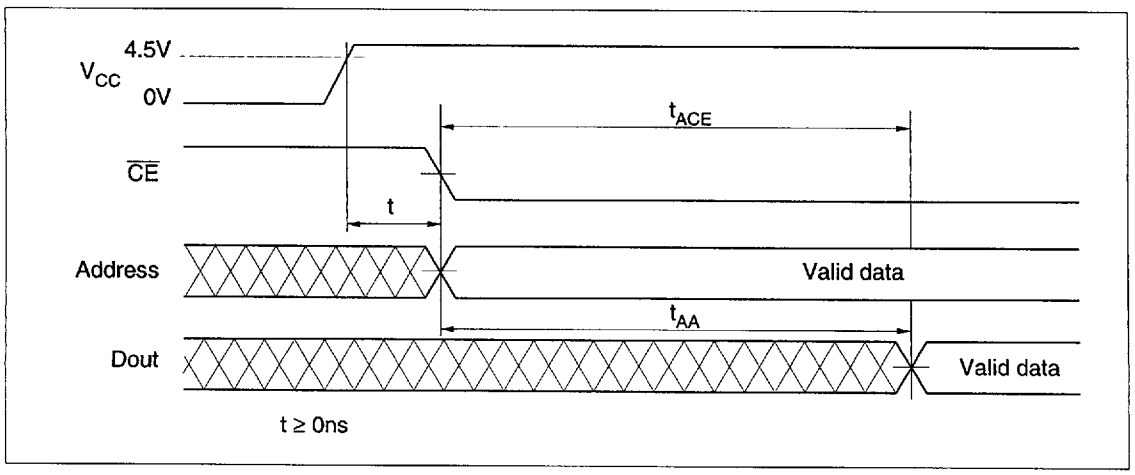
Word Mode, Byte Mode Switch*[5, 6]



Page Mode[*7, 8]



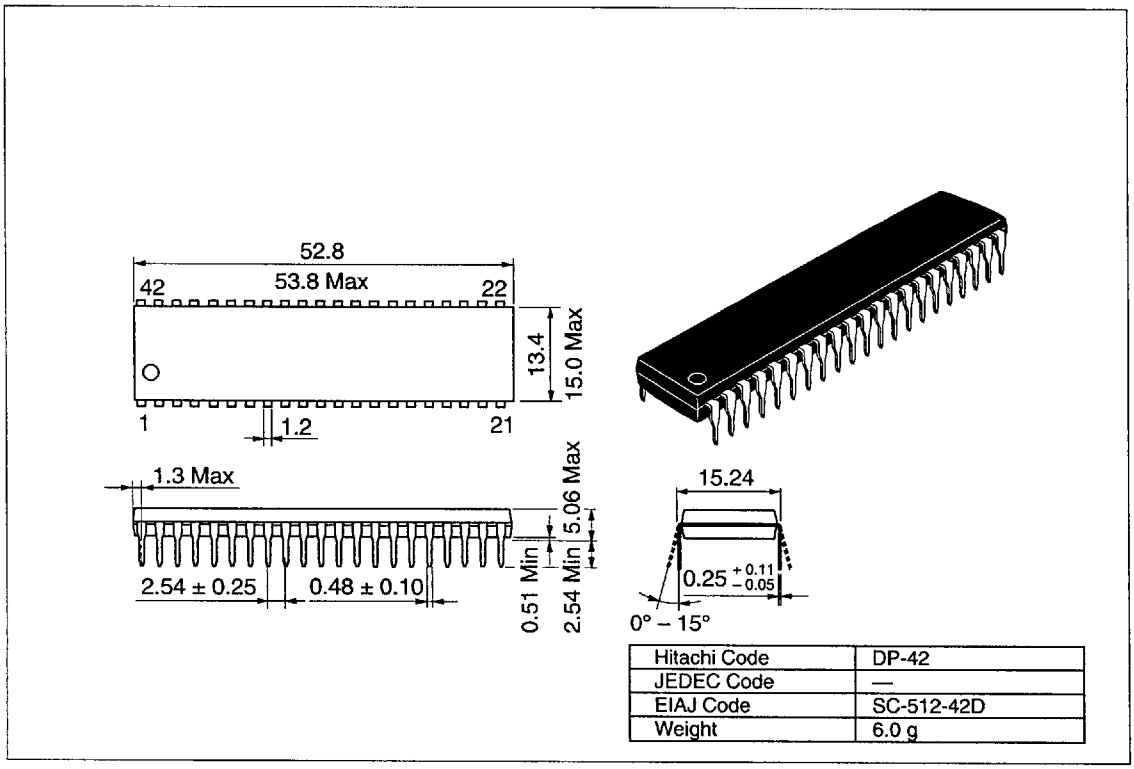
Power Up Sequence[*9]



Package Dimensions

HN624416NP Series (DP-42)

Unit: mm

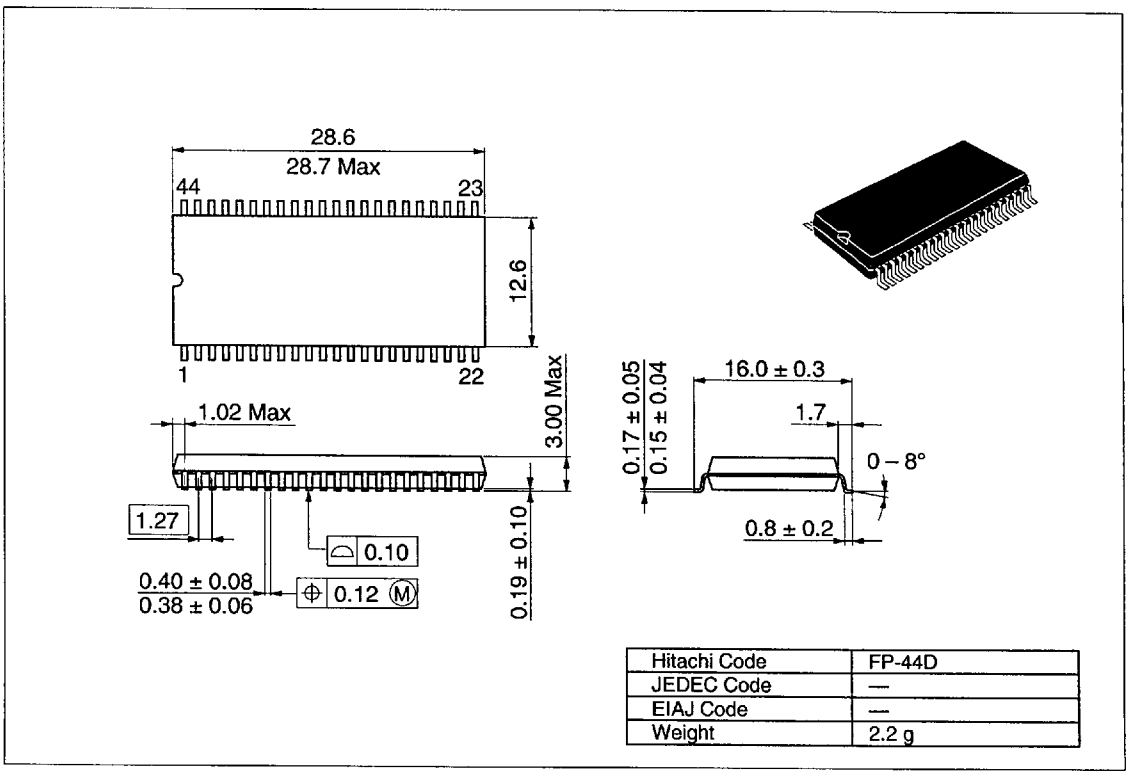


Hitachi Code	DP-42
JEDEC Code	—
EIAJ Code	SC-512-42D
Weight	6.0 g

Package Dimensions (cont.)

HN624416NFB Series (FP-44D)

Unit: mm

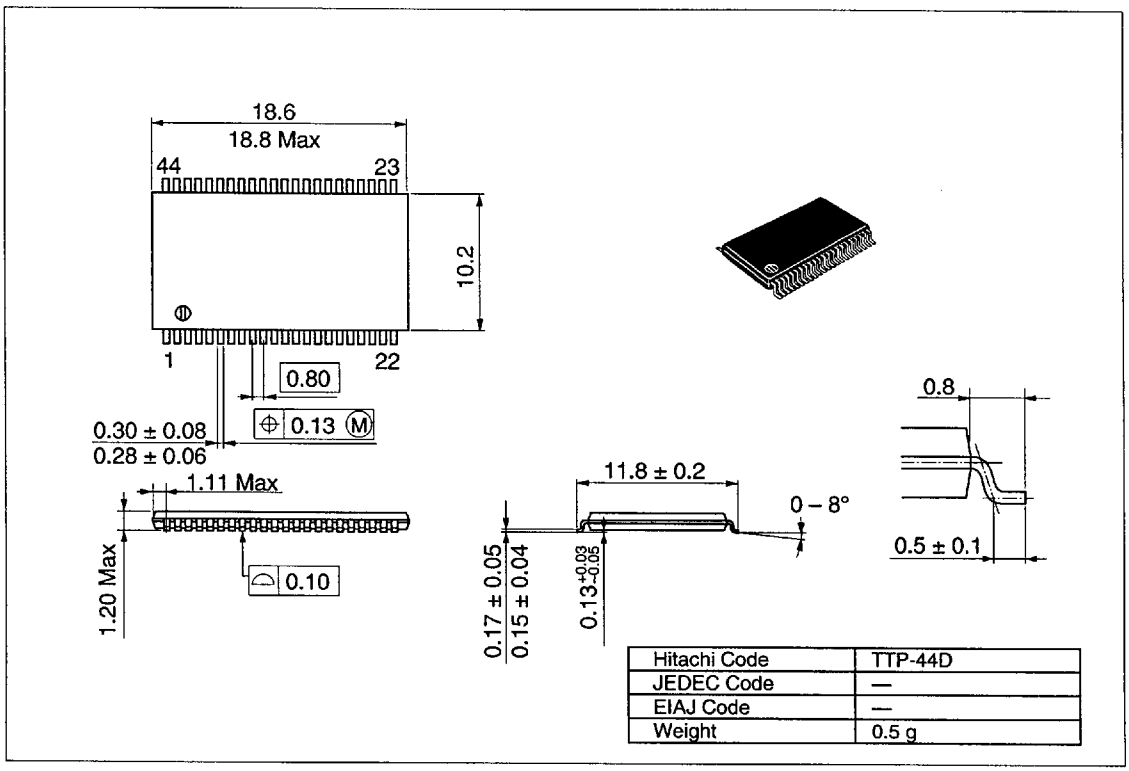


Hitachi Code	FP-44D
JEDEC Code	—
EIAJ Code	—
Weight	2.2 g

Package Dimensions (cont.)

HN624416NTT Series (TTP-44D)

Unit: mm



Hitachi Code	TTP-44D
JEDEC Code	—
EIAJ Code	—
Weight	0.5 g

Datasheet Title

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 18, 1997	Initial issue	Y. Nakamura	H. Moriuchi
1.0	May. 22, 1997	Change of format Deletion of HN62448N-10		