



Integrated Device Technology, Inc.

3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH162270 ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH162270:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This registered bus exchanger is built using advanced

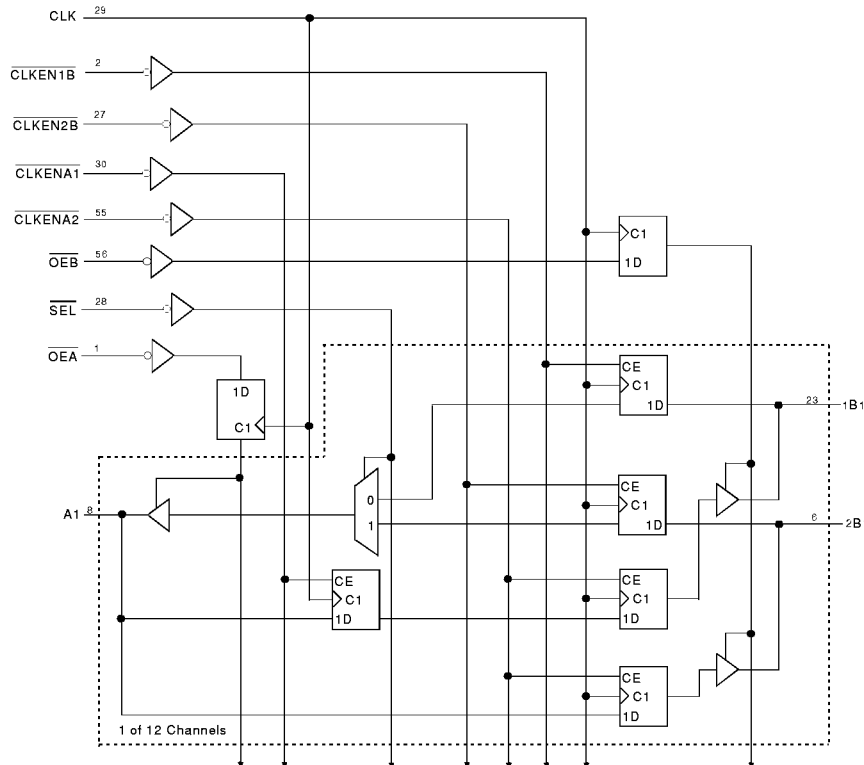
dual metal CMOS technology. The ALVCH162270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

This device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OE_A}$ and $\overline{OE_B}$). The control terminals are registered to synchronize the bus-direction changes with CLK.

The ALVCH162270 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

The ALVCH162270 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

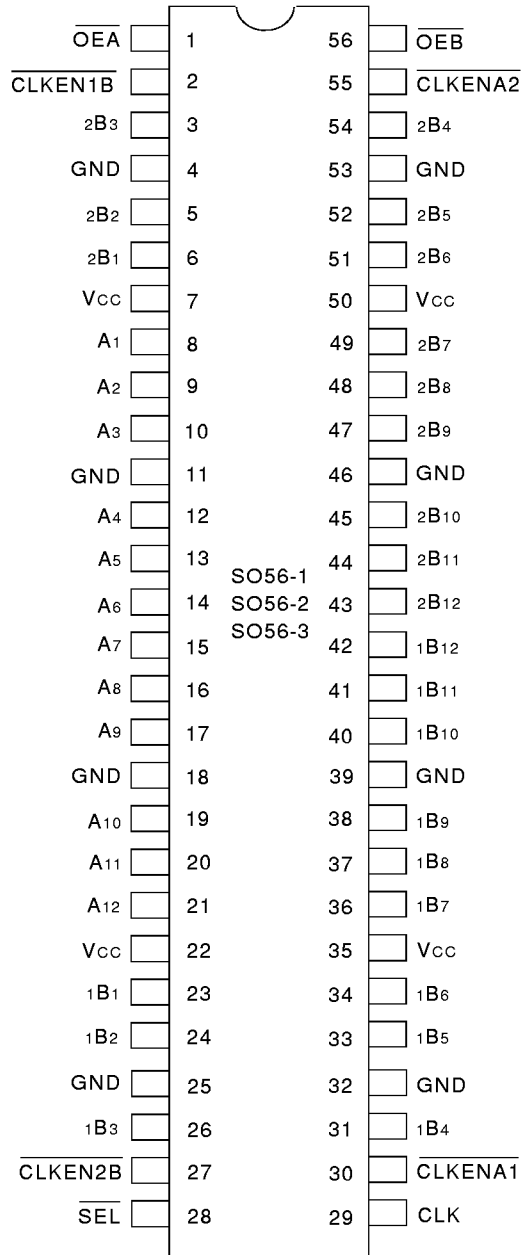


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EXTENDED COMMERCIAL TEMPERATURE RANGE

JANUARY 1999

PIN CONFIGURATIONS



**SSOP/TSSOP/TVSOP
TOP VIEW**

FUNCTION TABLES⁽¹⁾

OUTPUT ENABLE

| Inputs | | | Outputs | |
|--------|------------------|------------------|---------|----------|
| CLK | \overline{OEA} | \overline{OEB} | Ax | 1Bx, 2Bx |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

A-TO-B STORAGE ($\overline{OEB} = L$ AND $\overline{OEA} = H$)

| Inputs | | | Outputs | | |
|---------|---------|-----|---------|--------------------|--------------------|
| CLKENA1 | CLKENA2 | CLK | Ax | 1Bx | 2Bx |
| L | H | X | X | 1Bo ⁽²⁾ | 2Bo ⁽²⁾ |
| L | H | X | X | 1Bo ⁽²⁾ | 2Bo ⁽²⁾ |
| L | L | ↑ | L | L ⁽³⁾ | L |
| L | L | ↑ | H | H ⁽³⁾ | H |
| H | L | ↑ | L | 1Bo ⁽²⁾ | L |
| H | L | ↑ | H | 1Bo ⁽²⁾ | H |
| H | H | X | X | 1Bo ⁽²⁾ | 2Bo ⁽²⁾ |

B-TO-A STORAGE ($\overline{OEA} = L$ AND $\overline{OEB} = H$)

| Inputs | | | | | | Outputs |
|---------|---------|-----|-----|-----|-----|-------------------|
| CLKEN1B | CLKEN2B | CLK | SEL | 1Bx | 2Bx | Ax |
| H | X | X | H | X | X | Ao ⁽²⁾ |
| X | H | X | L | X | X | Ao ⁽²⁾ |
| L | X | ↑ | H | L | X | L |
| L | X | ↑ | H | H | X | H |
| X | L | ↑ | L | X | L | L |
| X | L | ↑ | L | X | H | H |

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established.
3. Two CLK edges are needed to propagate data.

PIN DESCRIPTION

| Pin Names | I/O | Description |
|-----------------------------|-----|---|
| Ax(1:12) | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. ⁽¹⁾ |
| 1Bx(1:12) | I/O | Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. ⁽¹⁾ |
| 2Bx(1:12) | I/O | Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. ⁽¹⁾ |
| CLK | I | Clock Input |
| $\overline{\text{CLKENA1}}$ | I | Clock Enable Input for the A-1B Register. If $\overline{\text{CLKENA1}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW). |
| $\overline{\text{CLKENA2}}$ | I | Clock Enable Input for the A-2B Register. If $\overline{\text{CLKENA2}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW). |
| $\overline{\text{CLKEN1B}}$ | I | Clock Enable Input for the 1B-A Register. If $\overline{\text{CLKEN1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW). |
| $\overline{\text{CLKEN2B}}$ | I | Clock Enable Input for the 2B-A Register. If $\overline{\text{CLKEN2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW). |
| $\overline{\text{SEL}}$ | I | 1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 2B Port to A Port. |
| $\overline{\text{OEA}}$ | I | Synchronous Output Enable for A Port (Active LOW) |
| $\overline{\text{OEB}}$ | I | Synchronous Output Enable for B Port (Active LOW) |

NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING⁽¹⁾

| Symbol | Description | Max. | Unit |
|----------------------------------|--|--------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | - 0.5 to + 4.6 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | - 0.5 to V _{CC} + 0.5 | V |
| T _{STG} | Storage Temperature | - 65 to + 150 | °C |
| I _{OUT} | DC Output Current | - 50 to + 50 | mA |
| I _{IK} | Continuous Clamp Current, V _I < 0 or V _I > V _{CC} | ± 50 | mA |
| I _{OK} | Continuous Clamp Current, V _O < 0 | - 50 | mA |
| I _{CC} | Continuous Current through each V _{CC} or GND | ±100 | mA |

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

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NOTE:

1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|--|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ± 5 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ± 5 | |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = V _{CC} | — | — | ± 10 | μA |
| | | | V _O = GND | — | — | ± 10 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | | — | 0.1 | 40 | μA |
| V _{IN} = GND or V _{CC} | | | | | | | |
| ΔI _{CC} | | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | | | |

NOTE:1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

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BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|--|----------------------------------|------------------------|----------------------------|------|---------------------|-------|------|
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 3.0V | V _I = 2.0V | -75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | -45 | — | — | μA |
| | | | V _I = 0.7V | 45 | — | — | |
| I _{BHHO} I _{BHLO} | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ± 500 | μA |

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

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OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|------------------------|------------------------|--------------------------------|--------------------------|--------------------------------|-------------------------|------|
| VOH | Output HIGH Voltage | V _{CC} = 2.3V to 3.6V | I _{OH} = -0.1mA | V _{CC} - 0.2 | — | V |
| | | V _{CC} = 2.3V | I _{OH} = -4mA | 1.9 | — | |
| | | | I _{OH} = -6mA | 1.7 | — | |
| | | V _{CC} = 2.7V | I _{OH} = -4mA | 2.2 | — | |
| | | | I _{OH} = -8mA | 2 | — | |
| | | V _{CC} = 3.0V | I _{OH} = -6mA | 2.4 | — | |
| | | | I _{OH} = -12mA | 2 | — | |
| | | VOL | Output LOW Voltage | V _{CC} = 2.3V to 3.6V | I _{OL} = 0.1mA | |
| V _{CC} = 2.3V | I _{OL} = 4mA | | | — | 0.4 | |
| | I _{OL} = 6mA | | | — | 0.55 | |
| V _{CC} = 2.7V | I _{OL} = 4mA | | | — | 0.4 | |
| | I _{OL} = 8mA | | | — | 0.6 | |
| V _{CC} = 3.0V | I _{OL} = 6mA | | | — | 0.55 | |
| | I _{OL} = 12mA | | | — | 0.8 | |

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

| Symbol | Parameter | Test Conditions | V _{CC} = 2.5V ± 0.2V | V _{CC} = 3.3V ± 0.3V | Unit |
|--------|---|---------------------------------|-------------------------------|-------------------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance Outputs enabled | C _L = 0pF, f = 10Mhz | — | — | pF |
| CPD | Power Dissipation Capacitance Outputs disabled | | — | — | pF |

SWITCHING CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | V _{CC} = 2.5V ± 0.2V | | V _{CC} = 2.7V | | V _{CC} = 3.3V ± 0.3V | | Unit |
|--------------------------------------|--|-------------------------------|------|------------------------|------|-------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PLH} t _{PHL} | Propagation Delay CLK to xBx | 2.5 | 6.9 | — | 6.4 | 1.7 | 5.6 | ns |
| t _{PLH} t _{PHL} | Propagation Delay CLK to Ax | 2.2 | 6.4 | — | 6 | 1.6 | 5.2 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{SEL} to Ax | 2.4 | 7.2 | — | 7 | 1.6 | 6 | ns |
| t _{PZH} t _{PZL} | Output Enable Time CLK to Ax or Bx | 2.1 | 7.9 | — | 7.4 | 1.6 | 6.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time CLK to Ax or Bx | 3 | 7.8 | — | 7.1 | 1.7 | 6.2 | ns |
| t _{SU} | Setup Time, Ax data before CLK \uparrow | 4.1 | — | 3.8 | — | 3.1 | — | ns |
| t _{SU} | Setup Time, Bx data before CLK \uparrow | 0.9 | — | 1.2 | — | 0.9 | — | ns |
| t _{SU} | Setup Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK \uparrow | 3.5 | — | 3.2 | — | 2.7 | — | ns |
| t _{SU} | Setup Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ before CLK \uparrow | 3.4 | — | 3 | — | 2.6 | — | ns |
| t _{SU} | Setup Time, \overline{OEB} or \overline{OEA} before CLK \uparrow | 4.4 | — | 3.9 | — | 3.2 | — | ns |
| t _H | Hold Time, Ax data after CLK \uparrow | 0 | — | 0 | — | 0.2 | — | ns |
| t _H | Hold Time, Bx data after CLK \uparrow | 1.4 | — | 1 | — | 1.7 | — | ns |
| t _H | Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK \uparrow | 0 | — | 0.1 | — | 0.3 | — | ns |
| t _H | Hold Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ after CLK \uparrow | 0 | — | 0 | — | 0.6 | — | ns |
| t _H | Hold Time, \overline{OEB} or \overline{OEA} after CLK \uparrow | 0 | — | 0 | — | 0.1 | — | ns |
| t _w | Pulse Width, CLK HIGH or LOW | 3.3 | — | 3.3 | — | 3.3 | — | ns |
| t _{SK(o)} | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps |

NOTES:

1. See test circuits and waveforms. T_A = -40°C to +85°C.

2. Skew between any two outputs of the same package and switching in the same direction.

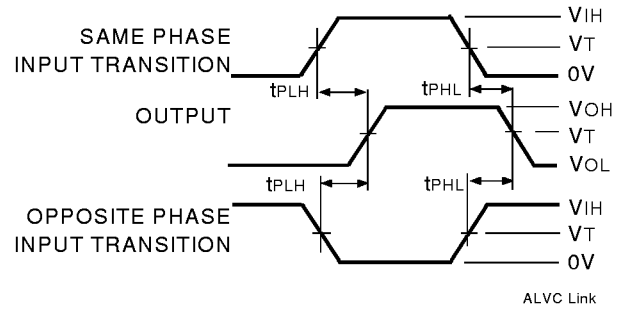
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

| Symbol | Vcc ⁽¹⁾ = 3.3V±0.3V | Vcc ⁽¹⁾ = 2.7V | Vcc ⁽²⁾ = 2.5V±0.2V | Unit |
|-------------------|--------------------------------|---------------------------|--------------------------------|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| CL | 50 | 50 | 30 | pF |

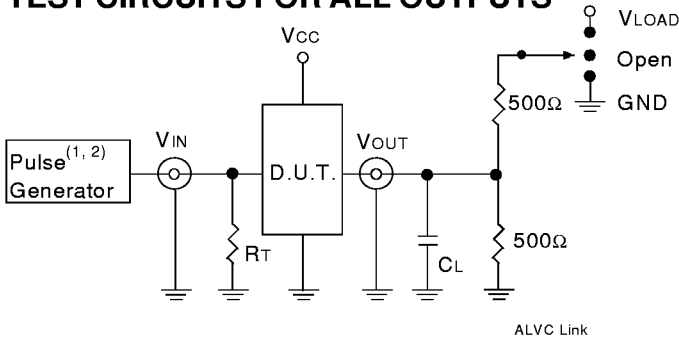
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

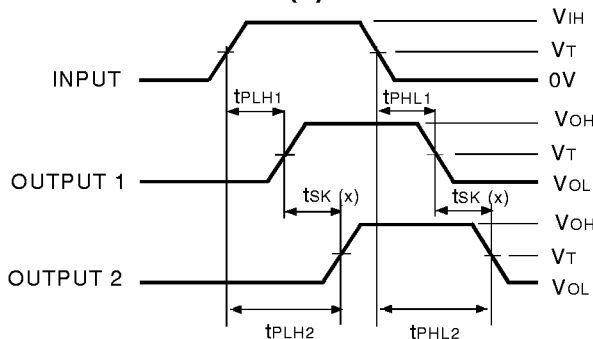
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION:

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other tests | Open |

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OUTPUT SKEW - t_{SK}(x)



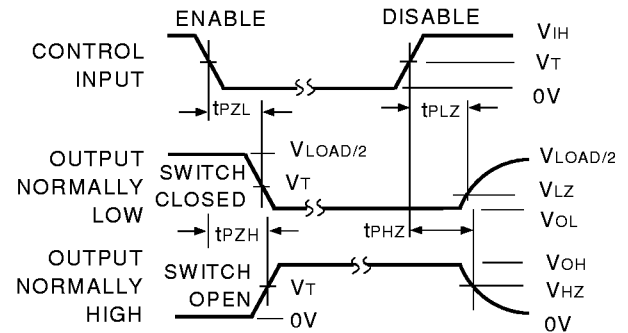
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

ENABLE AND DISABLE TIMES

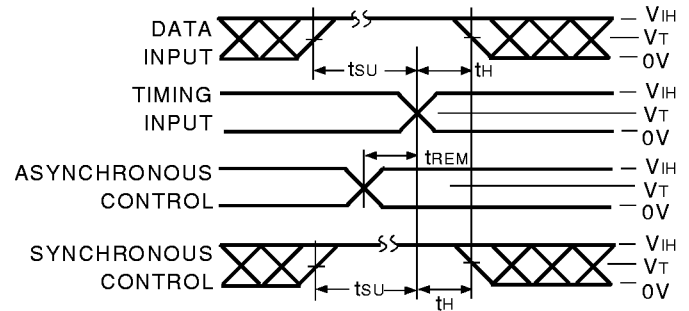


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NOTE:

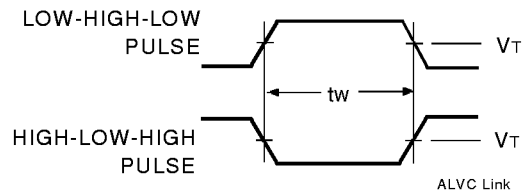
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

| IDT | XX | ALVC | X | XX | XXX | XX | |
|-------------|----------|--------|-------------|---------|-----|----|--|
| Temp. Range | Bus-Hold | Family | Device Type | Package | | | |
| | | | | | | | PV Shrink Small Outline Package (SO56-1) |
| | | | | | | | PA Thin Shrink Small Outline Package (SO56-2) |
| | | | | | | | PF Thin Very Small Outline Package (SO56-3) |
| | | | | | | | 270 12-Bit To 24-Bit Registered Bus Exchanger With 3-State Outputs |
| | | | | | | | 162 Double-Density, ±12mA |
| | | | | | | | H Bus-hold |
| | | | | | | | 74 -40°C to +85°C |