

8M X 32 DRAM Card

FEATURES

- Performance range:

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
STI328000C2-60V	60ns	15ns	110ns
STI328000C2-70V	70ns	20ns	130ns

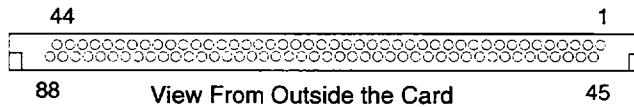
- Dimensions—2.13" wide x 3.37" long x 0.13" thick
- Meets specifications for JEDEC and JEIDA 88-pin DRAM cards
- 88-pin, two piece connector with keying
- PDx pins for card configuration information
- CBR, RAS only, or Hidden refresh capability
- Normal or Self-refresh options
- 2048 cycles/32ms refresh
- 3.3V power supply

GENERAL DESCRIPTION

The Simple Technology STI328000C2 is a 8M bit x 32 Dynamic RAM high density memory card. The Simple Technology STI328000C2 consist of sixteen CMOS 4M x 4 bit DRAMs in 24-pin SOJ package. The circuit board is enclosed in a credit-card sized frame and 88-pin connector package as specified for JEDEC and JEIDA standard card packaging.

The card's small package size makes it suitable for use in small portable computers, palmtops, etc. System memory upgrades are simplified due to the fact that the system box does not need to be opened or otherwise disassembled.

PIN CONFIGURATION



0066

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>SS</sub>	23	CAS <sub>0</sub>	45	V <sub>SS</sub>	67	V <sub>SS</sub>
2	DQ <sub>0</sub>	24	CAS <sub>1</sub>	46	DQ <sub>16</sub>	68	CAS <sub>3</sub>
3	DQ <sub>1</sub>	25	V <sub>CC</sub>	47	DQ <sub>17</sub>	69	RAS <sub>3</sub>
4	DQ <sub>2</sub>	26	RAS <sub>2</sub>	48	DQ <sub>18</sub>	70	W
5	DQ <sub>3</sub>	27	NC	49	DQ <sub>19</sub>	71	PD <sub>1</sub>
6	DQ <sub>4</sub>	28	PD <sub>2</sub>	50	DQ <sub>20</sub>	72	PD <sub>3</sub>
7	DQ <sub>5</sub>	29	PD <sub>4</sub>	51	DQ <sub>21</sub>	73	V <sub>SS</sub>
8	DQ <sub>6</sub>	30	PD <sub>6</sub>	52	DQ <sub>22</sub>	74	PD <sub>5</sub>
9	NC	31	NC	53	DQ <sub>23</sub>	75	PD <sub>7</sub>
10	DQ <sub>7</sub>	32	NC	54	NC	76	PD <sub>8</sub>
11	V <sub>CC</sub>	33	NC	55	NC	77	NC
12	NC	34	DQ <sub>8</sub>	56	V <sub>SS</sub>	78	NC
13	A <sub>0</sub>	35	V <sub>CC</sub>	57	A <sub>1</sub>	79	NC
14	A <sub>2</sub>	36	DQ <sub>9</sub>	58	A <sub>3</sub>	80	DQ <sub>24</sub>
15	NC	37	NC	59	A <sub>5</sub>	81	DQ <sub>25</sub>
16	A <sub>4</sub>	38	DQ <sub>10</sub>	60	A <sub>7</sub>	82	DQ <sub>26</sub>
17	V <sub>CC</sub>	39	DQ <sub>11</sub>	61	A <sub>9</sub>	83	DQ <sub>27</sub>
18	A <sub>6</sub>	40	DQ <sub>12</sub>	62	NC	84	DQ <sub>28</sub>
19	A <sub>8</sub>	41	DQ <sub>13</sub>	63	V <sub>SS</sub>	85	DQ <sub>29</sub>
20	A <sub>10</sub>	42	DQ <sub>14</sub>	64	NC	86	DQ <sub>30</sub>
21	NC	43	DQ <sub>15</sub>	65	RAS <sub>1</sub>	87	DQ <sub>31</sub>
22	RAS <sub>0</sub>	44	V <sub>SS</sub>	66	CAS <sub>2</sub>	88	V <sub>SS</sub>

Pin Names

Pin Name	Pin Function
A <sub>0</sub> -A <sub>10</sub>	Address Inputs
DQ <sub>0</sub> -DQ <sub>31</sub>	Data In/Out
W	Read/Write Input
RAS <sub>0</sub> -RAS <sub>3</sub>	Row Address Strobe
CAS <sub>0</sub> -CAS <sub>3</sub>	Column Address Strobe
PD <sub>1</sub> -PD <sub>8</sub>	Presence Detect
V <sub>CC</sub>	Power (+3.3V)
V <sub>SS</sub>	Ground
NC	No Connection

Presence Detect Pins

PD<sub>1</sub>=V<sub>SS</sub>, PD<sub>2</sub>=V<sub>SS</sub>, PD<sub>3</sub>=NC, PD<sub>4</sub>=V<sub>SS</sub>, for 32 MB Card using 4Mx4 chips and PD<sub>5</sub>=V<sub>SS</sub> for dual bank

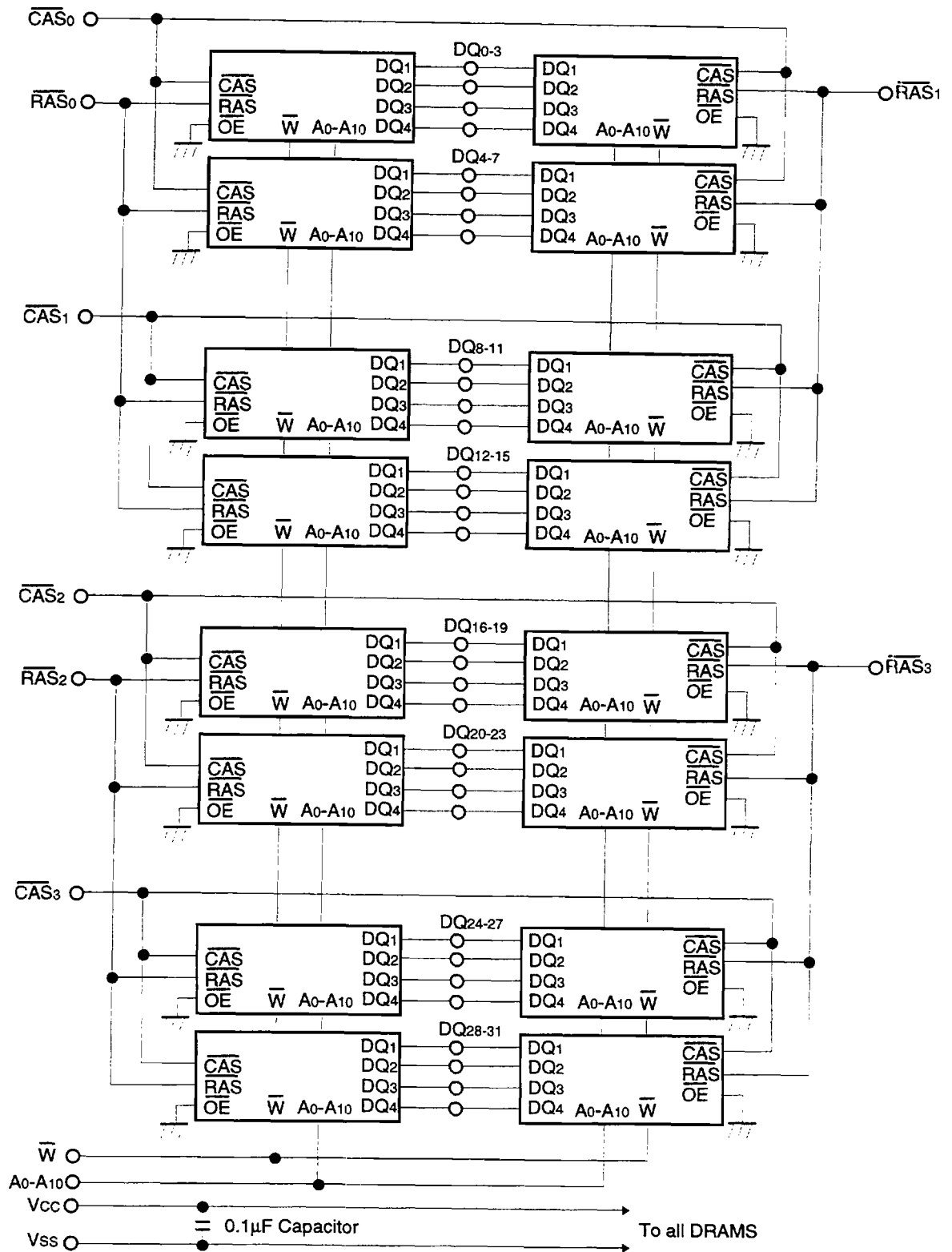
Access Time

Pin	60ns	70ns	80ns
PD <sub>6</sub>	NC	V <sub>SS</sub>	NC
PD <sub>7</sub>	NC	NC	V <sub>SS</sub>

Refresh Type

Pin	Slow Refresh	Self-Refresh
PD <sub>8</sub>	NC	V <sub>SS</sub>

FUNCTIONAL BLOCK DIAGRAM



0048M

**ABSOLUTE MAXIMUM RATINGS\***

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to $+V_{CC}+0.5$	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-1 to +4.6	V
Storage Temperature	$T_{stg}$	-55 to +150	°C
Power Dissipation	$P_D$	16	W
Short Circuit Output Current	$I_{OS}$	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage reference to  $V_{SS}$ ,  $T_A=0$  to  $70^{\circ}\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

**DC AND OPERATION CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* (RAS, CAS, Address Cycling @ $t_{RC}=\text{min.}$ )	STI328000C2-60V	$I_{CC1}$	—	968	mA
	STI328000C2-70V			888	mA
Standby Current (RAS=CAS= $V_{IH}$ )		$I_{CC2}$	—	16	mA
RAS-Only Refresh Current* (CAS= $V_{IH}$ , RAS Cycling @ $t_{RC}=\text{min.}$ )	STI328000C2-60V	$I_{CC3}$	—	968	mA
	STI328000C2-70V			888	mA
Fast Page Mode Current* (RAS= $V_{IL}$ , CAS Cycling: $t_{PC}=\text{min.}$ )	STI328000C2-60V	$I_{CC4}$	—	728	mA
	STI328000C2-70V			648	mA
Standby Current (RAS=CAS= $V_{CC}-0.2\text{V}$ )		$I_{CC5}$	—	8	mA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ $t_{RC}=\text{min.}$ )	STI328000C2-60V	$I_{CC6}$	—	968	mA
	STI328000C2-70V			888	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 3.6\text{V}$ , all other pins not under test=0V)		$I_{IL}$	-160	160	$\mu\text{A}$
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 3.6\text{V}$ )		$I_{OL}$	-20	20	$\mu\text{A}$
Output High Voltage Level ( $I_{OH}=-2\text{mA}$ )		$V_{OH}$	2.4	—	V
Output Low Voltage Level ( $I_{OL}=2\text{mA}$ )		$V_{OL}$	—	0.4	V

\*NOTE:  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  are dependent on output loading and cycling rates. Specified values are obtained with the output open.  $I_{CC}$  is specified as an average current.

CAPACITANCE ( $T_A=25\text{ }^\circ\text{C}$ )

Item	Symbol	Min	Max	Units
Input Capacitance ( $A_0$ - $A_{10}$ )	$C_{IN1}$	—	80	pF
Input Capacitance ( $\overline{W}$ )	$C_{IN2}$	—	112	pF
Input Capacitance ( $\overline{RAS}_0$ , $\overline{RAS}_2$ )	$C_{IN3}$	—	56	pF
Input Capacitance ( $\overline{CAS}_0$ - $\overline{CAS}_3$ )	$C_{IN4}$	—	28	pF
Input/Output Capacitance ( $DQ_{0-31}$ )	$C_{DQ1}$	—	14	pF

AC CHARACTERISTICS ( $0\text{ }^\circ\text{C} \leq T_A \leq 70\text{ }^\circ\text{C}$ ,  $V_{CC}=3.3V \pm 10\%$ , See notes 1, 2)

Parameter	Symbol	-60V		-70V		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	110		130		ns	
Access time from $\overline{RAS}$	$t_{RAC}$		60		70	ns	3, 4
Access time from $\overline{CAS}$	$t_{CAC}$		15		20	ns	3, 4, 5
Access time from column address	$t_{AA}$		30		35	ns	3, 11
$\overline{CAS}$ to output in Low-Z	$t_{CLZ}$	0		0		ns	3
Output buffer turn-off delay	$t_{OFF}$	0	15	0	20	ns	7
Transition time (rise and fall)	$t_T$	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	$t_{RP}$	40		50		ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	15		20		ns	
$\overline{CAS}$ hold time	$t_{CSH}$	60		70		ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	30	15	35	ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{CRP}$	5		5		ns	
Row address set-up time	$t_{ASR}$	0		0		ns	
Row address hold time	$t_{RAH}$	10		10		ns	
Column address set-up time	$t_{ASC}$	0		0		ns	
Column address hold time	$t_{CAH}$	15		15		ns	
Column address hold referenced to $\overline{RAS}$	$t_{AR}$	50		55		ns	6
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	30		35		ns	
Read command set-up time	$t_{RCS}$	0		0		ns	
Read command hold referenced to $\overline{CAS}$	$t_{RCH}$	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	$t_{RRH}$	0		0		ns	9
Write command hold time	$t_{WCH}$	10		15		ns	
Write command hold referenced to $\overline{RAS}$	$t_{WCR}$	45		55		ns	6
Write command pulse width	$t_{WP}$	10		15		ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15		20		ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15		20		ns	
Data-in set-up time	$t_{DS}$	0		0		ns	10
Data-in hold time	$t_{DH}$	15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	$t_{DHR}$	50		55		ns	6
Refresh period	$t_{REF}$		32		32	ms	

continued on the next page

## AC CHARACTERISTICS (continued)

Parameter	Symbol	-60V		-70V		Unit	Notes
		Min	Max	Min	Max		
Write command set-up time	$t_{WCS}$	0		0		ns	8
$\overline{CAS}$ set-up time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	$t_{CSR}$	10		10		ns	
$\overline{CAS}$ hold time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	$t_{CHR}$	10		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	5		5		ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$		35		40	ns	3
Fast Page mode cycle time	$t_{PC}$	40		45		ns	
$\overline{CAS}$ precharge time (fast page)	$t_{CP}$	10		10		ns	
$\overline{RAS}$ pulse width (fast page)	$t_{RASP}$	60	200,000	70	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	$t_{WRP}$	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	$t_{WRH}$	10		10		ns	
$\overline{CAS}$ precharge ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ counter test)	$t_{CPT}$	20		30		ns	

## NOTES

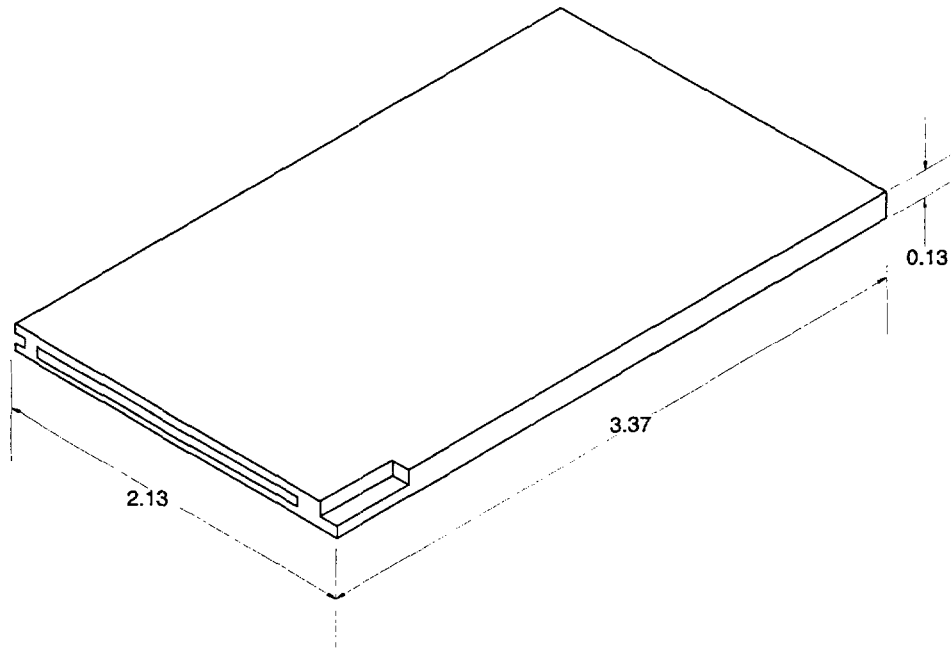
- An initial pause of 200  $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved.
- $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ , and are assumed to be 5ns for all inputs.
- Measure with a load equivalent to 2 TTL loads and 100pF.
- Operation within the  $t_{RCD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Assumes that  $t_{RCD} \geq t_{RCD(max)}$ .
- $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  are referenced to  $t_{RAD(max)}$ .
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ , and  $t_{AWD}$  are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS(min)}$ , the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{W}$  leading edge in read-write cycles.
- Operation within the  $t_{RAD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled by  $t_{AA}$ .

## TIMING DIAGRAMS

Please refer to attached Timing Chart I.

PACKAGE DIMENSIONS

Units: Inches



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TOLERANCES:  $\pm 0.005$  UNLESS OTHERWISE SPECIFIED