

Contents

| | |
|---|-----------|
| GENERAL DESCRIPTION | 1 |
| FEATURES | 1 |
| BLOCK DIAGRAM | 2 |
| PIN CONFIGURATION (TOP VIEW) | 3 |
| PIN DESCRIPTIONS | 4 |
| ABSOLUTE MAXIMUM RATINGS | 6 |
| RECOMMENDED OPERATING CONDITIONS | 6 |
| ELECTRICAL CHARACTERISTICS | 6 |
| DC Characteristics | 6 |
| Analog Characteristics | 7 |
| AC Characteristics | 7 |
| TIMING DIAGRAMS | 8 |
| Reset Timing | 8 |
| Read Timing | 8 |
| Write Timing | 9 |
| DMA Transfer Timing | 10 |
| FUNCTIONAL DESCRIPTION | 11 |
| Voice synthesis method | 11 |
| Data configuration when 8-bit bus is used | 11 |
| Data configuration when 16-bit bus is used | 12 |
| FIFO memory configuration | 13 |
| Playback Data Transfer Flowchart (without DMA transfer) | 19 |
| DMA Control Method | 20 |
| Playback Data Transfer Flowchart (with DMA transfer) | 22 |
| Using External DAC | 23 |
| COMMAND LIST | 24 |
| Description of commands | 26 |
| Description of status | 33 |
| CPU INTERFACE EXAMPLES | 34 |

OKI Semiconductor

MSM9842

Voice Synthesis LSI with Built-in FIFO

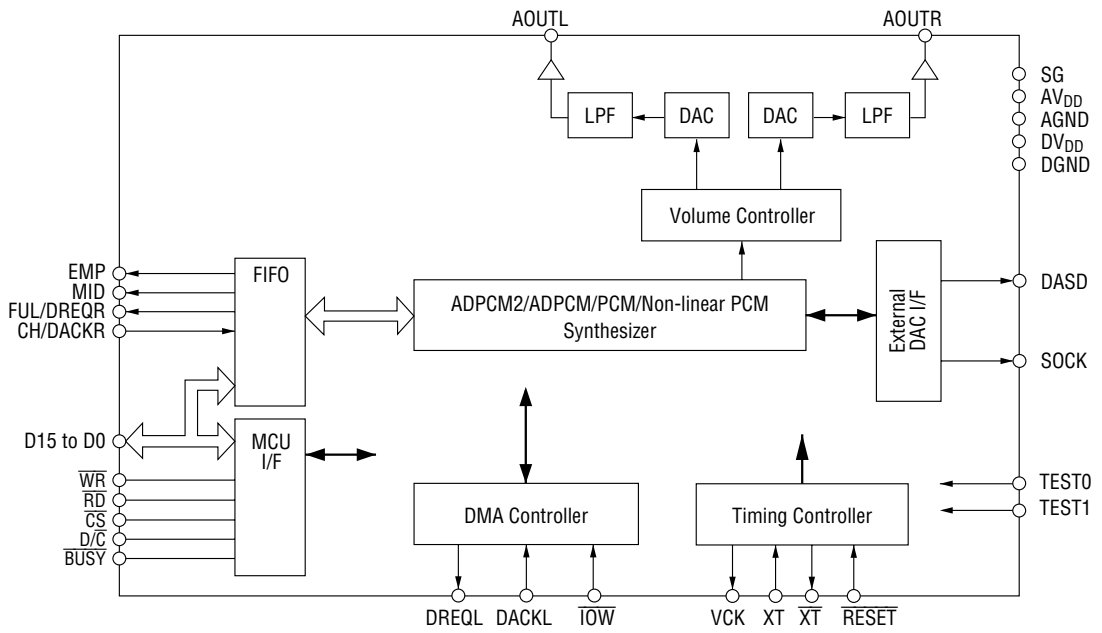
GENERAL DESCRIPTION

The MSM9842 is a mono/stereo playback LSI with a built-in 1K bit FIFO for easy interface with external systems or non-semiconductor memory. It utilizes multiple playback modes, including the new ADPCM2 algorithm, which allows for even higher quality sound reproduction. The playback functions of the MSM9842 are controlled by an MCU via 8/16 bus interface.

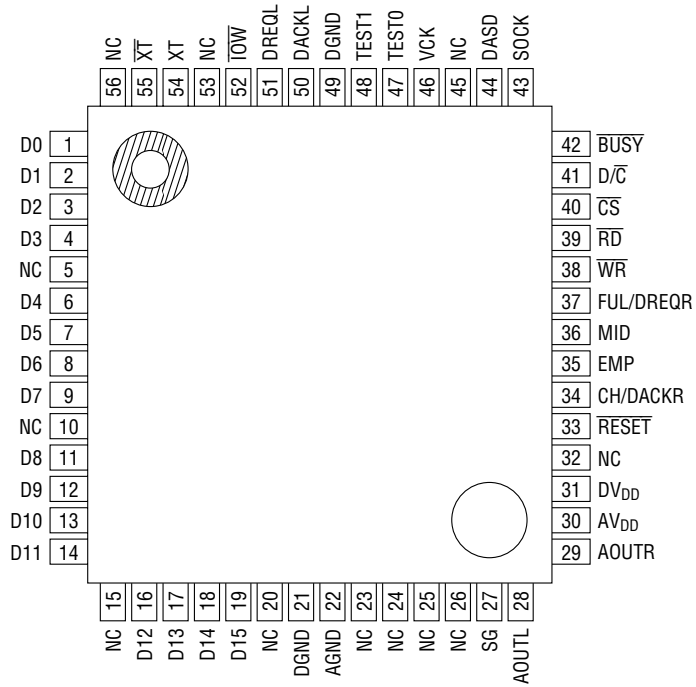
FEATURES

- 16/8-bit bus interface support
- FIFO capacity: User-definable (256/512/1024 bits)
(buffering time of 32 ms when using 8 kHz sampling frequency, 4-bit ADPCM2/ADPCM, and in monaural playback)
- Four voice analysis and synthesis systems:
4, 5, 6, 7, 8-bit ADPCM2; 4-bit ADPCM; 8, 16-bit PCM; and 8-bit Nonlinear PCM
- Source oscillation frequency: 4.096 MHz
- Sampling frequency: 4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz
- Volume control (8 steps: 0 dB to 21 dB)
- Built-in 14-bit D/A converter
- Built-in LPF: Attenuation factor -40 dBm/oct
- Package options:
56-pin plastic QFP (QFP56-P-910-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connection

56-pin plastic QFP

Note: This configuration may be changed.

PIN DESCRIPTIONS

| Symbol | Type | Description |
|-------------------|------|--|
| D15-D8 | I/O | For 8-bit bus interface, the command allows these pins to be configured to be inputs or outputs to input or output data to and from an external memory. Otherwise, these pins are configured to be outputs only. For a 16-bit interface, these pins are bidirectional data to and from an external microcontroller and memory. |
| D7-D0 | I/O | Birirectional data bus to input/output data and output status with an external microcontroller and memory. |
| \overline{WR} | I | Write pulse input pin. This pin pulse "L" when command or voice data is input to the D15-D0 pins. |
| \overline{RD} | I | Read pulse input pin. This pin pulse "L" when status is output to the D15-D0 pins. |
| \overline{CS} | I | Accepts write pulse and read pulse when this pin is "L". Does not accept write pulse and read pulse when this pin is "H". |
| D/\overline{C} | I | Inputs voice data from D15-D0 pins when this pin is "H". Inputs/outputs command and status from D7-D0 pins when this pin is "L". |
| \overline{BUSY} | O | This pin outputs an "L" level during recording, PLAYBACK or PAULSE. |
| EMP | O | "H" level indicates that there is no data in FIFO memory. Active "H" can be changed to active "L" by command input. |
| MID | O | "H" level indicates that more than half of the memory space is filled with data. Voice synthesis starts when MID changes to "H" level. Active "H" can be changed to active "L" by command input. |
| FUL/DREQR | O | "H" level indicates that FIFO memory is full of data. During playback, this pin is "H" and data cannot be written in FIFO memory. Active "H" can be changed to active "L" by command input. DREQR is selected when DMA transfer and stereo playback are chosen by command input. In this case, DREQR is a DMA transfer request signal for right voice data. When left FIFO memory capacity is empty (EMP state), DREQR goes to "H" level. Active "H" can be changed to active "L" by command input. |
| CH/DACKR | I | When stereo playback is selected and CH is "H", voice data is written in right FIFO memory, and the EMP, MID or FUL pin outputs the status of left FIFO memory. When CH is "L", data is written in left FIFO memory, and the EMP, MID or FUL pin outputs the status of left FIFO memory. When DMA transfer and stereo playback are selected, DACKR is selected. In this case, DACKR outputs a DMA transfer acknowledge signal. When DACKR is "H", the \overline{TOW} signal is accepted. Active "H" can be changed to active "L" by command input. |
| DREQL | O | When FIFO memory capacity is empty (EMP state), DREQL goes "H" and outputs a DMA transfer request signal. When stereo playback is selected, DREQL goes "H" and outputs a DMA transfer request signal. Active "H" can be changed to active "L" by command input. |
| DACKL | I | DMA transfer acknowledge signal. When DACKL is "H", the \overline{TOW} signal is accepted. When stereo playback is selected, DACKL is a DMA transfer acknowledge signal for left FIFO memory. Active "H" can be changed to active "L" by command input. If DMA transfer is not used, set this pin to "L" level. |
| \overline{TOW} | I | Signal to write external memory data to MSM9842 during DMA transfer. If DMA transfer is not used, set this pin to "L" level. |

PIN DESCRIPTIONS

| Symbol | Type | Description |
|--------------------|------|---|
| DASD | 0 | 16-bit serial data output pin when external DAC is used. |
| SIOCK | 0 | Synchronizing clock for 16-bit serial data input/output when external DAC is used. |
| XT | 1 | Oscillator connection pins. When external clock is used, input clock into XT pin and leave \overline{XT} pin open. |
| \overline{XT} | 0 | |
| VCK | 0 | Outputs sampling frequency selected at playback. This sampling frequency is used as a synchronizing signal when external DAC is used. |
| \overline{RESET} | 1 | When this pin is "L", the device is initialized. |
| TEST0 TEST1 | 1 | Pins for testing. Set the pins to "L". |
| SG | 0 | Analog circuit signal ground output pin. |
| AOUTL | 0 | Left side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers. |
| AOUTR | 0 | Right side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers. |
| DV _{DD} | — | Digital power supply pin. Insert a minimum 0.1 μ F bypass capacitor between this pin and DGND pin. |
| DGND | — | Digital GND pin. |
| AV _{DD} | — | Analog power supply pin. Insert a minimum 0.1 μ F bypass capacitor between this pin and AGND pin. |
| AGND | — | Analog GND pin. |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------|-----------|--------------------------|----------------------|--------------------|
| Power Supply Voltage | V_{DD} | $T_a=25^{\circ}\text{C}$ | -0.3 to +7.0 | V |
| Input Voltage | V_{IN} | $T_a=25^{\circ}\text{C}$ | -0.3 to $V_{DD}+3.0$ | V |
| Storage Temperature | T_{STG} | — | -55 to +155 | $^{\circ}\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit |
|------------------------|-----------|--------------|------------|--------------------|
| Power Supply Voltage | V_{DD} | DGND=AGND=0V | 4.5 to 5.5 | V |
| Operating Temperature | T_{OP} | — | -40 to +85 | $^{\circ}\text{C}$ |
| Master Clock Frequency | f_{OSC} | — | 4.096 | MHz |

ELECTRICAL CHARACTERISTICS**DC Characteristics**
 $DV_{DD}=AV_{DD}=4.5 \text{ to } 5.5\text{V}, DGND=AGND=0\text{V}, T_a=-40 \text{ to } +85^{\circ}\text{C}$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------|-----------|--|----------------------|------|---------------------|---------------|
| High-level Input Voltage | V_{IH} | — | $V_{DD} \times 0.85$ | — | — | V |
| Low-level Input Voltage | V_{IL} | — | — | — | $V_{DD} \times 0.2$ | V |
| High-level output Voltage | V_{OH} | $I_{OH}=-40 \mu\text{A}$ | $V_{DD}-0.3$ | — | — | V |
| Low-level output Voltage | V_{OL} | $I_{OL}=2 \mu\text{A}$ | — | — | 0.45 | V |
| High-level Input Current (*1) | I_{IH1} | $V_{IH}=V_{DD}$ | — | — | 10 | V |
| Low-level Input Current (*2) | I_{IH2} | $V_{IH}=V_{DD}$ | — | — | 20 | μA |
| Low-level Input Current (*3) | I_{IL1} | $V_{IL}=DGND$ | -10 | — | — | μA |
| Low-level Input Current (*2) | I_{IL2} | $V_{IL}=DGND$ | -20 | — | — | μA |
| Low-level Input Current (*4) | I_{IL3} | $V_{IL}=DGND$ | -400 | — | -20 | μA |
| Operating Current | I_{DD} | $f_{OSC}=4.096 \text{ MHz}$, without load | — | 7 | 15 | mA |
| Standby Current | I_{DDs} | At power down, without load $T_a=-40 \text{ to } +70^{\circ}\text{C}$ | — | — | 10 | μA |
| | | At power down, without load $T_a=-40 \text{ to } +85^{\circ}\text{C}$ | — | — | 50 | μA |

*1 Applicable to input excluding XT pin.

*2 Applicable to XT pin.

*3 Applicable to input pins without a pull-up resistor excluding XT pin.

*4 Applicable to input pins with a pull-up resistor excluding XT pin.

Analog Characteristics

 $DV_{DD}=AV_{DD}=4.5 \text{ to } 5.5\text{V}$, $DGND=AGND=0\text{V}$, $T_a=-40 \text{ to } +85^\circ\text{C}$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|-------------|-----------|------|------|------|------------|
| D/A Output Relative Error | $ V_{DAE} $ | No load | — | — | 10 | mV |
| AOUT L/R Output Load Resistance | R_{AOUT} | — | 50 | — | — | k Ω |

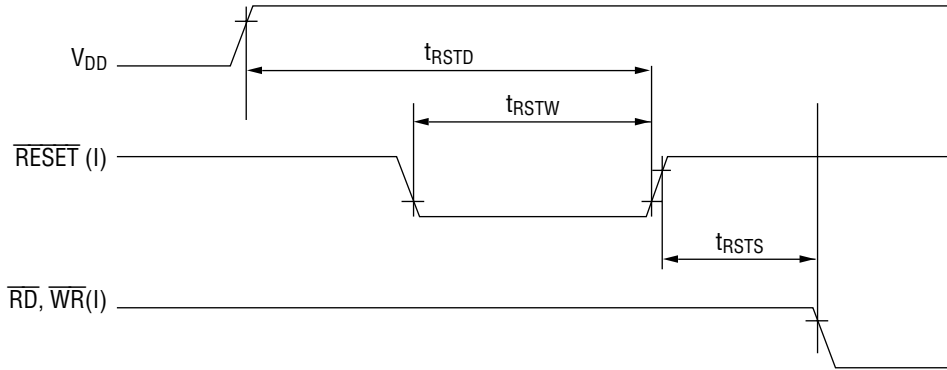
AC Characteristics

 $DV_{DD}=AV_{DD}=4.5 \text{ to } 5.5\text{V}$, $DGND=AGND=0\text{V}$, $T_a=-40 \text{ to } +85^\circ\text{C}$

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|------------|------|------|------|------|
| RESET Pulse Width | t_{RSTW} | 300 | — | — | ns |
| Setup Time after Rise of Power Supply for Fall of RESET | t_{RSTD} | 500 | — | — | ns |
| Time to Active First RD, WR after Fall of RESET | t_{RSTS} | 200 | — | — | ns |
| RD Pulse Width | t_{RR} | 160 | — | — | ns |
| CS, D/C, CH Setup and Hold Time for RD | t_{CR} | 30 | — | — | ns |
| Time from Fall of RD till Data Status Definition | t_{DRE} | — | — | 160 | ns |
| Time from Fall of RD till Data Float | t_{DRF} | — | 10 | 50 | ns |
| Time from Rise of RD till Fall of Next RD | t_{CRC} | 500 | — | — | ns |
| WR Pulse Width | t_{WW} | 160 | — | — | ns |
| CS, D/C, CH Setup and Hold Time for WR | t_{CW} | 30 | — | — | ns |
| Setup Time of Data, Command for Rise of WR | t_{DWS} | 160 | — | — | ns |
| Hold Time of Data, Command for Rise of WR | t_{DWH} | 10 | — | — | ns |
| Time from Rise of WR till Fall of Next WR | t_{CWC} | 500 | — | — | ns |
| IOW Pulse Width | t_{IOWW} | 160 | — | — | ns |
| Setup and Hold Time of DACKL/R for IOW | t_{DW} | 10 | — | — | ns |
| Setup Time of Data for Rise of IOW | t_{IOWE} | — | — | 160 | ns |
| Hold Time of Data for Rise of IOW | t_{IOWF} | — | 10 | 50 | ns |
| Time from Rise of IOW till Fall of Next IOW | t_{IOWC} | 200 | — | — | ns |

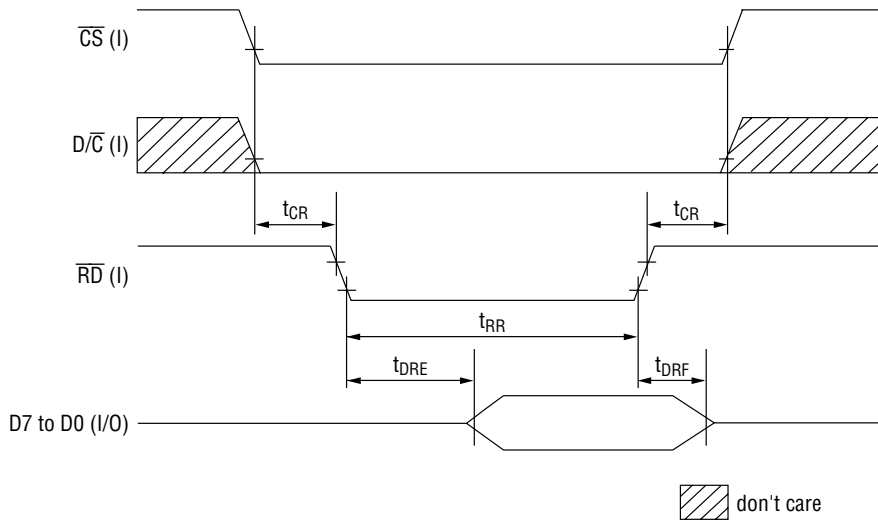
TIMING DIAGRAMS

Reset Timing

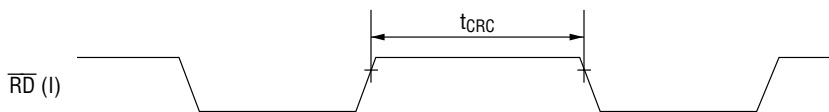


Read Timing

1. Status Read Timing

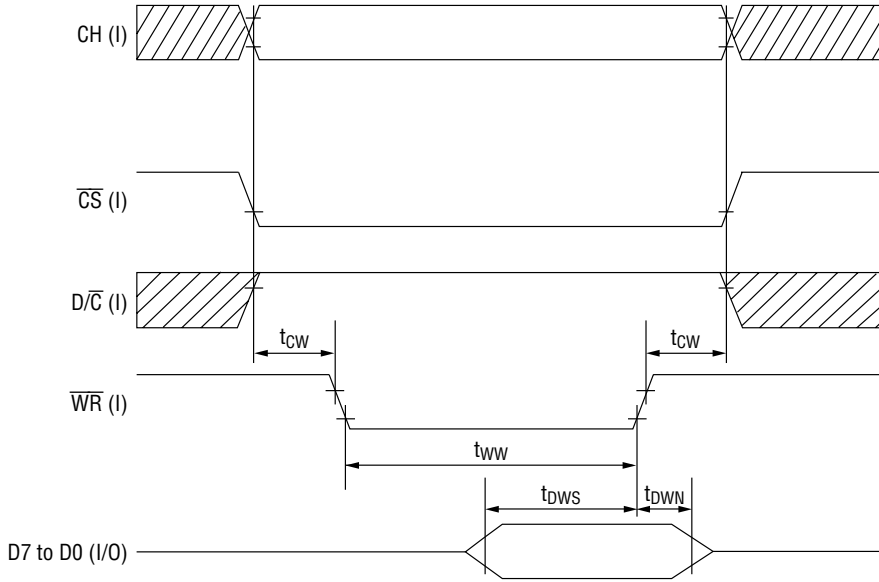


2. Read Cycle Timing

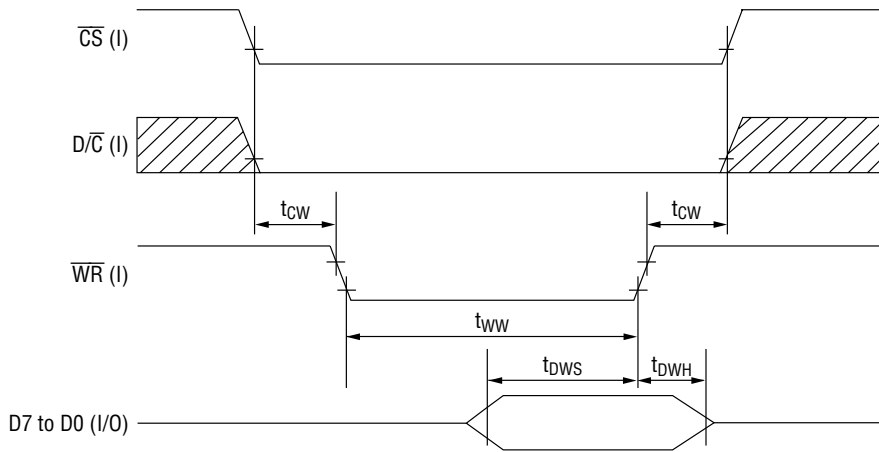


Write Timing

1. Data Write Timing

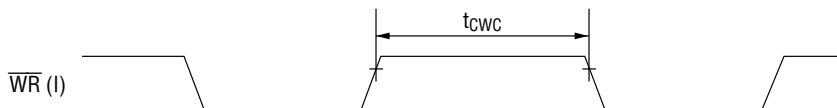


2. Command Write Timing



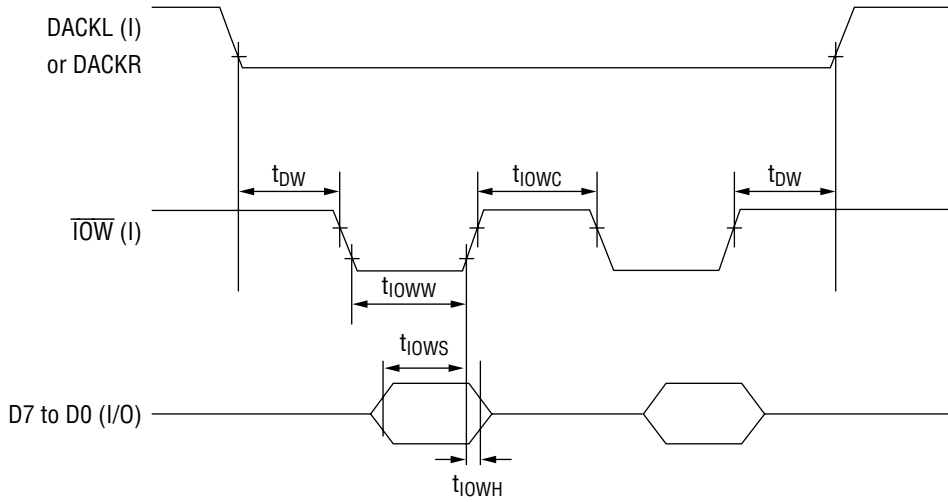
 don't care

3. Write Cycle Timing



DMA Transfer Timing

1. \overline{IOW} (during playback and 2-byte writing)



FUNCTIONAL DESCRIPTION

Voice synthesis method

The MSM9842 supports four PCM methods to process various kinds of voices :4-bit ADPCM; 4-, 5-, 6-, 7-, or 8-bit ADPCM2; 8- or 16-bit straight PCM; and 8-bit non-linear PCM.

1. 4-bit ADPCM method (Adaptive Differential Pulse Code Modulation).
This method encodes 4-bit data while adaptively varying the basic quantization width "Δ" at each sampling. This method reduces storage requirements by storing differences between successive digital samples rather than full values. This method very effectively processes human and animal voices and natural sounds, reducing voice data storage space. This method offers high sound reproduction quality.
2. 4-, 5-, 6-, 7-, or 8-bit ADPCM2 method
This method has higher sound reproduction quality than the ADPCM method. The ADOCM2 method offers compression methods (4-, 5-, 6-, 7-, or 8-bit) Note that data used in the 4-bit ADPCM method is not compatible with data in the 4-bit ADPCM2 method. Data conversion for these methods can be made by a development tool.
3. 8- or 16-bit straight PCM method
This method has the highest sound reproduction characteristics in all frequencies (of the above four PCM methods). This method is suitable for sound effects having high frequencies and sounds having pulse-like waveforms.
4. 8-bit non-linear PCM method
The method emphasizes the value of the center of each sound wave and processes it with 10 bit perceived accuracy. It is effective in improving the tone quality of low frequency voices and sounds.

Data configuration when 8-bit bus is used

1. 4-bit ADPCM method and 4-bit ADPCM2 method

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|------|------|------|------|------|------|
| MSB1 | 3SB1 | 2SB1 | LSB1 | MSB2 | 3SB2 | 2SB2 | LSB2 |

2. 5-bit ADPCM2 method

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|------|------|------|------|------|
| × | × | × | MSB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |

3. 6-bit ADPCM2 method

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|------|------|------|------|------|------|
| × | × | MSB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |

4. 7-bit ADPCM method and 4-bit ADPCM2 method

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|------|------|------|------|------|
| × | MSB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|------|------|------|------|------|------|
| MSB1 | 7SB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |

× : don't care

6. 16-bit Straight-PCM

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------|-------|-------|-------|-------|-------|-------|------|--------------|
| MSB1 | 15SB1 | 14SB1 | 13SB1 | 12SB1 | 11SB1 | 10SB1 | 9SB1 | 1st transfer |
| 8SB1 | 7SB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 | 2nd transfer |

Data configuration when 16-bit bus is used

1. 4-bit ADPCM method and 4-bit ADPCM2 method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|------|------|
| MSB1 | 3SB1 | 2SB1 | LSB1 | MSB2 | 3SB2 | 2SB2 | LSB2 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MSB3 | 3SB3 | 2SB3 | LSB3 | MSB4 | 3SB4 | 2SB4 | LSB4 |

2. 5-bit ADPCM2 method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|------|------|------|------|------|
| × | × | × | MSB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| × | × | × | MSB2 | 4SB2 | 3SB2 | 2SB2 | LSB2 |

3. 6-bit ADPCM2 method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|------|------|------|------|------|------|
| × | × | MSB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| × | × | MSB2 | 5SB2 | 4SB2 | 3SB2 | 2SB2 | LSB2 |

4. 7-bit ADPCM method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|------|------|------|------|------|------|------|
| × | MSB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| × | MSB2 | 6SB1 | 5SB1 | 4SB2 | 3SB2 | 2SB2 | LSB2 |

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|------|------|
| MSB1 | 7SB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MSB2 | 7SB2 | 6SB1 | 5SB1 | 4SB2 | 3SB2 | 2SB2 | LSB2 |

6. 16-bit straight PCM method

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|-------|-------|-------|-------|-------|-------|------|
| MSB1 | 15SB1 | 14SB1 | 13SB1 | 12SB1 | 11SB1 | 10SB1 | 9SB1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 8SB2 | 7SB1 | 6SB1 | 5SB1 | 4SB1 | 3SB1 | 2SB1 | LSB1 |

× : don't care

FIFO memory configuration

The configuration of FIFO memory can be changed with a command controlling on the D7 to D0 pins. Initially, the FIFO memory is 512 bits (64 words by 8 bits).

Outline of FIFO memory

- (1) The FIFO memory space has two FIFO paths (FIFOL and FIFOH) to enable asynchronous read and write operations in different cycles (see Figure 1). When FIFOL is used for a write operation, FIFOH is used for read operation. When FIFOL is full with data and writing in FIFOL is ready to be read.
- (2) The FIFO memory has two address pointers : a read address pointer that points to an address where data read has been completed and a write address pointer that points to an address where data write has been completed. When these two address pointers match, recording or playback ends.
- (3) Initially, these two pointers point to an identical address. (FUL="L,"MID="L," and EMP="H")

FIFO memory configuration when an 8-bit bus and monophonic reproduction are selected

The following three FIFO memory sizes are selectable by commands :

- 1024 bits (128 words by 8 bits)
- 512 bits (64 words by 8 bits)
- 256 bits (32 words by 8 bits)

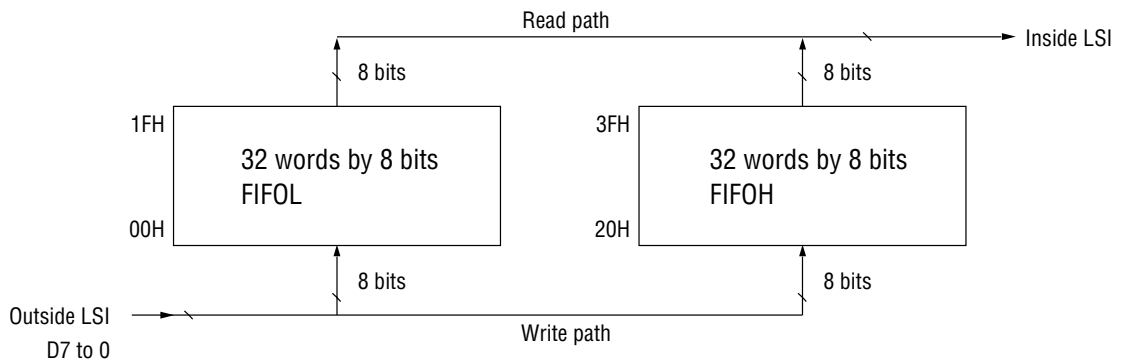


Figure 1 FIFO memory configuration when 64 words by 8 bits (512 bits) are selected.

FIFO memory configuration when a 16-bit bus and at monophonic reproduction are selected
 The following three FIFO memory sizes are selectable by commands :

- 1024 bits (64 words by 16 bits)
- 512 bits (32 words by 16 bits)
- 256 bits (16 words by 16 bits)

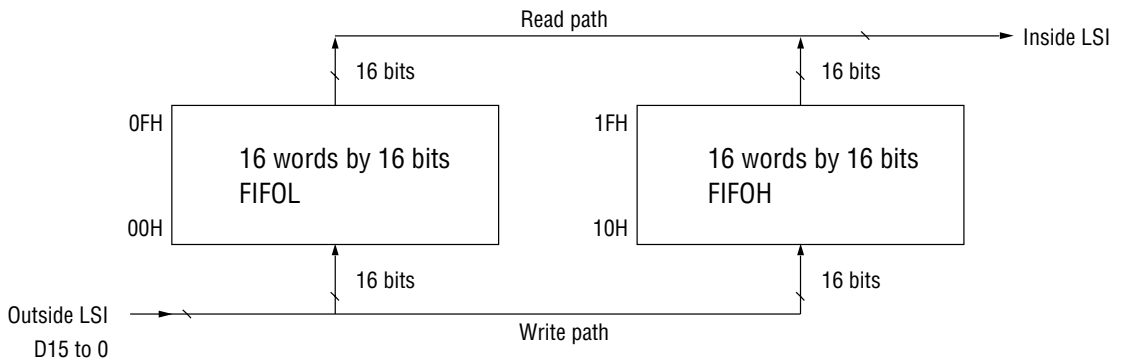


Figure 2 FIFO memory configuration when 512 bits (32 words by 16 bits) are selected.

FIFO memory configuration when an 8-bit bus and at stereophonic reproduction are selected
 The following three FIFO memory sizes are selectable by commands :

- 1024 bits (64 words by 8 bits) × 2
- 512 bits (32 words by 8 bits) × 2

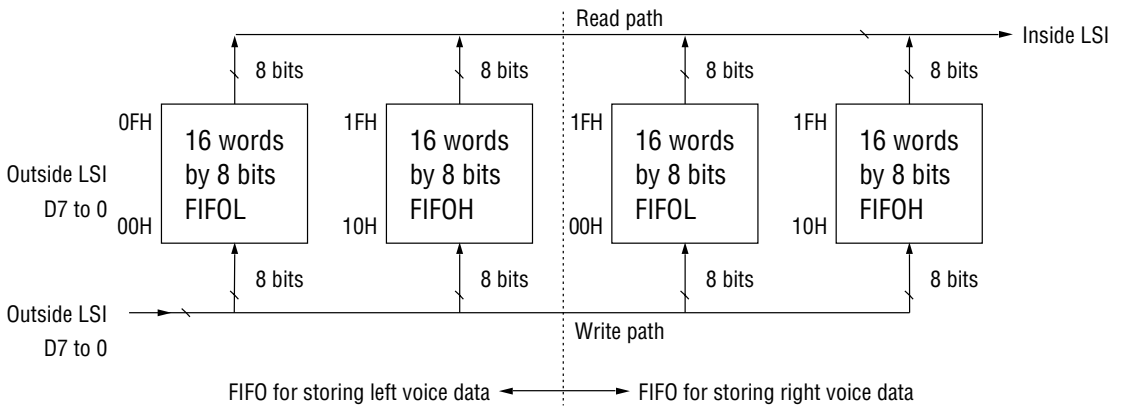


Figure 3 FIFO memory configuration when 512 bits (32 words by 8 bits) × 2 are selected.

FIFO memory configuration when 16-bit bus and at stereophonic reproduction are selected
 The following three FIFO memory sizes are selectable by commands :

- 1024 bits (32 words by 16 bits) × 2
- 512 bits (16 words by 16 bits) × 2

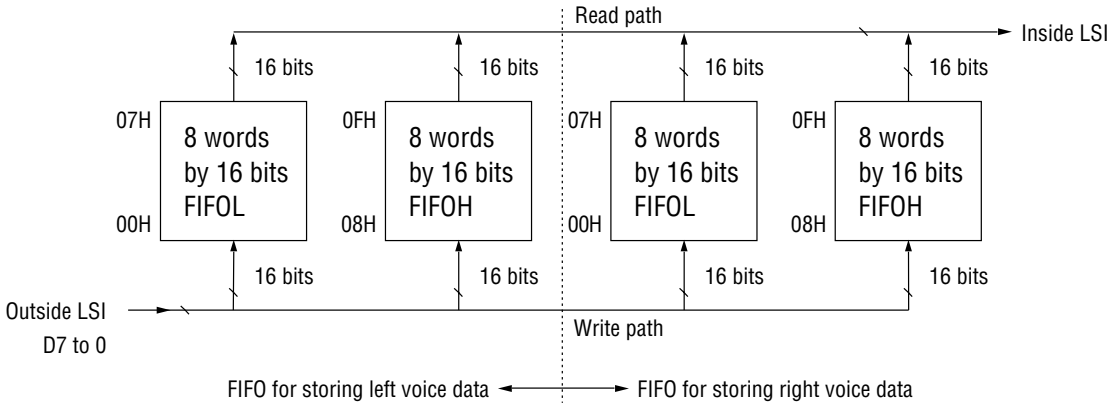


Figure 4 FIFO memory configuration when 512 bits (16 words by 16 bits) × 2 are selected.

Voice synthesis methods and maximum buffering times

FIFO capacity of 1024 bits and sampling frequency of 8kHz

- | | | | |
|-----|--------------------------------|--------------|----------------|
| (1) | 8-bit bus selected | (Monophonic) | (Stereophonic) |
| | 4-bit ADPCM2 or ADPCM : | 32ms | 16ms |
| | 5-, 6-, 7-, and 8-bit ADPCM2 : | 16ms | 8ms |
| | 8-bit PCM : | 16ms | 8ms |
| (2) | 16-bit bus selected | (Monophonic) | (Stereophonic) |
| | 16-bit PCM : | 16ms | 8ms |

The other methods are the same as those when the 8-bit bus is used.

Playback operation (8-bit bus, 512-bit FIFO configuration)

- (1) Voice synthesis sampling frequency, bus length, and stereophonic playback mode can be set by commands.
- (2) When a Playback Start command is entered or when data of 1 word by 8 bits is written in FIFOL, the MSM9842 recognizes the start of playback and starts synthesizing voices when the MID pin goes high ("H").
- (3) Status indication by EMP, MID, and FUL pins (64 words memory configuration)
 - EMP="H", MID="L", FUL="L"
No data is written in FIFO memory.
 - EMP="L", MID="L", FUL="L"
Data of 1 word to 31 words has been written in FIFO memory. In this state, the voice synthesizer cannot read data from FIFO memory.
 - EMP="L", MID="H", FUL="L"
Data of 32 words to 63 words has been written in FIFO memory. While the MID pin is "H," the voice synthesizer can read data from FIFO memory. If writing of 32 words into FIFOL is not completed when the voice synthesizer has completed reading 32 words from FIFOL, the MID pin goes low.
 - EMP="L," MID="H," FUL="H"
Data of 64 words is written in FIFO memory
In this state, writing of 32 words into FIFOL is completed before the voice synthesizer reads 32 words from FIFOL and no data can be written in FIFO memory.
- (4) End of playback
If data writing is not completed in a FIFO block (FIFOL or FIFOH) within a preset time period while the EMP, MID, and FUL pins are all low, the MSM9841 assumes that a write cycle has ended, moves the read address pointer to a FIFO block (FIFOL or FIFOH) having the write address pointer, and starts a read cycle. When both the read and write address pointers are in the same FIFO block (FIFOL or FIFOH), the FUL pin goes high (the EMP and MID pins remain low). When the read and write address pointers point to the same address, the EMP pin goes high and the MID pin goes low (the MID pin remains low). In this state, playback ends.

Pausing when playback is in progress

- (1) The playback operation can be paused by a command. At the same time, a write-operation on FIFO memory can be stopped during the pause. When the playback operation restarts, the read or write operation on FIFO memory is un-paused. It is also possible to continue the read or write operation on FIFO memory according to the previous pin status (EMP, MID, and FUL pins).

Intermediate stopping during playback

- (1) Playback can be stopped by a command any time. In this case, FIFO memory is cleared to the initial status.

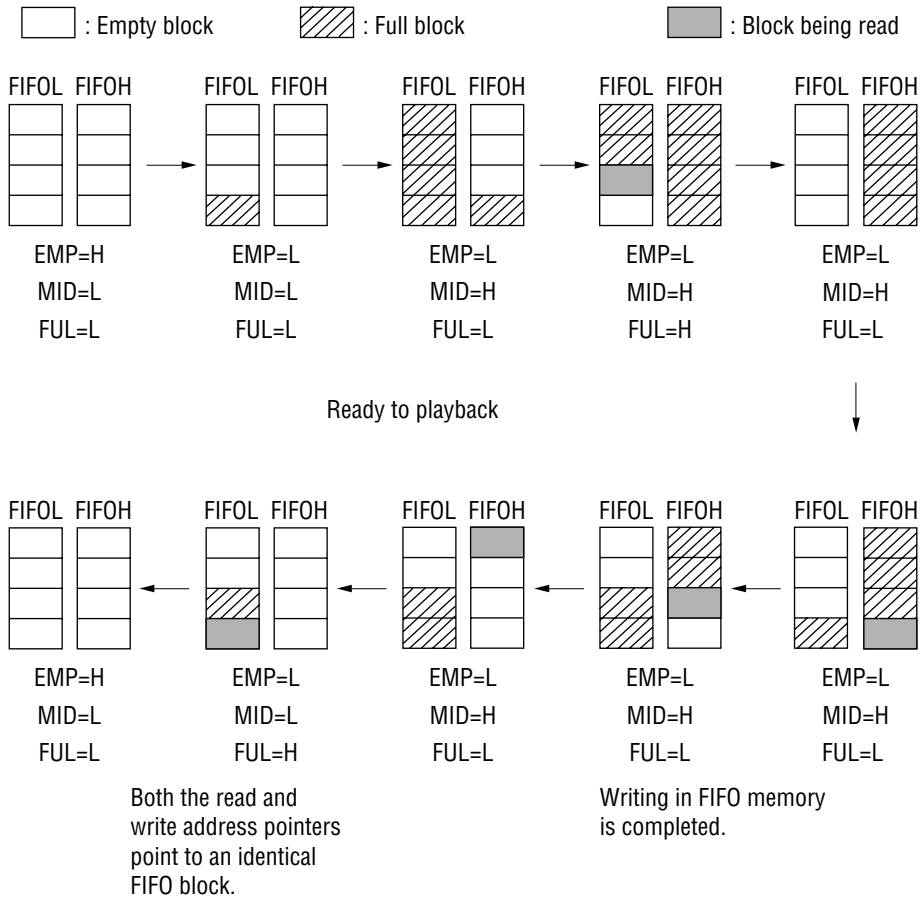
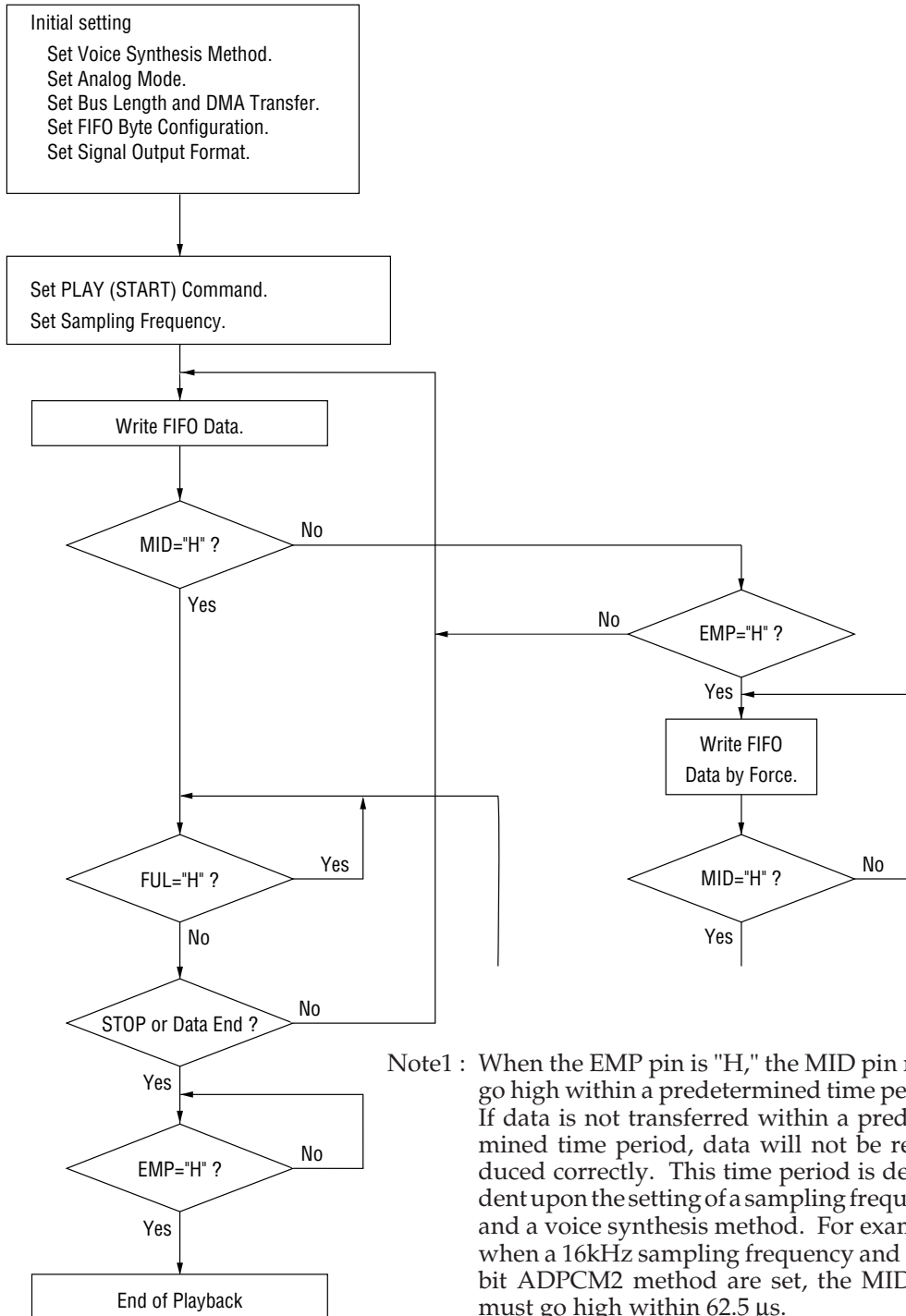


Figure 5 FIFO Memory Status Transition

Playback Data Transfer Flowchart (without DMA transfer)



Note1 : When the EMP pin is "H," the MID pin must go high within a predetermined time period. If data is not transferred within a predetermined time period, data will not be reproduced correctly. This time period is dependent upon the setting of a sampling frequency and a voice synthesis method. For example, when a 16kHz sampling frequency and an 8-bit ADPCM2 method are set, the MID pin must go high within 62.5 μs.

Note2 : When a stop command is entered or when data writing ends, the last data is transferred to the LSI and the EMP pin goes high. With this, all data transfer is completed.

DMA Control Method

The MSM9842 sends a DMA Transfer request to the DMA controller and waits for a DMA transfer permission from the DMA controller. Upon reception of the permission, the MSM9842 starts data transfer at a transfer cycle of the DMA controller. The DMA Transfer function is enabled or disabled by commands.

DREQL and DREQR pins (8-bit bus, 512-bit FIFO configuration)

These pins are used to send a DMA Transfer request to the DMA controller. The amount of DMA transfer data is 32 words or 64 words, selected by commands.

1. In case FIFO memory performs read and write operations simultaneously (DMA transfer data of 64 words) :
 - (1) When the PLAY (START) command is entered, the DREQL or DREQR pin goes high to request a cycle to write data into FIFO memory. After playback status, the DREQL/R pin remains high until the 64-word write cycle is completed. When a 32-word write cycle is completed, voice synthesis starts. From now on, each time the amount of data in FIFO memory becomes half, the DREQL/R pin goes high to send a request to DMA transfer 32 words.
2. In case the FIFO memory performs read and write operations alternately (DMA transfer data of 64 words) :
 - (1) When the PLAY (START) command is entered, the DREQL or DREQR pin goes high to request a cycle to write data into FIFO memory. After playback starts, the DREQL/R pin remains high until the 64-word write cycle is completed. When a 32-word write cycle is completed, voice synthesis starts. From now on, each time FIFO memory becomes empty, the DREQL/R pin goes high to send a request to DMA-transfer of 32 words.
 - (2) Data of 64 words must be transferred within a predetermined time period (e. g. a time period before the voice synthesizer reads the next data immediately after FIFO memory becomes empty). Data of 64 words must be written in FIFO memory within this time period.

Example : 62.5 μ s when 16kHz (sampling frequency) and the 8-bit PCM method are selected.

DACKL and DACKR

These pins recognize a DMA Transfer acknowledge signal from the DMA controller.

When the DACKL/DACKR pin is at a high level ("H"), the $\overline{\text{IOR}}$ pin is enabled.

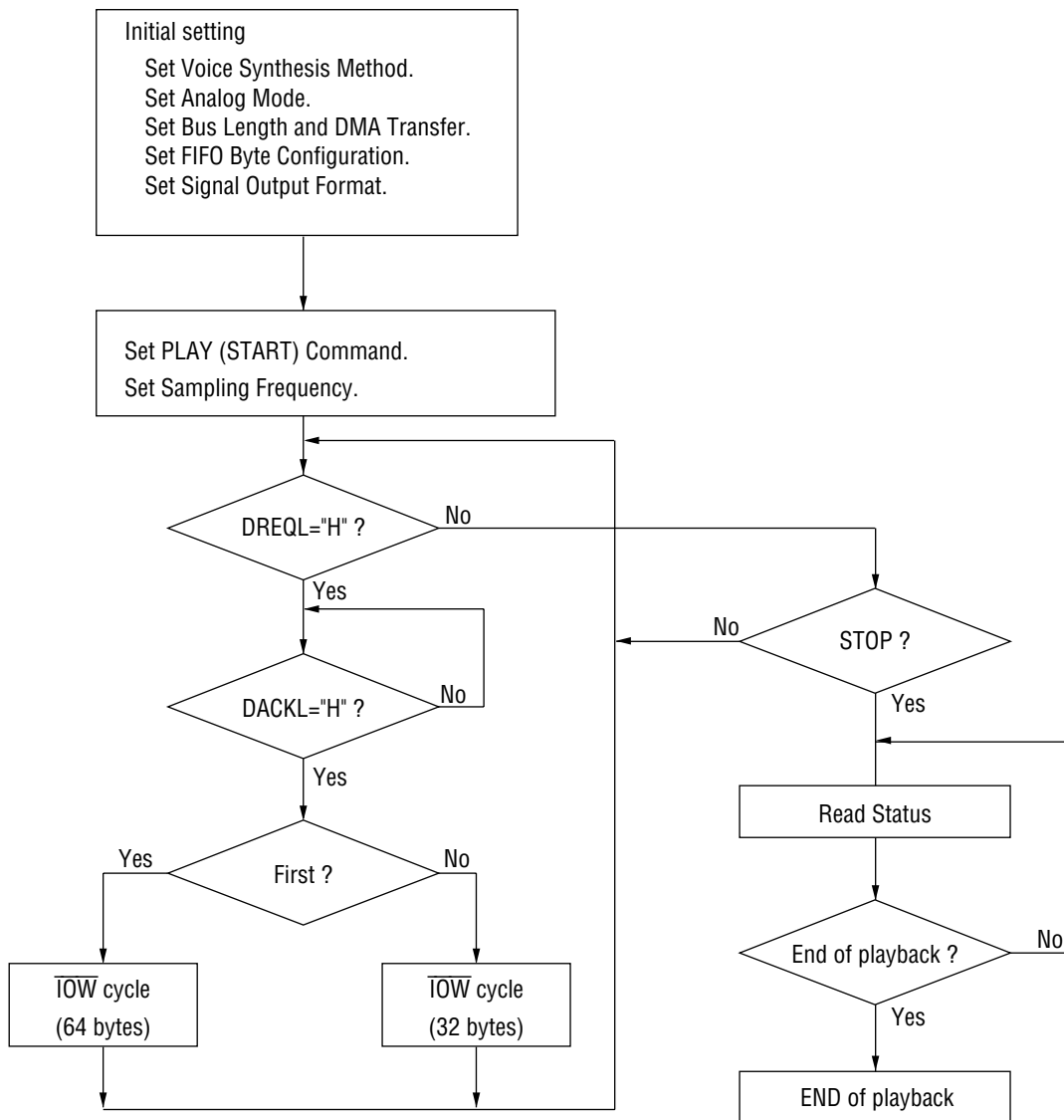
When the DACKL/DACKR pin is at a high level ("H"), control by the $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and $\text{D}/\overline{\text{C}}$ pins is disabled. Therefore, all settings on the MSM9842 must be completed before the DMA transfer cycle starts.

$\overline{\text{IOW}}$

The $\overline{\text{IOW}}$ pin is enabled when the DACKL or DACKR pin goes high and its state is controlled by the DMA controller.

The $\overline{\text{IOW}}$ pin is an input pin to transfer data from external memory to the MSM9842.

Playback Data Transfer Flowchart (with DMA transfer)



Note 1 : The above flowchart assumes that the size of FIFO memory is 64 bytes. The MSM9842 writes 64 bytes (block by block) in the first write operation and writes 32 bytes (block by block) in the second and later read operations. A time period between the input of a DREQ request and the method. When an 8kHz sampling frequency and an 8-bit ADPCM2 method are set, 32-byte block writing must be completed within 2ms.

Note 2 : After the STOP command is entered, all data that currently remains in FIFO memory is transferred to the LSI and voice synthesis is completed. The end of playback is recognized by the status read signal or the BUSY signal.

Using an External DAC

Select the External DAC mode and TOC or BIN by commands. The MSM9842 interfaces to the external DAC through the DASD, SIOCK, and VCK pins. In monophonic playback, the MSM9842 outputs data when the VCK pin is at a high level ("H"). In stereophonic playback, the MSM9842 outputs left data when the VCK pin is at a high level ("H") and right data when the VCK pin is at a low level ("L"). Figure 6 shows stereophonic playback timing of the external DAC at a sampling frequency of 32 kHz (maximum).

Data is valid in back justification. Left voice data is valid if it is entered before the VCK signal falls. Right voice data is valid if it is entered before the VCK signal rises.

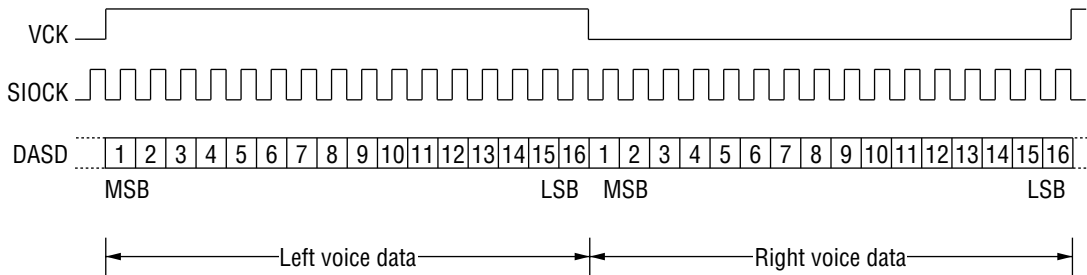


Figure 6 Stereophonic playback timing of the external DAC at VCK=32 kHz

COMMAND LIST

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|----|----|----|----|----|----|----|----|---------------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No function |
| 0 | 0 | 0 | 1 | × | S2 | S1 | S0 | No function |
| 0 | 0 | 1 | 0 | H3 | S2 | S1 | S0 | PLAY START |
| 0 | 0 | 1 | 1 | C3 | C2 | × | × | STOP |
| 0 | 1 | 0 | 0 | H3 | C2 | C1 | × | PAUSE |
| 0 | 1 | 0 | 1 | C3 | V2 | V1 | V0 | VOICE CONTROL |
| 0 | 1 | 1 | 0 | W3 | W2 | × | × | POWER-DOWN MODE |
| 0 | 1 | 1 | 1 | P3 | P2 | P1 | P0 | VOICE SYNTHESIS METHOD |
| 1 | 0 | 0 | 0 | R3 | R2 | R1 | R0 | Analog specification 1 |
| 1 | 0 | 0 | 1 | × | × | E1 | E0 | Analog opecification 2 and bus length |
| 1 | 0 | 1 | 0 | × | B2 | B1 | B0 | FIFO memory configuration |
| 1 | 0 | 1 | 1 | F3 | D2 | D1 | D0 | Signal output format |
| 1 | 1 | 0 | 0 | G2 | G1 | G0 | × | DMA Transfer |
| 1 | 1 | 0 | 1 | T3 | T2 | T1 | T0 | Test Command |

×=don't care

Voice synthesis method

| P3 | P2 | P1 | P0 | Function |
|----|----|----|----|------------------------|
| 0 | 0 | 0 | 0 | 4bitOKIADPCM2 * |
| 0 | 0 | 0 | 1 | 5bitOKIADPCM2 |
| 0 | 0 | 1 | 0 | 6bitOKIADPCM2 |
| 0 | 0 | 1 | 1 | 7bitOKIADPCM2 |
| 0 | 1 | 0 | 0 | 8bitOKIADPCM2 |
| 0 | 1 | 0 | 1 | 4bitOKIADPCM |
| 0 | 1 | 1 | 0 | 8bitPCM |
| 0 | 1 | 1 | 1 | 8bitOKI non-linear PCM |
| 1 | 0 | 0 | 0 | 16bitPCM |

Volume Setting

| V2 | V1 | V0 | dB |
|----|----|----|-------|
| 0 | 0 | 0 | 0dB * |
| 0 | 0 | 1 | -3dB |
| 0 | 1 | 0 | -6dB |
| 0 | 1 | 1 | -9dB |
| 1 | 0 | 0 | -12dB |
| 1 | 0 | 1 | -15dB |
| 1 | 1 | 0 | -18dB |
| 1 | 1 | 1 | -21dB |

Sampling frequency

| S2 | S1 | S0 | Frequency |
|----|----|----|-----------|
| 0 | 0 | 0 | 8.0 kHz * |
| 0 | 0 | 1 | 12.8 kHz |
| 0 | 1 | 0 | 16.0 kHz |
| 0 | 1 | 1 | 32.0 kHz |
| 1 | 0 | 0 | 6.4 kHz |
| 1 | 0 | 1 | 4.0 kHz |

Voice Output Setting

| C3 | C2 | Function |
|----|----|-------------------------------------|
| 0 | 0 | Left voice |
| 1 | 0 | Right voice |
| × | 1 | Common to both left and right sides |

Voice Output Setting

| H3 | Function |
|----|-------------|
| 0 | Left voice |
| 1 | Right voice |

Pause Setting

| C1 | Function |
|----|-----------------|
| 0 | Starts pausing |
| 1 | Cancels pausing |

FIFO memory configuration

| B1 | B0 | Function |
|----|----|---------------|
| 0 | 0 | 512 bits |
| 0 | 1 | 1024 bits |
| 1 | 0 | 256 bits |
| 1 | 1 | FIFO not used |

Note : Do not use in the stereophonic playback mode

| B2 | Function |
|----|---|
| 0 | Read or Write operation to FIFO for MID="H" |
| 1 | Read or Write operation to FIFO for FUL="H" |

Analog specification 1

| R3 | Function |
|----|--------------------------|
| 0 | Display 2's complements. |
| 1 | Display in binary. |
| R2 | Function |
| 0 | Use internal DAC. |
| 1 | Use external DAC. |
| R0 | Function |
| 0 | Monophonic playback |
| 1 | Stereophonic playback |

Power-down

| W3 | Function |
|----|---------------------------------|
| 0 | Cancel power-down. |
| 1 | Start power-down. |
| W2 | Function |
| 0 | Retain LSI internal setting. |
| 1 | Initialize LSI internal setting |

Analog specification 2 and data bus transfer setting

| A3 | Function |
|----|----------------------------------|
| 0 | With output amplifier |
| 1 | Without output amplifier |
| A2 | Function |
| 0 | With LPF |
| 1 | Without LPF |
| E1 | Function |
| 0 | 8-bit bus length |
| 1 | 16-bit bus length |
| E0 | Function |
| 0 | D15 to D8 not used for 8-bit bus |
| 1 | D15 to D8 used for 8-bit bus |

Signal output format

| F3 | Function |
|----|---|
| 0 | EMP, MID, and FUL outputs : Active high |
| 1 | EMP, MID, and FUL outputs : Active low |
| D2 | Function |
| 0 | DREQL and DREQR outputs : Active high |
| 1 | DREQL and DREQR outputs : Active low |
| D1 | Function |
| 0 | DACKL and DACKR outputs : Active high |
| 1 | DACKL and DACKR outputs : Active low |
| D0 | Function |
| 0 | No function |
| 1 | For testing. Don't use |

*Default

DMA transfer setting

| G2 | G3 | G1 | Function |
|----|----|----|----------------------|
| 0 | × | × | Without DMA transfer |
| 1 | 0 | 0 | Signal mode transfer |
| 1 | 0 | 1 | Block mode transfer |

Description of commands

1. NOP command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | × | × | × | × |

No function

2. PLAYBACK command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 1 | 0 | H3 | S2 | S1 | S0 |

This command starts playback. Bits D2 to D0 specify a sampling frequency. Bit D3 selects left or right voice data to be played back. For stereophonic playback, left and right sampling frequencies must be the same.

| H3 | Function |
|----|--|
| 0 | Playback of left voice. (Initial value) |
| 1 | Playback of right voice. (Initial value) |

| S2 | S1 | S0 | Sampling frequency |
|----|----|----|--------------------|
| 0 | 0 | 1 | 8.0 kHz (Initial) |
| 0 | 0 | 1 | 12.8 kHz |
| 0 | 1 | 0 | 16.0 kHz |
| 0 | 1 | 1 | 32.0 kHz |
| 1 | 0 | 0 | 6.4 kHz |
| 1 | 0 | 1 | 4.0 kHz |

3. STOP command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 1 | 1 | C3 | C2 | × | × |

This command aborts playback. When this command is entered, data in FIFO memory is cleared. Bit D3 selects left or right voice whose playback is aborted.

Turn on bit D2 to abort playback of both left and right voices at a time.

| C3 | C2 | Function |
|----|----|--|
| 0 | 0 | Aborts playback of left voice |
| 1 | 0 | Aborts playback of right voice |
| × | 1 | Aborts playback of left and reight voices. |

4. PAUSE command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | C3 | C2 | C1 | × |

This command pauses the current playback or recording operation. Bit D1 enables or disables pausing.

Bit D3 selects left or right voice whose playback is paused. Turn on bit D2 to pause playback of both left and right voices.

| C1 | Function |
|----|--------------------|
| 0 | Starts pausing. |
| 1 | Canceling pausing. |

| C3 | C2 | Function |
|----|----|---|
| 0 | 0 | Pauses playback of left voice |
| 1 | 0 | Pauses playback of right voice |
| × | 1 | Pauses playback of both left and reight voices. |

5. VOLUME command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | H3 | V2 | V1 | V0 |

This command controls the volumes of playback voices.

Bit D3 selects a left or right voice to be volume-controlled during playback. Bits D2 to D0 set a volume.

| H3 | Function |
|----|---------------------------------|
| 0 | Sets the volume of left voice. |
| 1 | Sets the volume of right voice. |

| V2 | V1 | V0 | Volume |
|----|----|----|----------------------|
| 0 | 0 | 0 | 0 dB (Initial value) |
| 0 | 0 | 1 | -3 dB |
| 0 | 1 | 0 | -6 dB |
| 0 | 1 | 1 | -9 dB |
| 1 | 0 | 0 | -12 dB |
| 1 | 0 | 1 | -15 dB |
| 1 | 1 | 0 | -18 dB |
| 1 | 1 | 1 | -21 dB |

6. POWER-DOWN command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 1 | 0 | W3 | W2 | × | × |

When receiving this command, the MSM9842 stops oscillation, minimizes the current consumption, and enters the power-down state. The AOUTL and AOUTR outputs immediately fall to the GND level. Bit D3 enables or disables the powerdown function and bit D2 enables or disables initialization of the internal circuit of the MSM9842.

| W3 | Function |
|----|----------------------------------|
| 0 | Disables the power-down function |
| 1 | Enables the power-down function |
| | W2 |
| | Function |
| | 0 |
| | 1 |

7. VOICE SYNTHESIS METHOD command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 1 | 1 | P3 | P2 | P1 | P0 |

This command selects a voice synthesis method. Bits D3 to D0 select a method. A total of nine voice synthesis methods are selectable. The selected voice synthesis method cannot be changed while playback or recording is in progress.

| P3 | P2 | P1 | P0 | Voice synthesis method |
|----|----|----|----|------------------------------|
| 0 | 0 | 0 | 0 | 4 bit ADPCM2 (Initial value) |
| 0 | 0 | 0 | 1 | 5 bit ADPCM2 |
| 0 | 0 | 1 | 0 | 6 bit ADPCM2 |
| 0 | 0 | 1 | 1 | 7 bit ADPCM2 |
| 0 | 1 | 0 | 0 | 8 bit ADPCM2 |
| 0 | 1 | 0 | 1 | 4 bit ADPCM |
| 0 | 1 | 1 | 0 | 8 bit straight PCM |
| 0 | 1 | 1 | 1 | 8 bit non-linear PCM |
| 1 | 0 | 0 | 0 | 16 bit straight PCM |

8. ANALOG SPECIFICATION 1 command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | R3 | R2 | × | R0 |

This command selects the built-in ADC, the external DAC, indication of 2's complement or binary, and the stereophonic or monophonic playback. When the MSM9842 is turned on, the AOUTL and AOUTR pin voltages immediately rise to $1/2 V_{DD}$.

| R3 | Function | | |
|----|--------------------------------|------------------------------|--|
| 0 | 2's complement (Initial value) | | |
| 1 | Binary | | |
| | R2 | Function | |
| | 0 | Internal DAC (Initial value) | |
| | 1 | External DAC | |
| | | R0 | Function |
| | | 0 | Monophonic playback mode |
| | | 1 | Stereophonic playback mode (Initial value) |

9. ANALOG SPECIFICATION 2 and DATA BUS LENGTH SET Command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | A3 | A2 | E1 | E0 |

D3 selects use or disuse of the internal output amplifiers to the AOUTL Pin and the AOUTR Pin. D2 selects use or disuse of the internal LPFs to the AOUTL Pin and the AOUTR Pin. D1 and D0 set a data bus length and also select use or disuse for voice data transfer when the 8-bit bus is set.

| A3 | Function | | | |
|----|---------------------------------------|--------------------------|----|---|
| 0 | With output amplifier (Initial value) | | | |
| 1 | Without output amplifier | | | |
| | A2 | Function | | |
| | 0 | With LPF (Initial value) | | |
| | 1 | Without LPF | | |
| | | E1 | E0 | Function |
| | | 0 | 0 | D15 to D8 not used for 8-bit bus length (Initial value) |
| | | 0 | 1 | D15 to D8 used for 8-bit bus length |
| | | 1 | × | 16-bit bus length |

10. FIFO MEMORY SPECIFICATION command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 1 | 0 | × | B2 | B1 | B0 |

The command sets a FIFO memory capacity and selects a requirement of FIFO memory operation. D1 and D0 set a FIFO memory capacity (word configuration).

D2 selects a requirement of operation as described below.

Recording

Setting D2 to "0", when the LSI device has written data to more than half (MID="H") of a FIFO memory capacity, allows the data to be read externally.

Setting D2 to "1", when the LSI device has written data to the whole (FUL="H") of a FIFO memory capacity, allows the data to be read externally.

Playback

Setting D2 to "0", when data has been written to more than half (MID="H") of a FIFO memory capacity externally, allows the LSI device to start reading the data.

Setting D2 to "1", when data has been written to the whole (FUL="H") of a FIFO memory capacity externally, allows the LSI device to start reading the data.

| B1 | B0 | 8-bit bus configuration | 16-bit bus configuration |
|----|--|-------------------------|--------------------------|
| 0 | 0 | 512 bits (64 words) | 512 bits (32 words) |
| 0 | 1 | 1024 bits (128 words) | 1024 bits (64 words) |
| 1 | 0 | 256 bits (32 words) | 256 bits (16 words) |
| 1 | 1 | FIFO memory not used | |
| B2 | Function | | |
| 0 | FIFO data can be written and read when MID="H" | | |
| 1 | FIFO data can be written and read when FUL="H" | | |

Note : For stereophonic playback, the word configuration cannot be selected.

11. SIGNAL OUTPUT FORMAT CONTROL command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 1 | 1 | F3 | D2 | D1 | D0 |

This command sets the output formats of the EMP, MID, FUL, DREQL, and DREQR pins and the input formats of the DACKL and DACKR pins.

| F3 | Function | | | |
|----|---|---|--|--------------------|
| 0 | EMP, MID, FUL outputs : Active high (Initial value) | | | |
| 1 | EMP, MID, FUL outputs : Active low | | | |
| | D2 | Function | | |
| | 0 | DREQL and DREQR outputs : Active high (Initial value) | | |
| | 1 | DREQL and DREQR outputs : Active low | | |
| | | D1 | Function | |
| | | 0 | DACK input : Active high (Initial value) | |
| | | 1 | DACK input : Active low | |
| | | | D0 | Function |
| | | | 0 | No function |
| | | | 1 | For test. Not used |

12. DMA TRASFER SET command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 0 | G3 | G2 | G1 | × |

This command sets use or disuse of DMA transfer and selects DMA transfer modes.

| G3 | G2 | G1 | Function |
|----|----|----|----------------------------------|
| 0 | × | × | Without transfer (Initial value) |
| 1 | 0 | 0 | Single mode DMA transfer |
| 1 | 0 | 1 | Block mode DMA transfer |

13. TEST command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 1 | T3 | T2 | T1 | T0 |

This command is used for test.

Description of Status

The MSM9842 supports the following seven status flags :

| | | |
|----|----------------------------------|--|
| D7 | Left Data Recording/Playing flag | High when recording or playback is in progress |
| D6 | Right Data Playing flag | High when playback is in progress |
| D5 | Left Pause flag | High when playback of left voice is paused |
| D4 | Right Pause flag | High when playback of right voice is paused |
| D3 | EMP Information Output flag | Output the same signal as the EMP pin. |
| D2 | MID Information Output flag | Output the same signal as the MID pin. |
| D1 | FUL Information Output flag | Output the same signal as the FUL pin. |
| D0 | Data Transfer Error flag | See the explanation below. |

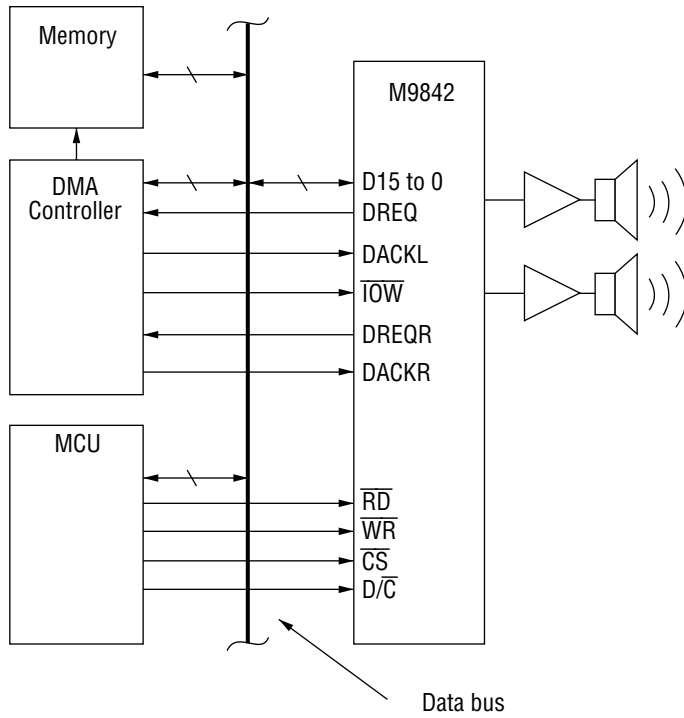
The MSM9842 supports the following two data transfer errors :

When FIFO memory is used

- (1) "H" when a read operation is mode while EMP is "H"
- (2) "H" when a write operation is mode while FUL is "H"

CPU INTERFACE EXAMPLES

1) Interface when DMA controller is used (16-bit bus)



2) MCU & external memory interface (16-bit bus)

