MOTOROLA

MC14544B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER FOR LIQUID CRYSTALS

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

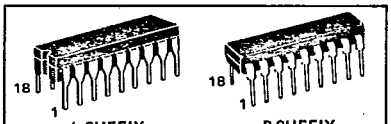
For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0 nA/package typical @ 5 V
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



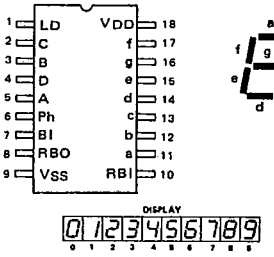
L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Input Current per Pin	I_{in}	±10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level (V_O = 4.5 or 0.5 V) (V_O = 9.0 or 1.0 V) (V_O = 13.5 or 1.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 V) (V_O = 1.0 or 9.0 V) (V_O = 1.5 or 13.5 V)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device) (V_{OH} = 2.5 V) Source (V_{OH} = 4.6 V) (V_{OH} = 0.5 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mA
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–	–	–	–10.1	–	–	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink (V_{OL} = 0.5 V) (V_{OL} = 9.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
		10	1.6	–	1.3	2.25	–	0.9	–	
		10	–	–	–	10.1	–	–	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device) (V_{OH} = 2.5 V) Source (V_{OH} = 4.6 V) (V_{OH} = 0.5 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0	–2.5	–	–2.1	–4.2	–	–1.7	–	mA
		5.0	–0.52	–	–0.44	–0.88	–	–0.36	–	
		10	–	–	–	–10.1	–	–	–	
		10	–1.3	–	–1.1	–2.25	–	–0.9	–	
		15	–3.6	–	–3.0	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink (V_{OL} = 0.5 V) (V_{OL} = 9.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
		10	1.3	–	1.1	2.25	–	0.9	–	
		10	–	–	–	10.1	–	–	–	
		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package) V_{in}=0 or V_{DD}, I_{out} = 0 µA	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µA
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package) V_{in}=0 or V_{DD}, I_{out} = 0 µA	I_{DD}	5.0	–	20	–	0.005	20	–	150	µA
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µA
		10	I_T = (3.1 µA/kHz) f + I_{DD}							
		15	I_T = (4.7 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

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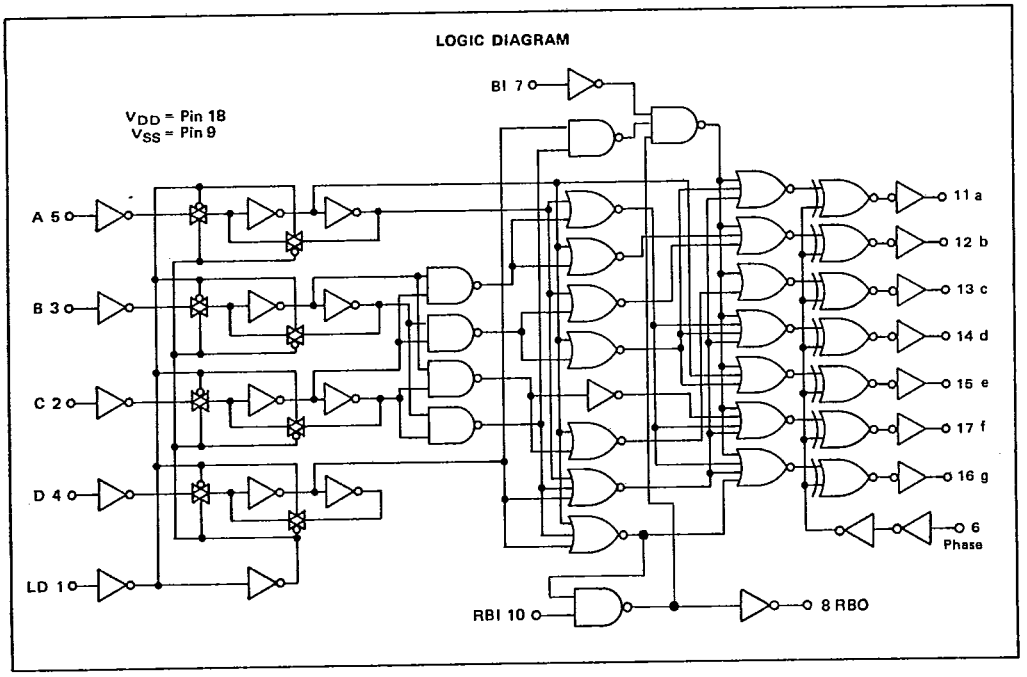
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0 ns/pF) C_L + 30 ns t_{TLH} = (1.5 ns/pF) C_L + 15 ns t_{TLH} = (1.1 ns/pF) C_L + 10 ns	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{THL} = (0.55 ns/pF) C_L + 12.5 ns	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Turn-Off Delay Time t_{PLH} = (1.7 ns/pF) C_L + 520 ns t_{PLH} = (0.66 ns/pF) C_L + 217 ns t_{PLH} = (0.5 ns/pF) C_L + 160 ns	t_{PLH}	5.0 10 15	– – –	605 250 185	1210 500 370	ns
Turn-On Delay Time t_{PHL} = (1.7 ns/pF) C_L + 420 ns t_{PHL} = (0.66 ns/pF) C_L + 172 ns t_{PHL} = (0.5 ns/pF) C_L + 130 ns	t_{PHL}	5.0 10 15	– – –	505 205 155	1650 660 495	ns
Setup Time	t_{su}	5.0 10 15	0 0 0	-40 -15 -10	– – –	ns
Hold Time	t_h	5.0 10 15	80 30 20	40 15 10	– – –	ns
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0 10 15	250 100 80	125 50 40	– – –	ns

*The formulas given are for the typical characteristics only.

LOGIC DIAGRAM



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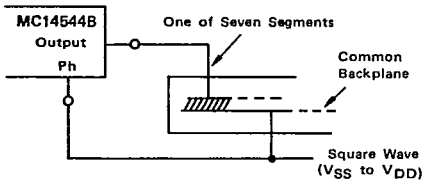
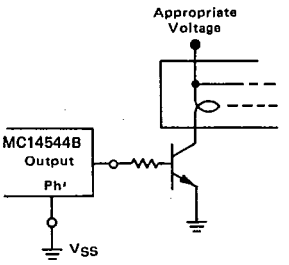
CONNECTIONS TO VARIOUS DISPLAY READOUTS

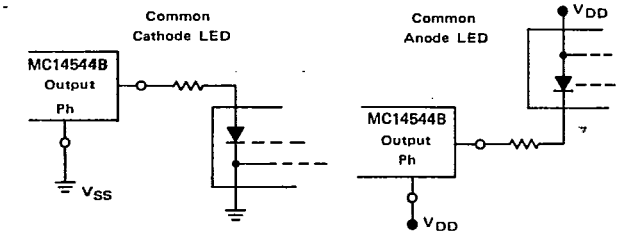
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

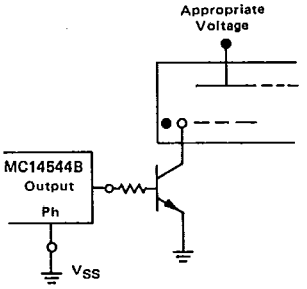


LIGHT EMITTING DIODE (LED) READOUT



Note: Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT



TRUTH TABLE

INPUTS								OUTPUTS							
RBI	LD	BI	Ph*	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	1	0	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2
X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
X	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	4
X	1	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5
X	1	0	0	0	1	1	0	0	1	0	1	1	1	1	1	6
X	1	0	0	0	1	1	1	0	1	1	1	0	0	0	0	7
X	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	8
X	1	0	0	1	0	0	1	0	1	1	1	1	0	1	1	9
X	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	X	X	#	**							**
†	†	†	1	†				†	Inverse of Output Combinations Above							Display as above

X Don't Care

† Above Combinations

* For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.

** Depends upon the BCD Code previously applied when LD = 1.

\# RBO=RBI • ($\overline{A}\overline{B}\overline{C}\overline{D}$)

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FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

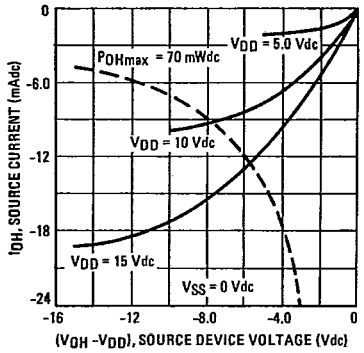


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

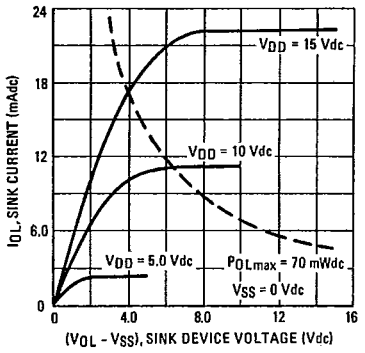


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

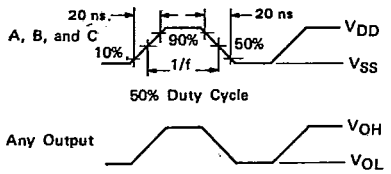
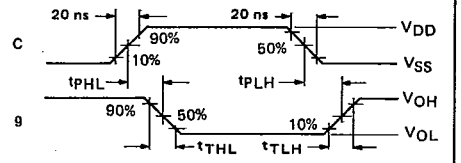
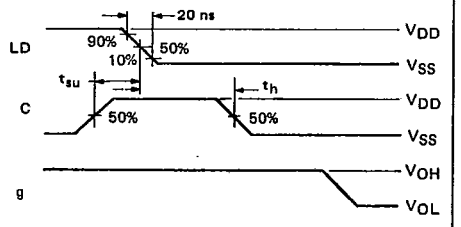


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

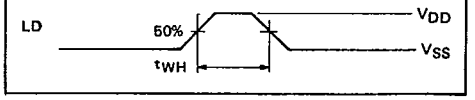
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches



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TYPICAL APPLICATIONS FOR RIPPLE BLANKING