

TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D2661, DECEMBER 1982 — REVISED DECEMBER 1983

- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil DIPs. The 'AS881A Is Offered in 300-mil DIPs. Both Devices Are Available in Both Plastic and Ceramic Chip Carriers

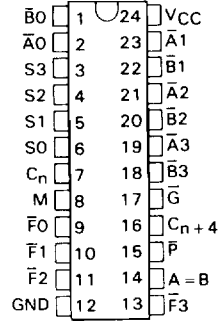
- Full Look-Ahead for High-Speed Operations on Long Words

- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations

- Logic Function Modes
 - Exclusive-OR Comparator
 - AND, NAND, OR, NOR
 - 'AS881A Provides Status Register Checks
 - Plus Ten Other Logic Operations

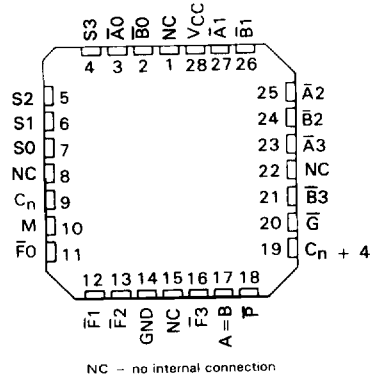
- Dependable Texas Instruments Quality and Reliability

SN54AS181A J OR JT PACKAGE
SN54AS881A JT PACKAGE
SN74AS181A N OR NT PACKAGE
SN74AS881A NT PACKAGE
(TOP VIEW)

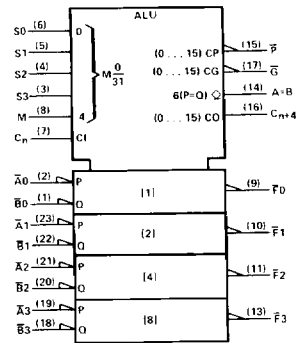


SN54AS181A, SN54AS881A FH PACKAGE
SN74AS181A, SN74AS881A FN PACKAGE

'AS181A, 'AS881A
(TOP VIEW)



logic symbol



Pin numbers shown are J, JT, N and NT packages.

TYPICAL ADDITION TIMES ($C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, $T_A = 25^\circ\text{C}$)

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALU's
	USING 'AS881A AND 'AS882	USING 'AS181A AND 'AS882	USING 'S181 AND 'S182	ARITHMETIC LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

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ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\bar{A}O$	$\bar{B}O$	$\bar{A}1$	$\bar{B}1$	$\bar{A}2$	$\bar{B}2$	$\bar{A}3$	$\bar{B}3$	$\bar{F}O$	$\bar{F}1$	$\bar{F}2$	$\bar{F}3$	C_n	C_{n+4}	\bar{P}	\bar{G}
Active-high data (Table 2)	AO	BO	A1	B1	A2	B2	A3	B3	FO	F1	F2	F3	\bar{C}_n	\bar{C}_{n+4}	X	Y

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Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A - B - 1$, which requires an end-around or forced carry to provide $A - B$.

The 'AS181A and 'AS881A can also be utilized as a comparator. The $A = B$ output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A = B$). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the \bar{P} , \bar{G} , and C_{n+4} outputs when the device is in the logic mode ($M=H$).

In the logic mode the 'AS881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the \bar{P} , \bar{G} and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\begin{aligned}\bar{P} &= F_0 + F_1 + F_2 + F_3 \\ \bar{G} &= H \\ C_{n+4} &= PC_n\end{aligned}$$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

C _n	S ₀ =S ₃ =H, S ₁ =S ₂ =L, and M=H				DATA INPUTS			OUTPUTS		
	A ₀ =B ₀	A ₁ =B ₁	A ₂ =B ₂	A ₃ =B ₃	\bar{G}	\bar{P}	C _{n+4}	H	L	H
H	A ₀ =B ₀	A ₁ =B ₁	A ₂ =B ₂	A ₃ =B ₃	H	L	H			
L	A ₀ ≠B ₀	A ₁ ≠B ₁	A ₂ ≠B ₂	A ₃ ≠B ₃	H	L	L			
X	A ₀ ≠B ₀	X	X	X	H	H	L			
X	X	A ₁ ≠B ₁	X	X	H	H	L			
X	X	X	A ₂ ≠B ₂	X	H	H	L			
X	X	X	X	A ₃ ≠B ₃	H	H	L			

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

C _n	S ₀ =S ₁ =S ₃ =L, S ₂ =H, and M=H						DATA INPUTS			OUTPUTS		
	\bar{A}_0 or $\bar{B}_0=L$	\bar{A}_1 or $\bar{B}_1=L$	\bar{A}_2 or $\bar{B}_2=L$	\bar{A}_3 or $\bar{B}_3=L$	\bar{G}	\bar{P}	C _{n+4}	H	L	H		
H	\bar{A}_0 or $\bar{B}_0=L$	\bar{A}_1 or $\bar{B}_1=L$	\bar{A}_2 or $\bar{B}_2=L$	\bar{A}_3 or $\bar{B}_3=L$	H	L	H					
L	\bar{A}_0 or $\bar{B}_0=L$	\bar{A}_1 or $\bar{B}_1=L$	\bar{A}_2 or $\bar{B}_2=L$	\bar{A}_3 or $\bar{B}_3=L$	H	L	L					
X	\bar{A}_0 or $\bar{B}_0=H$	X	X	X	H	H	L					
X	X	\bar{A}_1 or $\bar{B}_1=H$	X	X	H	H	L					
X	X	X	\bar{A}_2 or $\bar{B}_2=H$	X	H	H	L					
X	X	X	X	\bar{A}_3 or $\bar{B}_3=H$	H	H	L					

The combination of signals on the S₃ through S₀ control lines determine the operation performed on the data words to generate the output bits F_i. By monitoring the \bar{P} and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an A = B status while the exclusive-OR (⊕) function is being utilized. When the control inputs (S₃, S₂, S₁, S₀) equal H, L, L, H; a status check is generated to determine whether all pairs (A_i, B_i) are equal in the following manner: $\bar{P} = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole \bar{P} output is particularly useful when cascading 'AS881's. As the A = B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode (\bar{P} and \bar{G}). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs (\bar{A}_i , \bar{B}_i) being high, it is necessary to set the control lines (S₃, S₂, S₁, S₀) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\bar{P} = \bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$.

S ₃	S ₂	S ₁	S ₀	M	$\bar{P} = F_0 + F_1 + F_2 + F_3$
L	H	L	L	H	$\bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$
H	L	L	H	H	$(A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$

signal designations

In both Figures 1 and 2, the polarity indicators ($\bar{\square}$) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181 and 'AS881 together with the 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

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TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

2 ALAS AND AS CIRCUITS

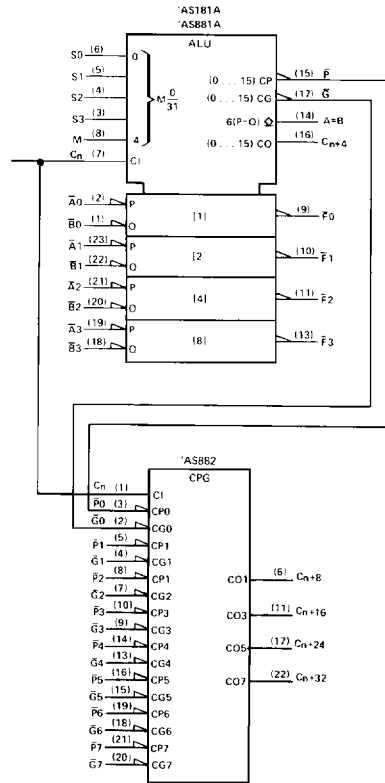


FIGURE 1
(USE WITH TABLE 1)

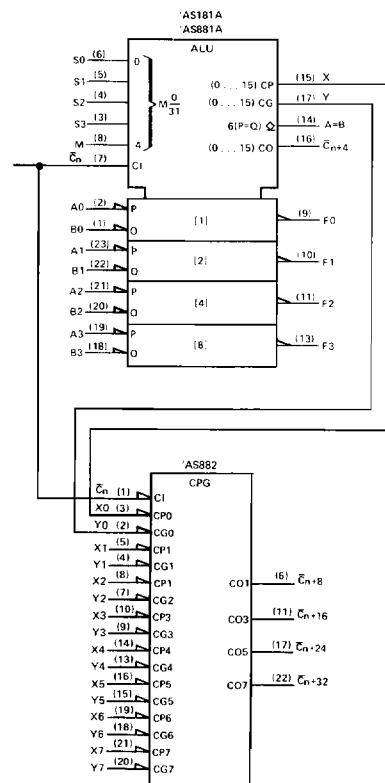


FIGURE 2
(USE WITH TABLE 2)

TABLE 1

SELECTION	ACTIVE-LOW DATA			
	M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS		C _n = H (with carry)
		C _n = L (no carry)		
L L L L	F = \bar{A}	F = A MINUS 1	F = A	
L L L H	F = $\bar{A}\bar{B}$	F = AB MINUS 1	F = AB	
L L H L	F = $\bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$	
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO	
L H L L	F = $\bar{A} + \bar{B}$	F = A PLUS (A + \bar{B})	F = A PLUS (A + \bar{B}) PLUS 1	
L H L H	F = \bar{B}	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1	
L H H L	F = $\bar{A} \odot B$	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = A + \bar{B}	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
H L L L	F = $\bar{A}\bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1	
H L L H	F = A \odot B	F = A PLUS B	F = A PLUS B PLUS 1	
H L H L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1	
H L H H	F = A + B	F = (A + B)	F = (A + B) PLUS 1	
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1	
H H L H	F = $\bar{A}\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1	
H H H L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1	
H H H H	F = A	F = A	F = A PLUS 1	

* Each bit is shifted to the next more significant position.

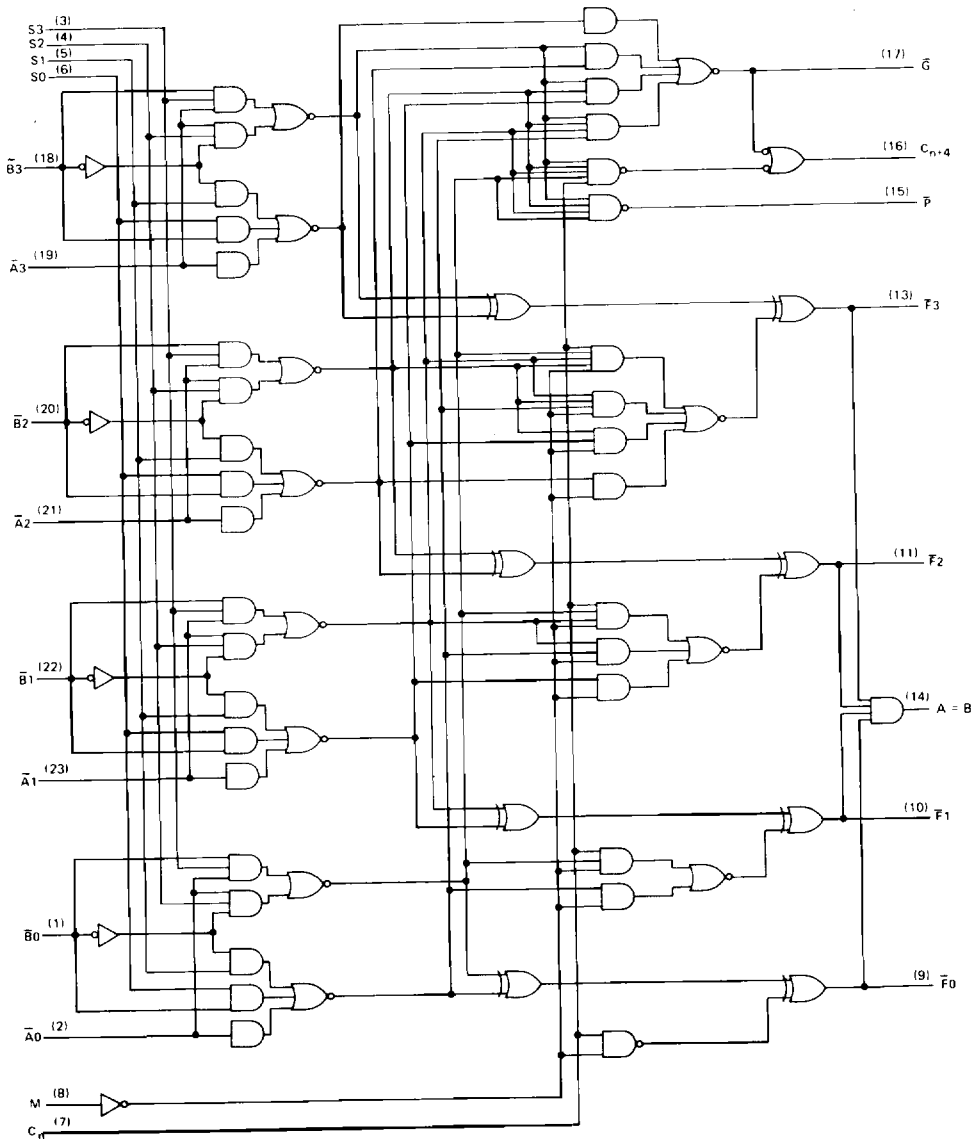
TABLE 2

SELECTION	ACTIVE-HIGH DATA			
	M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS		C _n = L (with carry)
		C _n = H (no carry)		
L L L L	F = \bar{A}	F = A	F = A PLUS 1	
L L L H	F = $\bar{A} + \bar{B}$	F = A + B	F = (A + B) PLUS 1	
L L H L	F = $\bar{A}\bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO	
L H L L	F = $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1	
L H L H	F = \bar{B}	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1	
L H H L	F = A \odot B	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = $\bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$	
H L L L	F = $\bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1	
H L L H	F = A \odot B	F = A PLUS B	F = A PLUS B PLUS 1	
H L H L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1	
H L H H	F = AB	F = AB MINUS 1	F = AB	
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1	
H H L H	F = A + \bar{B}	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1	
H H H L	F = A + B	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1	
H H H H	F = A	F = A MINUS 1	F = A	

TYPES SN54AS181A, SN74AS181A
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)

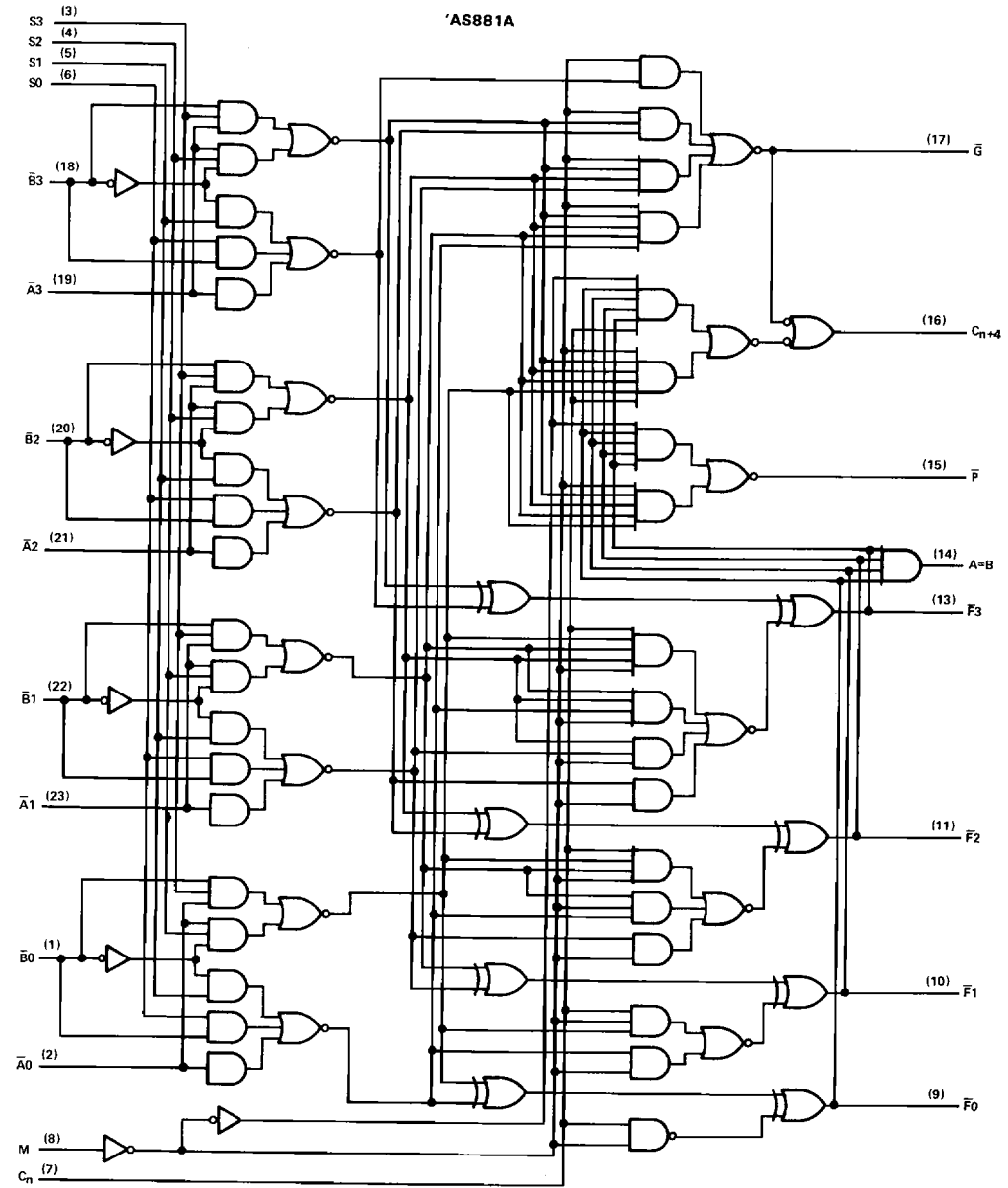
'AS181A



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 ALS AND AS CIRCUITS

**TYPES SN54AS881A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

logic diagram (positive logic)



**2
ALS AND AS CIRCUITS**

**TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Off-state output voltage (A = B output only)	7 V
Operating free-air temperature range: SN54AS181A, SN54AS881A	- 55 °C to 125 °C
SN74AS181A, SN74AS881A	0 °C to 70 °C
Storage temperature range	- 65 °C to 150 °C

recommended operating conditions

		SN54AS*			SN74AS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current	A = B output only						
		All outputs except A = B and \bar{G}			-2		-2	mA
		\bar{G}			-3		-3	mA
I_{OL}	Low-level output current	All outputs except \bar{G}			20		20	mA
		\bar{G}			48		48	mA
T_A	Operating free-air temperature		-55	125		0	70	°C

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ALS AND AS CIRCUITS

TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS*			SN74AS*			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}	Any output except A = B V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA			V _{CC} - 2			V _{CC} - 2	V	
V _{OH}	\bar{G} V _{CC} = 4.5 V, I _{OH} = -3 mA			2.4	3.4		2.4 3.4	V	
I _{OH}	A = B V _{CC} = 4.5 V, V _{OH} = 5.5 V						0.1	mA	
V _{OL}	Any output except \bar{G} V _{CC} = 4.5 V, I _{OL} = 20 mA			0.3	0.5		0.3 0.5	V	
V _{OL}	\bar{G} V _{CC} = 4.5 V, I _{OL} = 48 mA			0.4	0.5		0.4 0.5	V	
I _I	M input	V _{CC} = 5.5 V, V _I = 7 V					0.1	mA	
	Any A or B input						0.3		
	Any S input						0.4		
	Carry input						0.6		
I _{IH}	M input	V _{CC} = 5.5 V, V _I = 2.7 V					20	μA	
	Any A or B input						60		
	Any S input						80		
	Carry input						120		
I _{IL}	M input	V _{CC} = 5.5 V, V _I = 0.4 V					-2	mA	
	Any A or B input						-6		
	Any S input						-8		
	Carry input						-12		
I _O ‡	All outputs except A = B and \bar{G}	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-45	-112	-30	-45	-112	mA
	\bar{G}							-165	
I _{CC}	V _{CC} = 5.5 V	'AS181A	135	200		135	200	mA	
		'AS881A	135	210		135	210		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

2 ALS AND AS CIRCUITS

TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 5 V, C _L = 15 pF, R _L = 500 Ω (280 Ω for A=B), T _A = 25 °C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF (15 pF for A=B), R _L = 500 Ω (280 Ω for A=B), T _A = MIN to MAX				UNIT		
				'AS181A 'AS881A		SN54AS181A SN54AS881A		SN74AS181A SN74AS881A				
				MIN	TYP†	MAX	MIN	TYP†	MAX		MIN	TYP†
t _{pd}	C _n	C _{n+4}		5		2	7	11	2	7	9	ns
t _{pd}	Any \bar{A} or \bar{B}	C _{n-4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	6		2	8	14	2	8	12	ns
t _{pd}	Any \bar{A} or \bar{B}	C _{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	7		2	8	20	2	8	16	ns
t _{pd}	C _n	Any \bar{F}	M = 0 V (SUM or DIFF mode)	5		3	6	11	3	6	9	ns
t _{pd}	Any \bar{A} or \bar{B}	\bar{G}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	4		2	5	9	2	5	7	ns
t _{pd}	Any \bar{A} or \bar{B}	\bar{G}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	5		2	6	12	2	6	9	ns
t _{pd}	Any \bar{A} or \bar{B}	\bar{P}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	5		2	6	11	2	6	8	ns
t _{pd}	Any \bar{A} or \bar{B}	\bar{P}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	5		2	6	13	2	6	10	ns
t _{pd}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V (SUM mode)	5		2	5	11	2	5	8	ns
t _{pd}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 0 V, S0 = S1 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	5		2	6	12	2	6	10	ns
t _{pd}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 4.5 V (LOGIC mode)	6		2	6	16	2	6	11	ns
t _{pd}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	12		4	14	26	4	14	21	ns

additional 'AS881A switching characteristics involving status checks (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 5 V, C _L = 15 pF, R _L = 500 Ω, T _A = 25 °C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT		
				'AS881A		SN54AS881A		SN74AS881A				
				MIN	TYP†	MAX	MIN	TYP†	MAX		MIN	TYP†
t _{pd}	Any \bar{A} or \bar{B}	\bar{P}	C _n = 4.5 V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\bar{A}_i = \bar{B}_i$ or $\bar{A}_i \neq \bar{B}_i$)	8		2	10	19	2	10	15	ns
t _{pd}	Any \bar{A} or \bar{B}	C _{n+4}	C _n = 4.5 V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\bar{A}_i = \bar{B}_i$ or $\bar{A}_i \neq \bar{B}_i$)	10		2	12	24	2	12	18	ns
t _{pd}	Any \bar{A} or \bar{B}	\bar{P}	C _n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\bar{A}_i = \bar{B}_i = H$ or \bar{A}_i or $\bar{B}_i = L$)	8		2	10	19	2	10	15	ns
t _{pd}	Any \bar{A} or \bar{B}	C _{n+4}	C _n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\bar{A}_i = \bar{B}_i = H$ or \bar{A}_i or $\bar{B}_i = L$)	11		2	13	25	2	13	19	ns

t_{pd} = t_{PHL} or t_{PLH}

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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ALS AND AS CIRCUITS

TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = M = 0\text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PLH}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5\text{ V}$, $S_0 = S_3 = M = 0\text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	Out-of-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	In-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	$A - B$	In-Phase
t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A - B$	Out-of-Phase
t_{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	C_{n+4} or any \bar{F}	In-Phase
t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	In-Phase

NOTE A: For load circuit and voltage waveforms, see page 1-12.

2 ALS AND AS CIRCUITS

**TYPES SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{F}_i	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{F}_i	Out-of-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE

FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	Out-of-Phase
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	In-Phase
t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{A} and \bar{B} , C _n	None	\bar{P}	In-Phase
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	C _n + 4	In-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C _n	None	C _n + 4	In-Phase
t _{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A} and \bar{B} , C _n	None	C _n + 4	Out-of-Phase
t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{A} and \bar{B} , C _n	None	C _n + 4	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE

FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} , C _n	Remaining \bar{B}	\bar{P}	In-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{B} , C _n	Remaining \bar{A}	\bar{P}	In-Phase
t _{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} , C _n	Remaining \bar{B}	C _n + 4	Out-of-Phase
t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{B} , C _n	Remaining \bar{A}	C _n + 4	Out-of-Phase

NOTE A: For load circuit and voltage waveforms, see page 1-12.

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ALS AND AS CIRCUITS**