NEC

MOS INTEGRATED CIRCUIT

μPD98404

Phase-out/Discontinued

ADVANCED ATM SONET FRAMER

DESCRIPTION

The μPD98404 NEASCOT-P30™ is an LSI for ATM applications, which can be used in ATM adapter boards for connecting PCs or workstations to an ATM network and can also be used in ATM hubs and ATM switches. This LSI provides the TC sub-layer functions in the SONET/SDH-base physical layer within the ATM protocol defined by the ATM Forum's UNI3.1 recommendations.

This product's main functions include transmission functions such as mapping of ATM cells sent from the ATM layer to the payload field in a 155 Mbps SONET STS-3c/SDH STM-1 frame and transmission to PMD (Physical Media Dependent) sub-layer in the physical layer. Its reception functions include separation of the overhead from the ATM cells in data streams received from PMD sub-layer and transmission of the ATM cells to the ATM layer. In addition, this LSI includes a clock recovery function that extracts a reception sync clock from bit streams in received data and a clock synthesis function that generates a clock for transmissions.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD98404 User's Manual: S11821E

FEATURES

- On-chip clock recovery/clock synthesis functions
- Provides TC sub-layer function for the ATM protocol's physical layer
- Supported frame formats include 155 Mbps SONET STS-3c/SDH STM-1
- Conforms to ATM Forum UTOPIA interface Level 2 V1.0 (af-phy-0039.000 June 1995)
  Supports three UTOPIA interfaces:
  - Single PHY octet-level handshaking
  - Single PHY cell-level handshaking
  - Multi PHY mode
- Selectable to drop/bypass unassigned cells
- On-chip internal loopback functions for PMD layer loopback and ATM layer loopback
- Supports two PMD interfaces: serial and parallel
  - 155.52 Mbps serial interface
  - 19.44 MHz parallel interface
- Provides registers for writing/reading overhead information
  SOH (section overhead) :J0 byte, Z0 (first and second) bytes, F1 byte
  LOH (line overhead) :K1 byte, K2 byte
  POH (path overhead) :F2 byte, C2 byte, H4 byte
- Provides pseudo error frame transmit function for various errors
- Supports JTAG boundary scan test function (IEEE 1149.1)
- CMOS technology
- +3.3 V single power supply

Document No. S11822EJ5V0DS00 (5th edition)
Date Published April 2002 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

- Provides abundant OAM (Operation and Maintenance) functions

Transmit side

- Transmission of various alarm data
  - * Source-triggered automatic loopback transmission
    - Line RDI, Path RDI
    - Line REI, Path REI
  - * Command-specified transmission
    - Line AIS, Path AIS
- Pseudo error generation frame transmit functions
  - LOS generated frame
  - OOF, LOF generated frame
  - LOP generated frame
  - OCD, LCD generated frame
  - B1 error generated frame
  - B2 error generated frame
  - B3 error generated frame

Receive side

- Detection of alarm and fault signals
  - LOS (Loss Of Signal)
  - OOF (Out Of Frame)
  - LOF (Loss Of Frame)
  - LOP (Loss Of Pointer)
  - OCD (Out of Cell Delineation)
  - LOC (Loss Of Cell delineation)
  - Line RDI, Path RDI
  - Line AIS, Path AIS
- Detection and display of quality loss sources
  - B1 error, B2 error, B3 error,
  - Line REI, Path-REI
- On-chip error counters
  - B1 byte error counter (16-bit)
  - B2 byte error counter (20-bit)
  - B3 byte error counter (16-bit)
  - Line REI error counter (20-bit)
  - Path REI error counter (16-bit)
  - Rx Frequency justification processing counter (12-bit)
  - HEC error drop cell counter (20-bit)
  - FIFO overflow drop cell counter (20-bit)
  - Idle cell counter (20-bit)

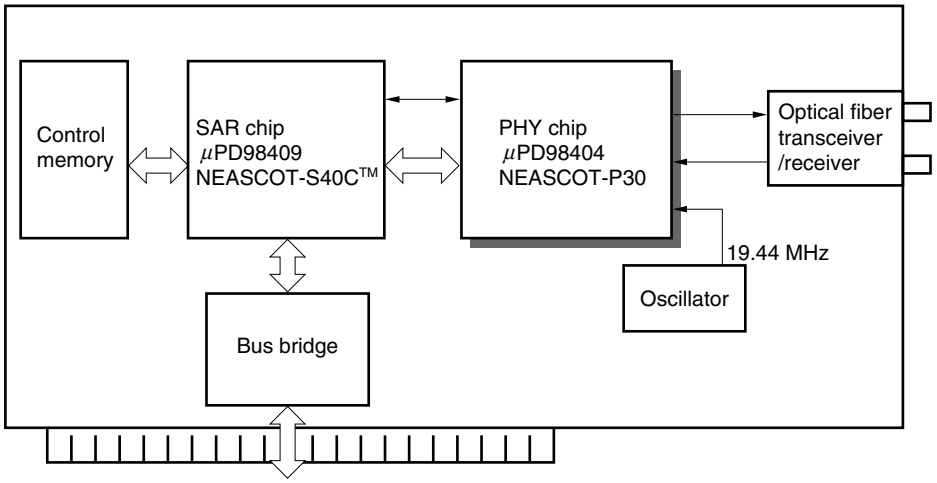
ORDERING INFORMATION

Part number	Package
μPD98404GJ-KEU	144-pin plastic QFP (fine pitch) (20 × 20)

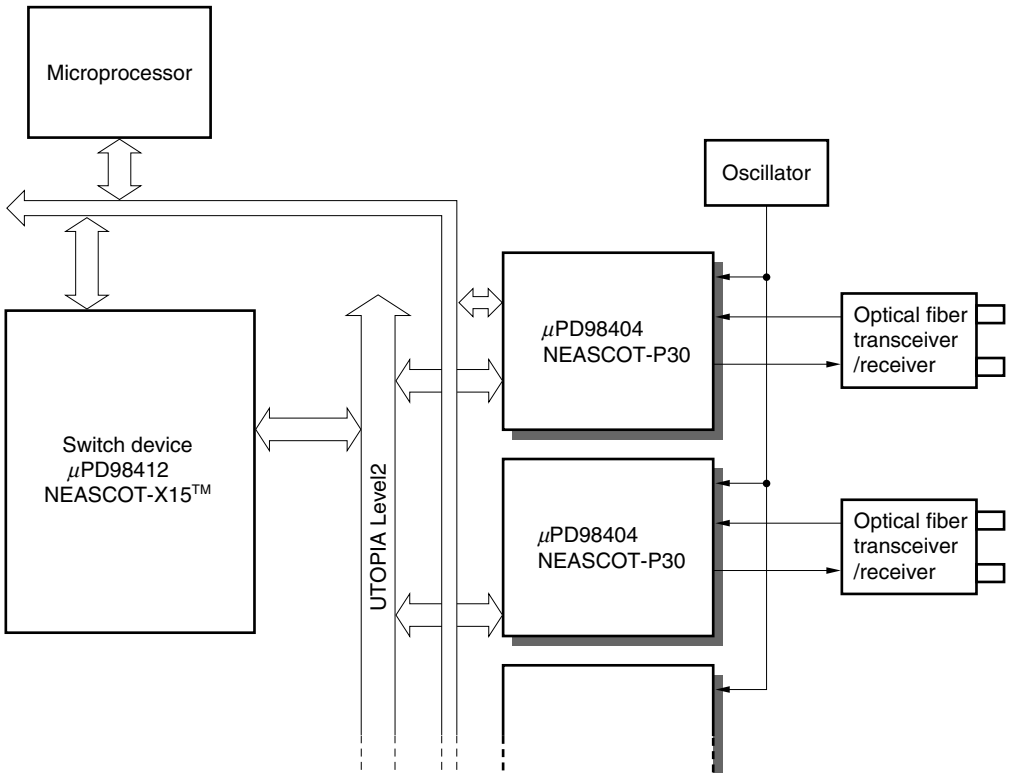
SYSTEM CONFIGURATION EXAMPLE

The following is an example of a system configuration using the μPD98404.

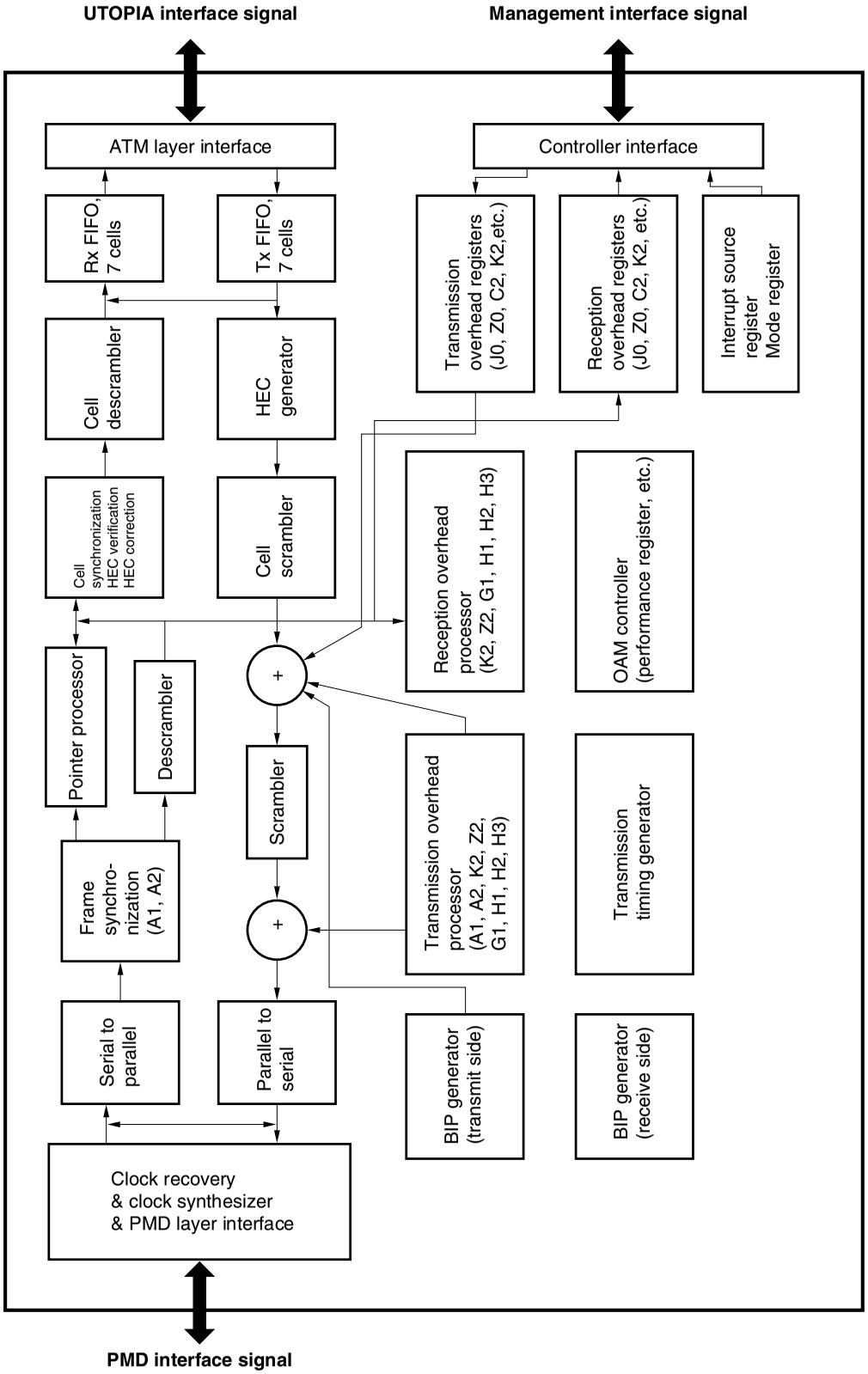
★ **ATM adapter card application**



Hub (terminal side) application

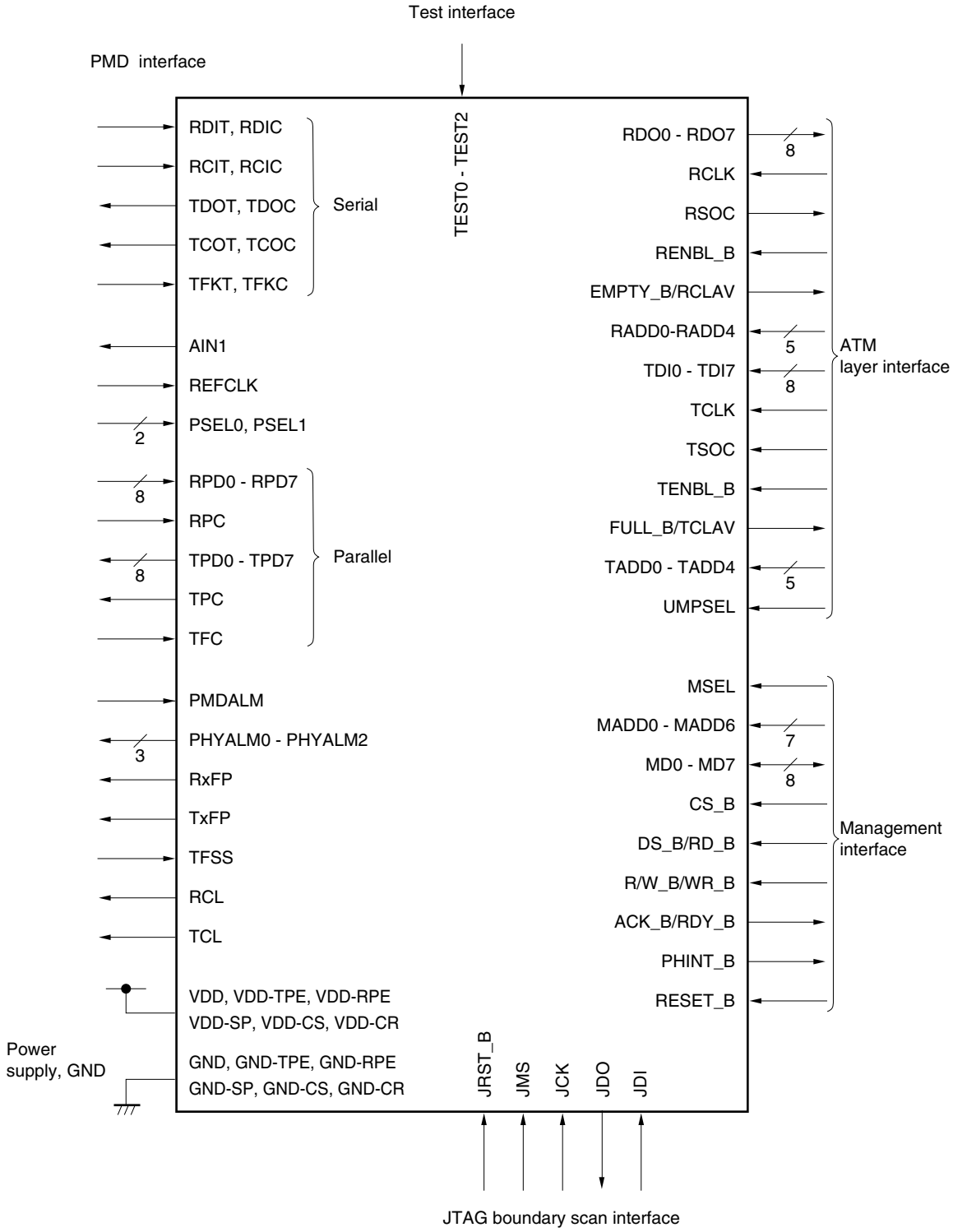


BLOCK DIAGRAM



Phase-out/Discontinued

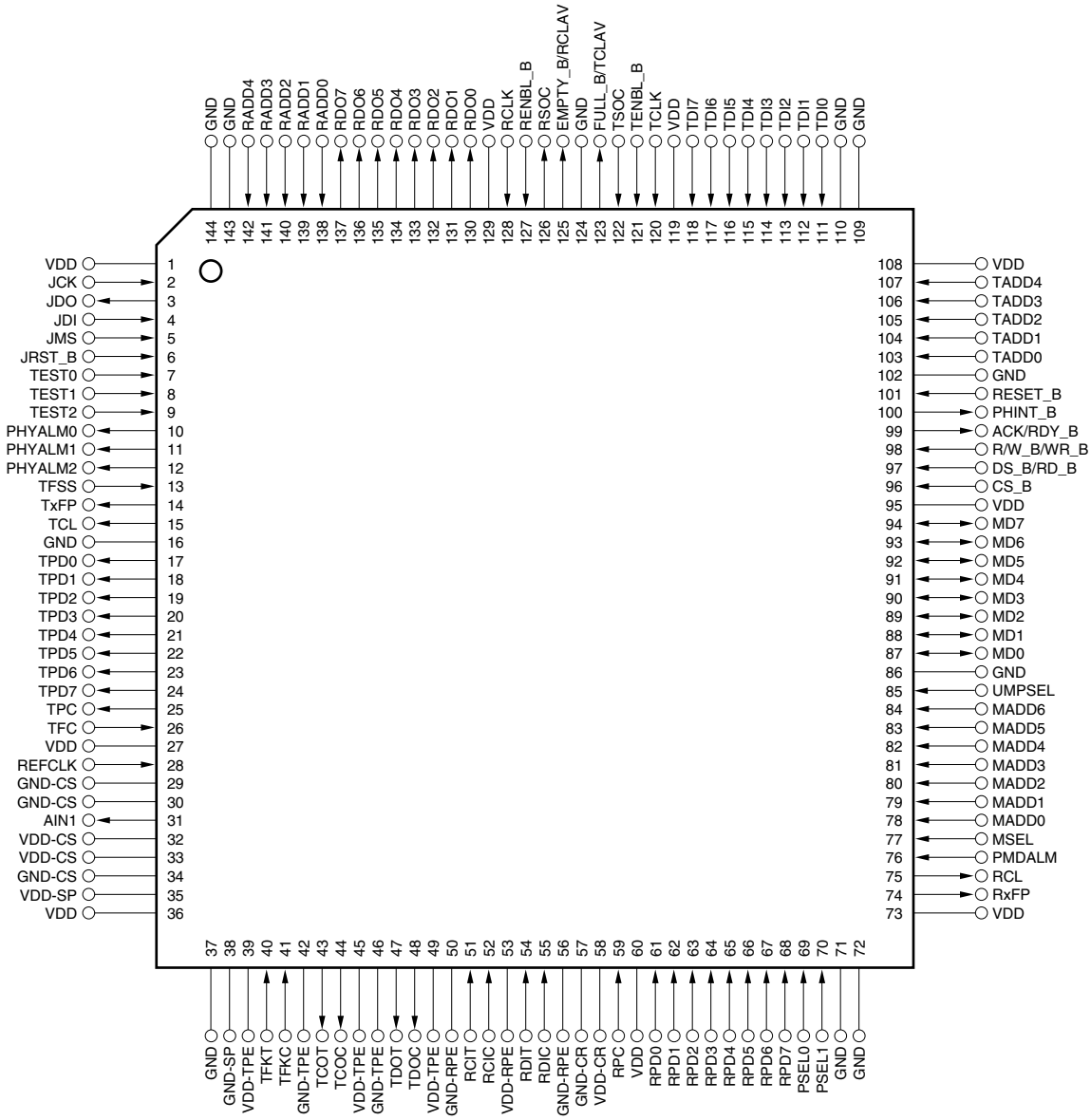
PIN CONFIGURATION



Remark Active low pins are indicated with the suffix "_B" in this document.

PIN CONFIGURATION (TOP VIEW)

144-pin plastic QFP (fine pitch) (20 × 20)



PIN ALLOCATION

Number	Pin name	Number	Pin name	Number	Pin name	Number	Pin name
1	VDD	37	GND	73	VDD	109	GND
2	JCK	38	GND-SP	74	RxFP	110	GND
3	JDO	39	VDD-TPE	75	RCL	111	TDI0
4	JDI	40	TFKT	76	PMDALM	112	TDI1
5	JMS	41	TFKC	77	MSEL	113	TDI2
6	JRST_B	42	GND-TPE	78	MADD0	114	TDI3
7	TEST0	43	TCOT	79	MADD1	115	TDI4
8	TEST1	44	TCOC	80	MADD2	116	TDI5
9	TEST2	45	VDD-TPE	81	MADD3	117	TDI6
10	PHYALM0	46	GND-TPE	82	MADD4	118	TDI7
11	PHYALM1	47	TDOT	83	MADD5	119	VDD
12	PHYALM2	48	TDOC	84	MADD6	120	TCLK
13	TFSS	49	VDD-TPE	85	UMPSEL	121	TENBL_B
14	TxFP	50	GND-RPE	86	GND	122	TSOC
15	TCL	51	RCIT	87	MD0	123	FULL_B/TCLAV
16	GND	52	RCIC	88	MD1	124	GND
17	TPD0	53	VDD-RPE	89	MD2	125	EMPTY_B/RCLAV
18	TPD1	54	RDIT	90	MD3	126	RSOC
19	TPD2	55	RDIC	91	MD4	127	RENBL_B
20	TPD3	56	GND-RPE	92	MD5	128	RCLK
21	TPD4	57	GND-CR	93	MD6	129	VDD
22	TPD5	58	VDD-CR	94	MD7	130	RDO0
23	TPD6	59	RPC	95	VDD	131	RDO1
24	TPD7	60	VDD	96	CS_B	132	RDO2
25	TPC	61	RPD0	97	DS_B/RD_B	133	RDO3
26	TFC	62	RPD1	98	R/W_B/WR_B	134	RDO4
27	VDD	63	RPD2	99	ACK_B/RDY_B	135	RDO5
28	REFCLK	64	RPD3	100	PHINT_B	136	RDO6
29	GND-CS	65	RPD4	101	RESET_B	137	RDO7
30	GND-CS	66	RPD5	102	GND	138	RADD0
31	AIN1	67	RPD6	103	TADD0	139	RADD1
32	VDD-CS	68	RPD7	104	TADD1	140	RADD2
33	VDD-CS	69	PSEL0	105	TADD2	141	RADD3
34	GND-CS	70	PSEL1	106	TADD3	142	RADD4
35	VDD-SP	71	GND	107	TADD4	143	GND
36	VDD	72	GND	108	VDD	144	GND

PIN NAMES

ACK_B : Read/write Cycle Receive Acknowledge
AIN1 : External Filter Connection
CS : Chip Select
DS_B : Data Strobe
EMPTY_B : Output Buffer Empty
FULL_B : Buffer Full
GND : Ground
GND-RPE : Ground for Receive PECL Buffer
GND-CR : Ground for Clock Recovery Circuit
GND-CS : Ground for Clock Synthesis
GND-SP : Ground for Serial/Parallel Circuit
GND-TPE : Ground for Transmit PECL Buffer
JCK : JTAG Clock
JDI : JTAG Data Input
JDO : JTAG Data Output
JMS : JTAG Mode Select
JRST_B : JTAG Reset
MADD0-MADD6 : Management Interface Address Bus
MD0-MD7 : Management Interface Data Bus
MSEL : Management Interface Mode Select
PHINT_B : Physical Interrupt
PHYALM0-PHYALM2 : PHY Alarm Detection
PMDALM : PMD Device Alarm
PSEL0, PSEL1 : PMD Mode Select
RADD0-RADD4 : Receive PHY Device Address
RCIC : Receive Clock Input Complement
RCIT : Receive Clock Input True
RCL : Internal Receive System Clock
RCLAV : Receive Cell Available
RCLK : Receive Data Transferring Clock
RD_B : Read Select
RDIC : Receive Data Input Complement
RDIT : Receive Data Input True
RDO0-RDO7 : Receive Data Output
RDY_B : Ready Signal
REFCLK : System Clock
RENBL_B : Receive Data Enable
RESET_B : System Reset
RPC : Receive Parallel Data Clock
RPD0-RPD7 : Receive Parallel Data
RSOC : Receive Start Address of ATM Cell
RxFP : Receive Frame Pulse
R/W_B : Read/write Control
TADD0-TADD4 : Transmit PHY Device Address
TCL : Internal Transmit System Clock
TCLAV : Transmit Cell Available
TCLK : Transmit Data Transferring Clock
TCOC : Transmit Clock Output Complement
TCOT : Transmit Clock Output True
TDI0-TDI7 : Transmit Data Input from the ATM Layer
TDOC : Transmit Data Output Complement
TDOT : Transmit Data Output True
TENBL_B : Transmit Data Enable
TEST0-TEST2 : Test Mode Pin
TFC : Transmit Reference Clock
TFKC : Transmit Reference Clock Complement
TFKT : Transmit Reference Clock True
TFSS : Transmit Frame Set Signal
TPC : Transmit Parallel Data Clock
TPD0-TPD7 : Transmit Parallel Data
TSOC : Transmit Start Address of ATM Cell
TxFP : Transmit Frame Pulse
UMPSEL : Utopia Multi-PHY Mode Select
VDD : Supply Voltage for Logic Circuit
VDD-RPE : Voltage Supply for Receive PECL Buffer
VDD-CR : Voltage Supply for Clock Recovery Circuit
VDD-CS : Voltage Supply for Clock Synthesis
VDD-SP : Voltage Supply for Serial/Parallel Circuit
VDD-TPE : Voltage Supply for Transmit PECL Buffer
WR_B : Write Select

1. PIN FUNCTIONS

1.1 PMD Interface

(1/2)

Pin name	Pin No.	I/O level	I/O	Function
RDIT	54	P-ECL True(+)	I	Serial receive data input. When PSEL [1:0] is set to 00, the data is sampled on a clock recovered by the internal clock recovery PLL. When PSEL [1:0] is set to 01, the data is sampled on the clock input to RCIT/RCIC.
RDIC	55	P-ECL Complement(-)	I	
RCIT	51	P-ECL True(+)	I	Serial receive clock input (155.52 MHz). When PSEL [1:0] is set to 01, the input is used as a receive clock.
RCIC	52	P-ECL Complement(-)	I	
TDOT	47	P-ECL True(+)	O	Serial transmit data output. The data is output in sync with the rising edge of the serial clock TCOT.
TDOC	48	P-ECL Complement(-)	O	
TCOT	43	P-ECL True(+)	O	Serial transmit clock output (155.52 MHz). When PSEL [1:0] is set to 00, the clock generated by the internal synthesizer PLL is output as the transmit clock. When PSEL [1:0] is set to 01, the clock supplied to TFKT/TFKC is output. Depending on the mode selected, the transmit data may be latched by the receive clock for output. Even in such a case, this pin outputs the clock of the internal synthesizer or the clock input to the TFKT/TFKC pin in accordance with the setting of the PSEL[1:0] pins. It does not output the receive recovery clock.
TCOC	44	P-ECL Complement(-)	O	
TFKT	40	P-ECL True(+)	I	Serial transmit clock input (155.52 MHz). When PSEL [1:0] is set to 01, the input is used as the transmit clock.
TFKC	41	P-ECL Complement(-)	I	
RPD0-RPD7	61-68	TTL	I	Parallel receive data input. When PSEL [1:0] is set to 1X, these pins input receive data. The data is sampled in sync with the rising edge of parallel receive clock RPC.
RPC	59	TTL	I	Parallel receive clock input (19.44 MHz). When PSEL [1:0] is set to 1X to select parallel mode, this pin inputs a 19.44 MHz receive clock.
TPD0-TPD7	17-24	TTL	O	Parallel transmit data output. When PSEL [1:0] is set to 1X to select parallel mode, these pins output transmit data in sync with the rising edge of PC.
TPC	25	TTL	O	Parallel transmit clock output. When PSEL [1:0] is set to 1X, this pin outputs the clock (19.44 MHz) supplied to TFC.

(2/3)

Pin name	Pin No.	I/O level	I/O	Function
TFC	26	TTL	I	Parallel transmit clock input. When PSEL [1:0] is set to 1X to select parallel mode, this pin inputs a parallel transmit clock of 19.44 MHz. If the TxCL bits [1:0] of the MDR1 register are set to 10 in the serial mode with PSEL[1:0] = "00", input the 19.44 MHz source clock of the internal clock synthesizer PLL.
REFCLK	28	TTL	I	Reference clock input. This pin supplies a system clock of 19.44 MHz to the internal clock recovery/synthesizer. Always input this clock.
PSEL0, PSEL1	69, 70	TTL	I	PMD interface mode select input. These pins select the interface mode of the PMD layer to be used. PSEL [1:0] = 00 :Serial mode. The clock generated by the internal clock recovery/synthesizer PLL is used for transmission and reception. PSEL [1:0] = 01 :Serial mode. The clock input of the external RCIT/RCIC and TFKT/TFKC is used for transmission and reception. PSEL [1:0] = 1x:Parallel mode. The clock input of RPC and TFC is used.
AIN1	31	Analog	O	This pin connects the loop filter of the internal synthesizer PLL. Leave open.
PMDALM	76	TTL	I	PMD layer alarm signal input. The signal level of this pin is reflected in the state bit of an internal register. The transition of the bit can be used as an interrupt source. The state signal from a peripheral device is input. ★ This signal input can be added as a condition of LOS error detection by setting of PMD bit in IACM register. Refer to **3.5 Alarm Report Pins (PHYALM[2:0], PMDALM)** in **μPD98404 User's Manual (S11821E)**.
PHYALM0-PHYALM2	10-12	TTL	O	PHY layer alarm detection signal output. These pins output a signal indicating that an internally monitored error state (PMDALM, CMDARM, LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, or Path RDI) has been detected. The pins can output an error either singly or in combination. The type of the error to be indicated is selected by setting the internal AMPR, AMR1, and AMR2 registers. For details on use, refer to **3.5 Alarm Report Pins (PHYALM[2:0], PMDALM)** in **μPD98404 User's Manual (S11821E)**.
RxFP	74	TTL	O	Frame pulse output for the receive side (8 kHz). This pin outputs a pulse signal at one-clock intervals in sync with the RCL clock in the frame synchronization state.

(3/3)

Pin name	Pin No.	I/O level	I/O	Function
TxFP	14	TTL	O	Frame pulse signal output for the transmit side (8 kHz). This pin outputs a pulse signal at one-clock intervals in sync with the TCL clock.
TFSS	13	TTL	I	Transmit frame output disable signal input. When the signal is high, the transmit frame output stops. When the signal is low, transmission starts from the beginning of a frame. The μPD98404 samples this signal at the rising edge of the TCL clock. The transmit frame output is resumed at the ninth rising edge of the TCL clock after the rising edge at which the high level of this signal was last detected.
RCL	75	TTL	O	Internal system clock output for the receive side (19.44 MHz). This pin outputs the receive clock divided by 8. The source receive clock depends on the selected mode, which is either the clock generated by the internal clock recovery PLL or the clock supplied from the RCIT/RCIC and RFC pins. Clock output from this pin is stopped while the device is being reset.
TCL	15	TTL	O	Internal system clock output of the transmit side (19.44 MHz). This pin outputs the transmit clock divided by 8. The source transmit clock depends on the selected mode, which is either the clock generated by the internal synthesizer or the clock supplied from the TCIT/TCIC and TFC pins. Clock output from this pin is stopped while the device is being reset.

1.2 ATM layer interface

(1/2)

Pin name	Pin No.	I/O level	I/O	Function
RDO0- RDO7	130-137	TTL	O (2 or 3-state)	Receive data output. These pins form an 8-bit data bus that outputs receive data to an ATM layer device. The data is output in sync with the rising edge of the RCLK clock. These pins operate in two or three states, depending on the UTOPIA interface mode.
RCLK	128	TTL	I	Receive clock input. This pin supplies a clock of up to 40 MHz for receive data transfer.
RSOC	126	TTL	O (2 or 3-state)	Receive cell start position signal output. This pin outputs a signal indicating the position of the first byte of a receive cell. This pin operates in two or three states, depending on the UTOPIA interface mode.
RENBL_B	127	TTL	I	Receive enable signal input. This pin inputs a signal indicating that the ATM layer is ready to receive data.

(2/2)

Pin name	Pin No.	I/O level	I/O	Function
EMPTY_B/ RCLAV	125	TTL	O (2 or 3-state)	Receive FIFO data transfer disable signal output or receive FIFO cell data transfer enable signal output. This pin functions as either EMPTY_B (2-state operation) or RCLAV (3-state operation), depending on the selected mode of the UTOPIA interface. EMPTY_B indicates that the receive FIFO has no receive data bytes to be transferred to the ATM layer. RCLAV indicates that the receive FIFO has data of at least once cell to be transferred to the ATM layer. This pin operates in two or three states, depending on the UTOPIA interface mode.
RADD0- RADD4	138-142	TTL	I	PHY address input for the receive side. In multi-PHY mode, these pins input the address of the PHY layer device to be selected.
TDI0- TDI7	111-118	TTL	I	Transmit data input. These pins form an 8-bit data bus that inputs transmit data. The data is input in sync with the rising edge of the TCLK clock.
TCLK	120	TTL	I	Transmit clock input. This pin inputs a clock of 20 to 40 MHz for transmit data transfer. **Caution The μPD98404 also uses this clock as the system clock of the management interface block. Therefore, always input a clock of 20 MHz or higher.**
TSOC	122	TTL	I	Transmit cell start position input. This pin inputs a signal indicating the position of the first byte of the transmit cell input to the μPD98404.
TENBL_B	121	TTL	I	Transmit enable input. This pin inputs a signal indicating that an ATM layer device is outputting valid transmit data to TDI0 - TDI7.
FULL_B/ TCLAV	123	TTL	O (2 or 3-state)	Transmit FIFO data transfer disable signal output or transmit FIFO cell data transfer enable signal output. This pin functions as either FULL_B (2-state operation) or TCLAV (3-state operation), depending on the selected UTOPIA interface mode. FULL_B indicates that the transmit FIFO has no free area to receive transmit data. TCLAV indicates that the transmit FIFO has a free area of at least one cell for storing transmit data. This pin operates in two or three states, depending on the UTOPIA interface mode.
TADD0- TADD4	103-107	TTL	I	PHY address input for the transmit side. When used in multi-PHY mode, these pins input an address for selecting a PHY layer device.
UMPSEL	85	TTL	I	Multi-PHY mode select signal input. • When the signal is high, multi-PHY mode is selected. • When the signal is low, single PHY mode is selected.

1.3 Management interface

(1/2)

Pin name	Pin No.	I/O level	I/O	Function
MSEL	77	TTL	I	Mode select signal input. The level of input to this pin determines the management interface mode. MSEL = 1: Pin functions RD_B, WR_B, and RDY_B are selected. MSEL = 0: Pin functions DS_B, R/W_B, and ACK_B are selected.
MADD0-MADD6	78-84	TTL	I	Address input. These pins form an address bus to input the address of an internal register of the μPD98404.
MD0-MD7	87-94	TTL	I/O (3-state)	8-bit data bus. These pins form a data bus to read or write data of an internal register of the μPD98404.
CS_B	96	TTL	I	Chip select signal input. When the signal is low, access to an internal register is enabled.
DS_B/ RD_B	97	TTL	I	Data strobe signal input or read signal input. This pin functions as either DS_B or RD_B, depending on the mode selected by the MSEL pin. MSEL = 0: This pin functions as DS_B to input the data strobe signal. MSEL = 1: This pin functions as RD_B to select read access.
R/W_B/ WR_B	98	TTL	I	Read/write signal input or write signal input. This pin functions as either R/W_B or WR_B, depending on the mode selected by the MSEL pin. MSEL = 0: This pin functions as R/W_B that inputs the read/write control signal. High: Read cycle Low: Write cycle MSEL = 1: This pin functions as WR_B that selects write access.
ACK_B/ RDY_B	99	TTL	O (3-state)	Data acknowledge signal output or ready signal output. This pin functions as either ACK_B or RDY_B, depending on the mode selected by the MSEL pin. MSEL = 0 : The pin functions as ACK_B that outputs the data strobe signal. MSEL = 1 : The pin functions as RDY_B that selects read access.
PHINT_B	100	TTL	O	Interrupt signal output. This pin notifies the host that an internal interrupt source has been detected. The pin is active low.

(2/2)

Pin name	Pin No.	I/O level	I/O	Function
RESET_B	101	TTL	I	System reset signal input. The signal initializes the μPD98404. The input signal should be kept low for 1 μs or more. Especially, in case of the power on, above-mentioned pulse width must be kept after the supply voltage reaches equal to or more than 90% at least. When the RESET_B signal is input, the following clock must be input according to the PMD interface mode. Serial mode : TCLK/RCLK clock Parallel mode: TCLK/RCLK and TFC/RPC clocks

1.4 JTAG boundary scan

Pin name	Pin No.	I/O level	I/O	Function
JDI	4	TTL	I	Boundary scan data input. When not being used, this pin should be grounded.
JDO	3	TTL	O (3-state)	Boundary scan data output. When not being used, this pin should be left open.
JCK	2	TTL	I	Boundary scan clock input. When not being used, this pin should be grounded.
JMS	5	TTL	I	Boundary scan mode select signal input. When not being used, this pin should be grounded.
JRST_B	6	TTL	I	Boundary scan reset signal input. When not being used, this pin should be grounded.

Remark Processing of JTAG boundary scan pins not used (during normal operation)
The reason that the JRST_B pin is grounded when it is not used (during normal operation) is to better prevent malfunctioning of the JTAG logic. The JTAG pin may be also processed in either of the following ways:

- Reset the JTAG logic without using the JRST_B pin
  Reset the JTAG logic by using the JMS and JCK pins and keep it in the reset status (the JRST_B pin is pulled up).
  Fix the JMS pin to 1 (pull up) and input 5 clock cycles or more to the JCK pin.

- Reset the JTAG logic by using the JRST_B pin
  Input a low pulse of the same width as RESET_B of the μPD98404 to the JRST_B pin. If both the JMS and JRST_B pins are pulled up and kept high, the JTAG logic is not released from the reset status. Therefore, the normal operation is not affected. Fix the input level of the JDI and JCK pins by pulling them down or up.

1.5 Internal test pins

Pin name	Pin No.	I/O level	I/O	Function
TEST0-TEST2	7-9	TTL	I	These pins are used to test the μPD98404. In normal operation, all these pins should be grounded. TEST [2:0] =000 : Normal operation TEST [2:0] =Other than 000 : Test mode

★

1.6 Power and ground

Pin name	Pin No.	I/O	Function
VDD	1, 27, 36, 60, 73, 95, 108, 119, 129	-	Power supply (+3.3 V ±0.15 V) and ground for the general logic block.
GND	16, 37, 71, 72, 86, 102, 109, 110, 124, 143, 144	-	
VDD-TPE	39, 45, 49	-	Power supply (+3.3 V ±0.15 V) and ground for output PECL I/O. Any noise in this power supply will affect the jitter characteristics. A means of eliminating this noise, such as a filter, is needed.
GND-TPE	42, 46	-	
VDD-RPE	53	-	Power supply (+3.3 V ±0.15 V) and ground for input PECL I/O. Any noise in this power supply will affect the jitter characteristics. A means of eliminating this noise, such as a filter, is needed.
GND-RPE	50, 56	-	
VDD-SP	35	-	Power supply (+3.3 V ±0.15 V) and ground for the serial /parallel block. Any noise in this power supply will affect the jitter characteristics. A means of eliminating this noise, such as a filter, is needed.
GND-SP	38	-	
VDD-CS	32, 33	-	Power supply (+3.3 V ±0.15 V) and ground for the clock synthesizer PLL block. Any noise in this power supply will affect the jitter characteristics. A means of eliminating this noise, such as a filter, is needed.
GND-CS	29, 30, 34	-	
VDD-CR	58	-	Power supply (+3.3 V ±0.15 V) and ground for the clock recovery PLL block. Any noise in this power supply will affect the jitter characteristics. A means of eliminating this noise, such as a filter, is needed.
GND-CR	57	-	

1.7 Recommended connection of unused pins

Pin	Recommended Connection of Unused Pins
Each input pin at level other than P-ECL	Connect to ground (parallel input pin in serial mode) RPD0 through RPD7, RPC, TFC (Multi-PHY pins in single PHY mode) TADD0 to TADD4, RADD0 through RADD4 (others) TFSS (essential)
Each input pin at P-ECL level	Pull up True(+) pins (TFKT, RCIT, RDIT) to 3.3 V. Connect Complement(–) pins (TFKC, RCIC, RDIC) to ground.
Output pin	Leave open. (Parallel input pins in serial mode) TPD0 to TPD7 TPC (others) TxFP, RxFP, TCL, RCL
Output pin at P-ECL level	Leave open. TDOT, TDOC, TCOT, TCOC
AIN1	Leave Open. Because noise on this pin affects the characteristics of the internal PLL, do not wire a clock line in the vicinity.

2. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Condition	Ratings	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input/output voltage	V_{I1}/V_{O1}	Pin other than P-ECL, analog level	–0.5 to +6.6 or V_{DD} +3.0	V
	V_{I2}/V_{O2}	P-ECL, analog level	–0.5 to +4.6 or V_{DD} +0.5	V
Operating temperature	T_A		–45 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If even one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the values at which the product can be used without physical damage. Be sure not to exceed or fall below these values when using the product.

Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	Frequency: = 1 MHz		6	10	pF
Output capacitance	C_O	Frequency: = 1 MHz		6	10	pF
Input/output capacitance	C_{IO}	Frequency: = 1 MHz		6	10	pF

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Power supply voltage	V_{DD}		3.15	3.3	3.45	V
Operating temperature range	T_A		–40		+85	°C
Low-level input voltage	V_{IL1}	Pin other than P-ECL level pin	0		0.8	V
	V_{IL2}	P-ECL level pin	V_{DD} – 2.82		V_{DD} – 1.50	V
High-level input voltage	V_{IH1}	Pin other than P-ECL level pin	2.2		5.25	V
	V_{IH2}	P-ECL level pin	V_{DD} – 1.49		V_{DD} – 0.40	V
Differential input voltage	V_{IDIFF2}		300		1900	mV

Remark P-ECL level pins: RDIT, RDIC, RCIT, RDIC, TDOT, TDOC, TCOT, TCOC, TFKT, TFKC
Analog pins : AIN1

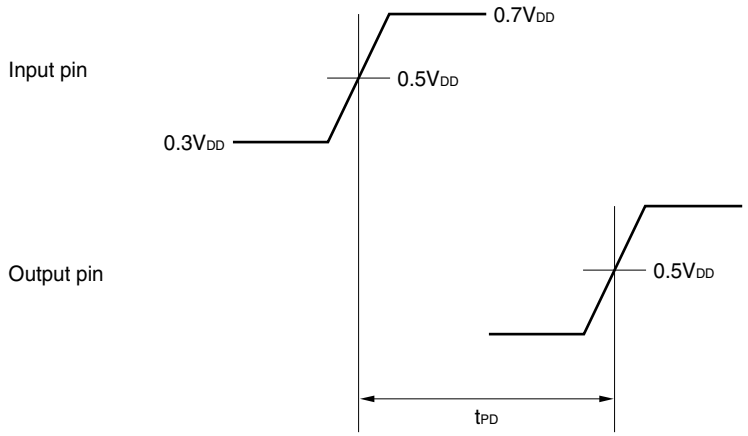
DC Characteristics (V_{DD} = 3.3 ±0.15 V, T_A = –40 to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Off-state output current	I_{OZ}	V_I = V_{DD} or GND			±10	μA
Input leakage current	I_{LI1}	V_I = V_{DD} or GND Pin other than P-ECL level pin			±10	μA
	I_{LI2}	P-ECL level pin			±10	μA
Low-level output voltage	V_{OL1}	I_{OL} = +8mA, V_{DD} = 3.3 V Pin other than P-ECL level pin			0.4	V
	V_{OL2}	R_L = 50 Ω, V_T = V_{DD} – 2 V P-ECL level pin	V_{DD} – 2.175	V_{DD} – 1.975	V_{DD} – 1.755	V
High-level output voltage	V_{OH1}	I_{OH} = –8 mA, V_{DD} = 3.3 V Pin other than P-ECL level pin	2.4			V
	V_{OH2}	R_L = 50 Ω, V_T = V_{DD} – 2 V P-ECL level pin	V_{DD} – 1.14	V_{DD} – 0.92	V_{DD} – 0.69	V
Power supply current	I_{DD}	During normal operation		200	450	mA

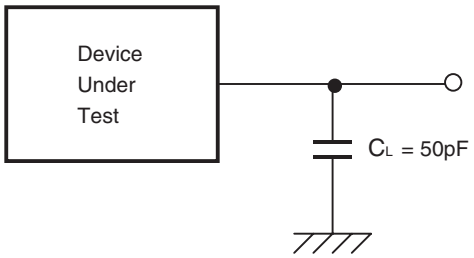
AC Characteristics (V_{DD} = 3.3 ±0.15 V, T_A = –40 to +85°C)

AC Test Condition

The propagation delay time is defined as shown below.



AC Testing Load Circuit



Management Interface

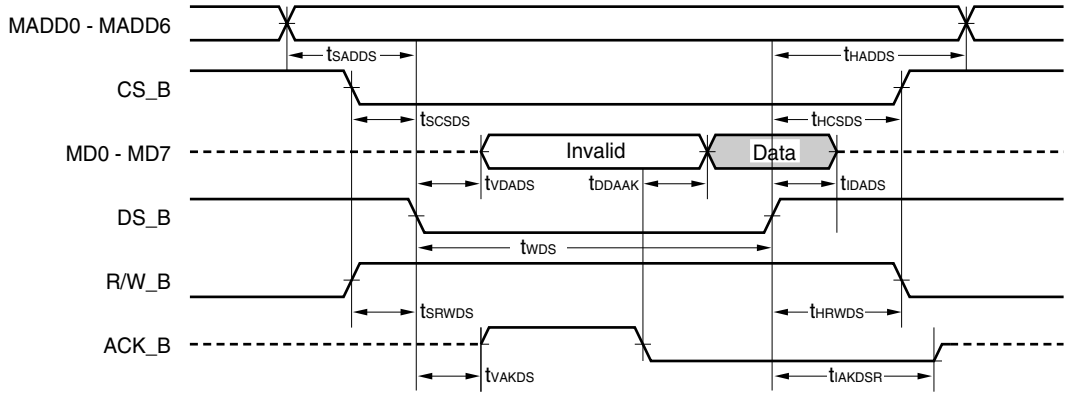
(a) Internal register read

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to DS_B↓ [RD_B↓])	t_{SADDS}		10			ns
CS_B setup time (to DS_B↓ [RD_B↓])	t_{SCSDS}		5		$9 \times t_{CYTK}$	ns
R/W_B[WR_B] setup time (to DS_B↓ [RD_B↓])	t_{SRWDS}		5			ns
Address hold time (to DS_B↑ [RD_B↑])	t_{HADDS}		4			ns
CS_B hold time (to DS_B↑ [RD_B↑])	t_{HCSDS}		0			ns
R/W_B [WR_B] hold time (to DS_B↑ [RD_B↑])	t_{HRWDS}		4			ns
DS_B↓ [RD_B↓] → ACK_B [RDY_B] output delay time	t_{VAKDS}	Load capacity = 50 pF			15	ns
DS_B↓ [RD_B↓] → data output delay time	t_{VDADS}	Load capacity = 50 pF			20	ns
DS_B↑ [RD_B↑] → ACK_B [RDY_B] float delay time	t_{IAKDSR}	Load capacity = 50 pF	5		30	ns
DS_B↑ [RD_B↑] → data float delay time	t_{IDADS}	Load capacity = 50 pF	15		45	ns
ACK↓ → data output delay time	t_{DDAAK}	Load capacity = 50 pF			10	ns
DS_B[RD_B] pulse width[Note]	t_{WDS}		50			ns
DS_B↑[RD_B↑]→DS_B↓[RD_B↓]↓ recovery time	t_{DSINT}		$4 \times t_{CYTK}$			ns

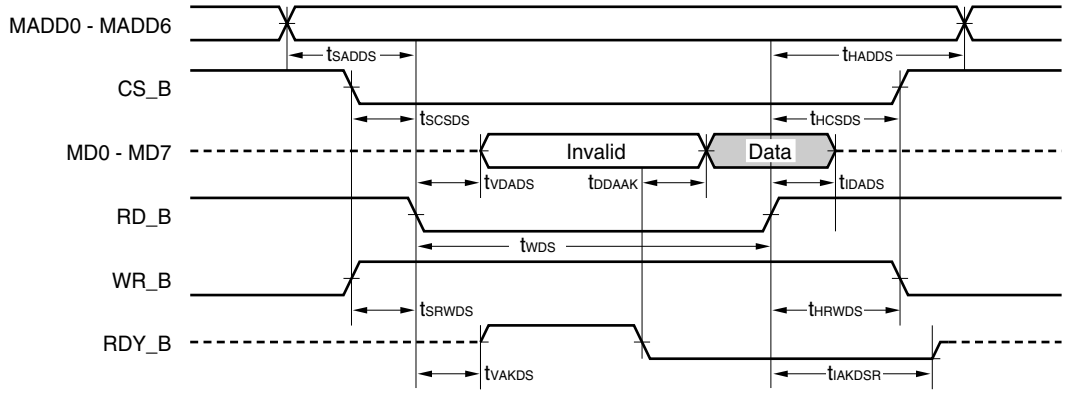
Note t_{WDS} defines the time during which the μPD98404 can recognize DS_B [RD_B] as a low level, and does not define the pulse width of DS_B [RD_B] with which data can be accurately read.
The time required for the μPD98404 to make ACK_B [RDY_B] low after DS_B [RD_B] has gone low differs depending on the register to be accessed. Make DS_B [RD_B] high after confirming that ACK_B [RDY_B].
The time required for the μPD98404 to make ACK_B [RDY_B] low after DS_B [RD_B] has gone low is “4 x TCLK clock cycle (t_{CYTK})” at best. So that any register can be read without using ACK_B [RDY_B], widen the pulse width of DS_B [RD_B] to at least to “4 x TCLK clock cycle”.

Remark t_{CYTK} is the cycle of the TCLK clock.

(i) When MSEL = "0" (Motorola compatible)



(ii) When MSEL = "1" (Intel compatible)



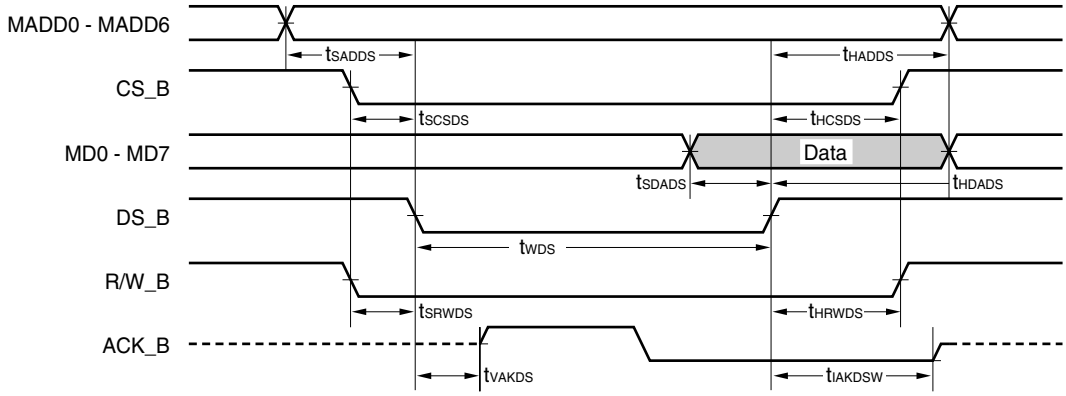
(b) Internal register write

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to DS_B↓ [WR_B↓])	t_{SADDS}		10			ns
CS_B setup time (to DS_B↓ [WR_B↓])	t_{SCSDS}		5		$9 \times t_{CYTK}$	ns
R/W_B[RD_B] setup time (to DS_B↓ [WR_B↓])	t_{SRWDS}		5			ns
Data setup time (to DS_B↑ [WR_B↑])	t_{SDADS}		15			ns
Address hold time (to DS_B↑ [WR_B↑])	t_{HADDS}		4			ns
CS_B hold time (to DS_B↑ [WR_B↑])	t_{HCSDS}		0			ns
R/W_B [WR_B] hold time (to DS_B↑ [WR_B↑])	t_{HRWDS}		4			ns
Data hold time (to DS_B↑ [WR_B↑])	t_{HDADS}		4			ns
DS_B↓ [WR_B↓] → ACK_B [RDY_B] output delay time	t_{VAKDS}	Load capacity = 50 pF			15	ns
DS_B↑ [WR_B↑] → ACK_B [RDY_B] float delay time	t_{IAKDSW}	Load capacity = 50 pF			10	ns
DS_B [WR_B] pulse width[Note]	t_{WDS}		50			ns
DS_B↑[WR_B↑]→DS_B↓[WR_B↓]↓ recovery time	t_{DSINT}		$4 \times t_{CYTK}$			ns

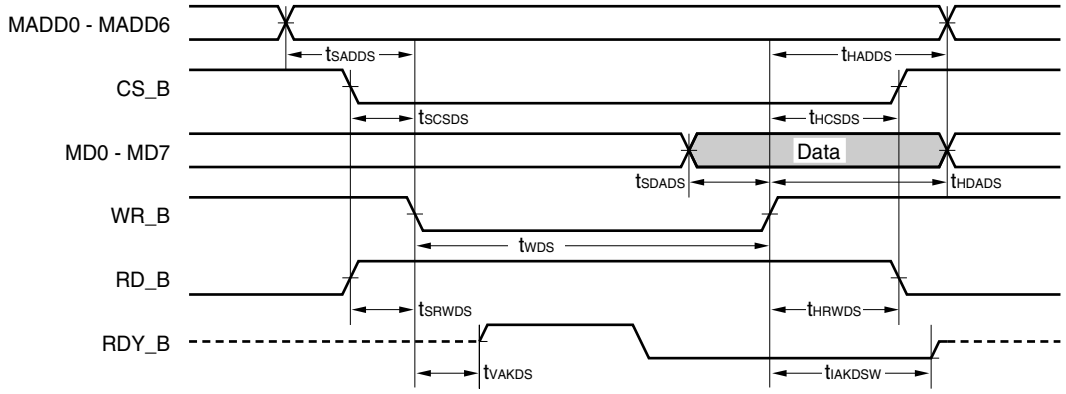
Note t_{WDS} defines the time during which the μPD98404 can recognize DS_B [WR_B] as a low level, and does not define the pulse width of DS_B [WR_B] with which data can be accurately read.
The time required for the μPD98404 to make ACK_B [RDY_B] low after DS_B [WR_B] has gone low differs depending on the register to be accessed. Make DS_B [WR_B] high after confirming that ACK_B [RDY_B] has gone low.
The time required for the μPD98404 to make ACK_B [RDY_B] low after DS_B [WR_B] has gone low is “4 x TCLK clock cycle (t_{CYTK})” at best. So that any register can be write without using ACK_B [RDY_B], widen the pulse width of DS_B [WR_B] to at least to “4 x TCLK clock cycle”.

Remark t_{CYTK} is the cycle of the TCLK clock.

(i) When MSEL = "0" (Motorola compatible)



(ii) When MSEL = "1" (Intel compatible)

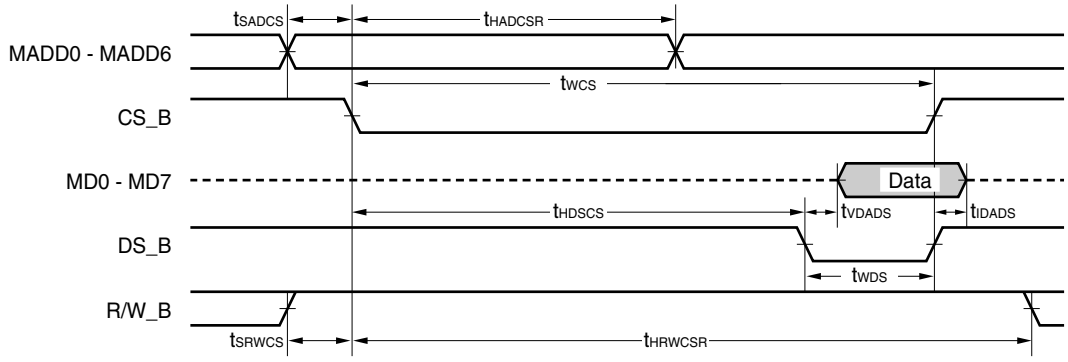


(c) Internal register read/write (NEASCOT-S15 connection mode, MSEL = "0")

(i) Read timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to CS_B↓)	t_{SADCS}		10			ns
R/W_B setup time (to CS_B↓)	t_{SRWCS}		10			ns
Address hold time (to CS_B↓)	t_{HADCSR}		$5\times t_{CYTK}+10$			ns
R/W_B hold time (to CS_B↓)	t_{HRWCSR}		$15\times t_{CYTK}+10$			ns
DS_B hold time (to CS_B↓)	t_{HDSCS}		$15\times t_{CYTK}+10$			ns
DS_B↓ → data output delay time	t_{VDADS}	Load capacity = 50 pF			$30 + t_{CYTK}$	ns
DS_B↑ → data float delay time	t_{IDADS}	Load capacity = 50 pF	15		45	ns
CS_B pulse width	t_{WCS}		$15 \times t_{CYTK}$			ns
DS_B pulse width	t_{WDS}		$4 \times t_{CYTK}$			ns

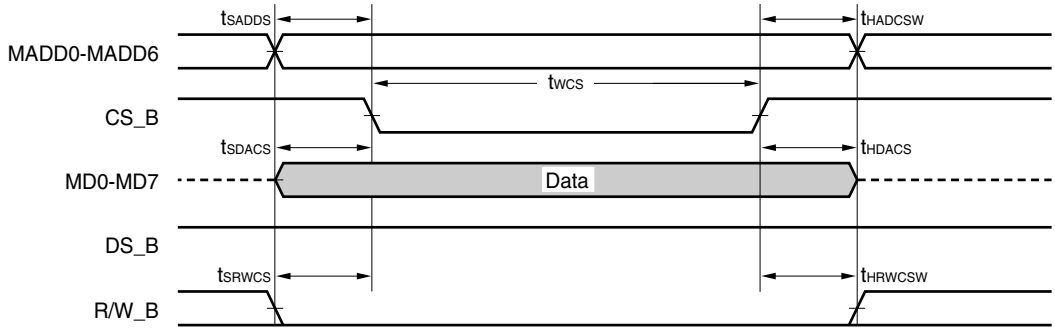
Remark t_{CYTK} is the cycle of the TCLK clock.



(ii) Write timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to CS_B↓)	t_{SADCS}		10			ns
R/W_B setup time (to CS_B↓)	t_{SRWCS}		10			ns
Data setup time (to CS_B↓)	t_{SDACS}		10			ns
Address hold time (to CS_B↑)	t_{HADCSW}		10			ns
R/W_B hold time (to CS_B↑)	t_{HRWCSW}		10			ns
Data hold time (to CS_B↑)	t_{HDACS}		10			ns
CS_B pulse width	t_{WCS}		$4 \times t_{CYTK}$			ns

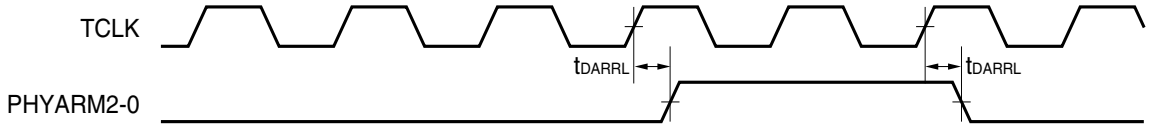
Remark t_{CYTK} is the cycle of the TCLK clock.



Caution If the device is reset via software by setting the CMR2 register, do not read or write all the registers for the duration of at least "20 x TCLK clock cycle (t_{CYTK})" from that write cycle. Otherwise, the registers may not be read or written correctly.

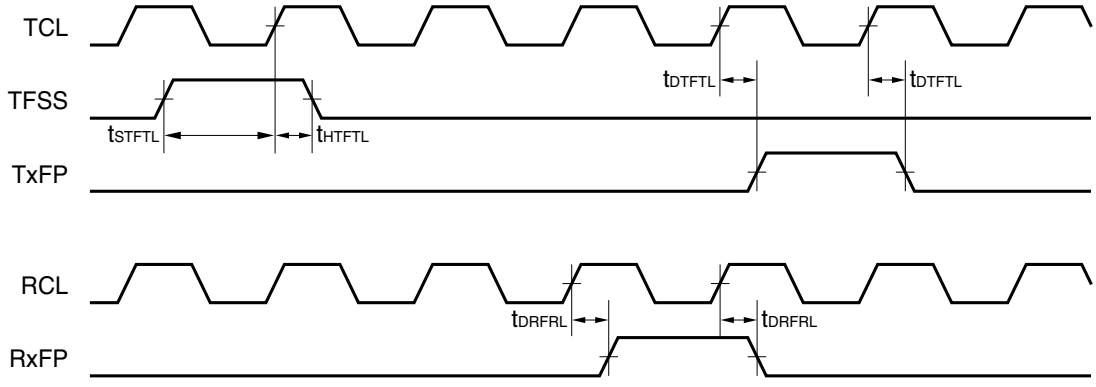
OAM interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCLK↑ → PHYARM2-0 delay time	t_{DARRL}	Load capacity = 50 pF			25	ns



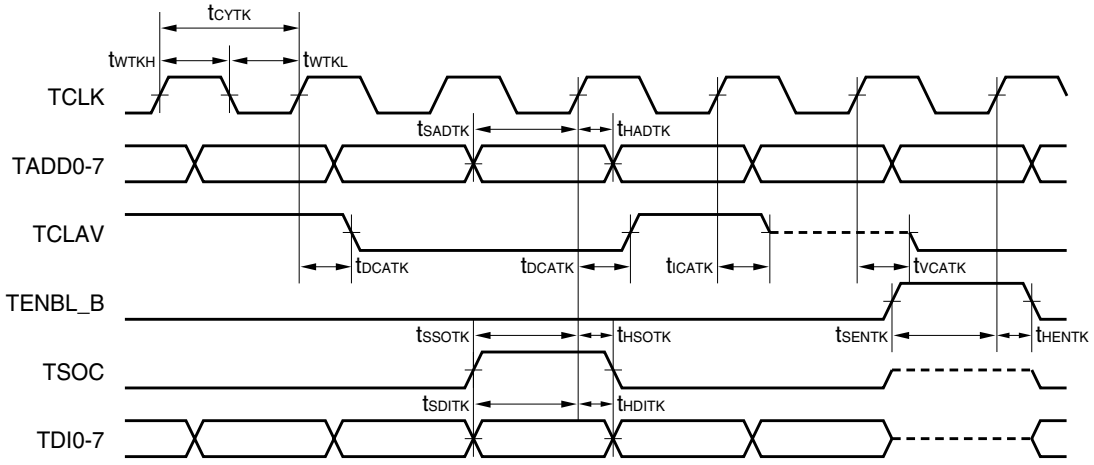
Control signal interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TFSS setup time (to TCL↑)	t_{STFTL}		20			ns
TFSS hold time (to TCL↑)	t_{HTFTL}		5			ns
TCL↑ → TxFP delay time	t_{DTFTL}	Load capacity = 50 pF			25	ns
RCL↑ → RxFP delay time	t_{DRFRL}	Load capacity = 50 pF			25	ns



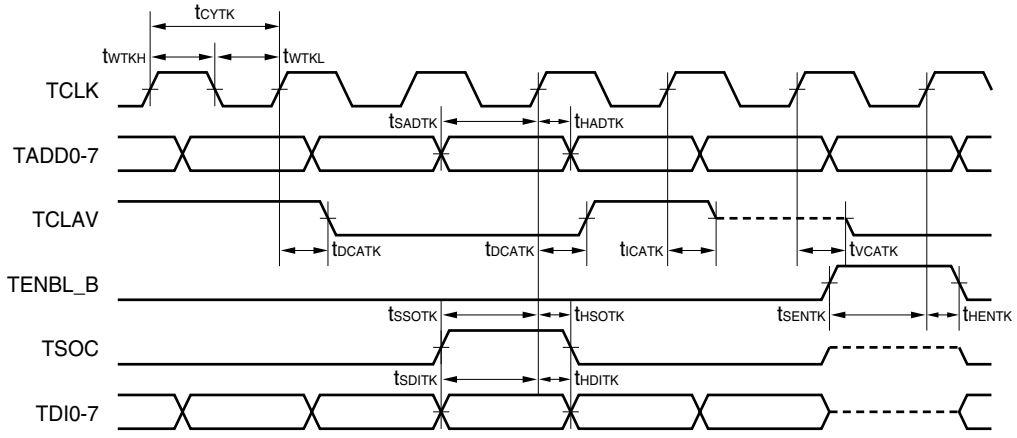
UTOPIA interface (transmit side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCLK cycle time	t_{CYTK}		25		50	ns
TCLK high level width	t_{WTKH}		0.4 × t_{CYTK}		0.6 × t_{CYTK}	ns
TCLK low level width	t_{WTKL}		0.4 × t_{CYTK}		0.6 × t_{CYTK}	ns
TCLK↑ → TCLAV↑↓ delay time	t_{DCATK}	Load capacity = 50 pF	1		19	ns
TCLK↑ → TCLAV output delay time	t_{VCATK}	Load capacity = 50 pF	1		19	ns
TCLK↑ → TCLAV data float delay time	t_{ICATK}	Load capacity = 50 pF	1		25	ns
TDI0-7 setup time (to TCLK↑)	t_{SDITK}		4			ns
TDI0-7 hold time (to TCLK↑)	t_{HDITK}		1			ns
TSOC setup time (to TCLK↑)	t_{SSOTK}		4			ns
TSOC hold time (to TCLK↑)	t_{HSOTK}		1			ns
TADD0-7 setup time (to TCLK↑)	t_{SADTK}		4			ns
TADD0-7 hold time (to TCLK↑)	t_{HADTK}		1			ns
TENBL_B setup time (to TCLK↑)	t_{SENTK}		4			ns
TENBL_B hold time (to TCLK↑)	t_{HENTK}		1			ns



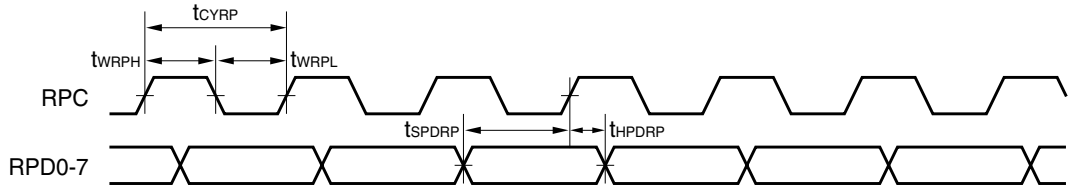
UTOPIA interface (receive side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RCLK cycle time	t_{CYRK}		25			ns
RCLK high level width	t_{WRKH}		0.4 × t_{CYRK}		0.6 × t_{CYRK}	ns
RCLK low level width	t_{WRKL}		0.4 × t_{CYRK}		0.6 × t_{CYRK}	ns
RCLK↑ → RCLAV↑↓ delay time	t_{DCARK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RCLAV output delay time	t_{VCARK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RCLAV data float delay time	t_{ICARK}	Load capacity = 50 pF	1		25	ns
RCLK↑ → RDO0-7↑↓ delay time	t_{DDORK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RDO0-7 output delay time	t_{VDORK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RDO0-7 data float delay time	t_{IDORK}	Load capacity = 50 pF	1		25	ns
RCLK↑ → RSOC↑↓ delay time	t_{DSORK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RSOC output delay time	t_{VSORK}	Load capacity = 50 pF	1		19	ns
RCLK↑ → RSOC data float delay time	t_{ISORK}	Load capacity = 50 pF	1		25	ns
RADD0-7 setup time (to RCLK↑)	t_{SADRK}		4			ns
RADD0-7 hold time (to RCLK↑)	t_{HADRK}		1			ns
RENBL_B setup time (to RCLK↑)	t_{SENRK}		4			ns
RENBL_B hold time (to RCLK↑)	t_{HENRK}		1			ns



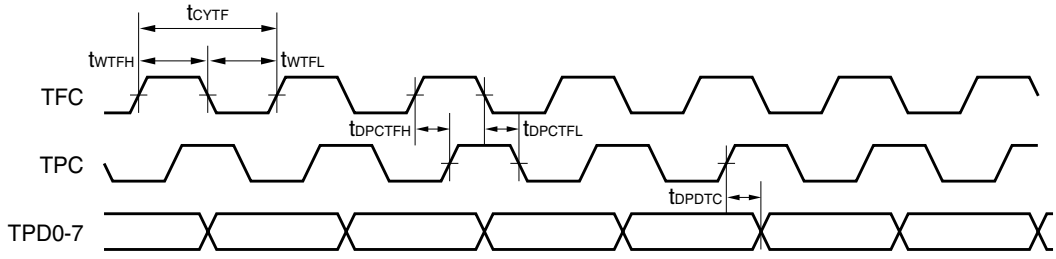
PMD parallel interface (receive side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RPC cycle time	t_{CYRP}		50			ns
RPC high level width	t_{WRPH}		0.4 × t_{CYRP}		0.6 × t_{CYRP}	ns
RPC low level width	t_{WRPL}		0.4 × t_{CYRP}		0.6 × t_{CYRP}	ns
RPD0 - RPD7 setup time (to RPC↑)	t_{SPDRP}		10			ns
RPD0 - RPD7 hold time (to RPC↑)	t_{HPDRP}		5			ns



PMD parallel interface (transmit side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TFC cycle time	t_{CYTF}		50			ns
TFC high level width	t_{WTFH}		0.4 × t_{CYTF}		0.6 × t_{CYTF}	ns
TFC low level width	t_{WTFL}		0.4 × t_{CYTF}		0.6 × t_{CYTF}	ns
TFC↑ → TPC↑ delay time	t_{DPCTFH}	Load capacity = 50 pF			25	ns
TFC↓ → TPC↓ delay time	t_{DPCTFL}	Load capacity = 50 pF			25	ns
TPC↑ → TPD0-TPD7 delay time	t_{DPDTC}	Load capacity = 50 pF	–5		+5	ns



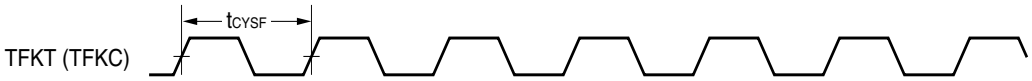
PMD serial interface (transmit side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REFCLK cycle time[Note]	t_{CYRF}		−20ppm	51.4403	+20ppm	ns
REFCLK high level width	t_{WRFH}		0.4 × t_{CYRF}		0.6 × t_{CYRF}	ns
REFCLK low level width	t_{WRFL}		0.4 × t_{CYRF}		0.6 × t_{CYRF}	ns
TFKT(C) cycle time	t_{CYSF}		−0.005UI	6.43	+0.005UI	ns

Caution To get the TCL clock which is a jitter below 0.01UI, the basis signal which has at least equal to or more than 40 ppm precision must be inputted.

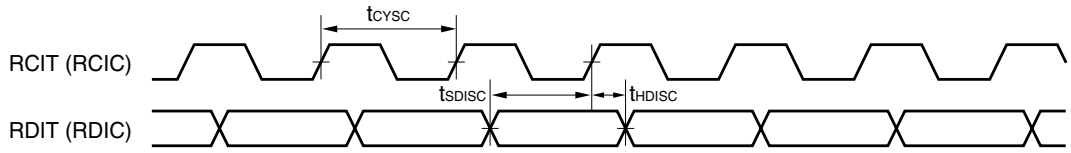
(i) When using a clock synthesizer

(ii) When using an external serial clock



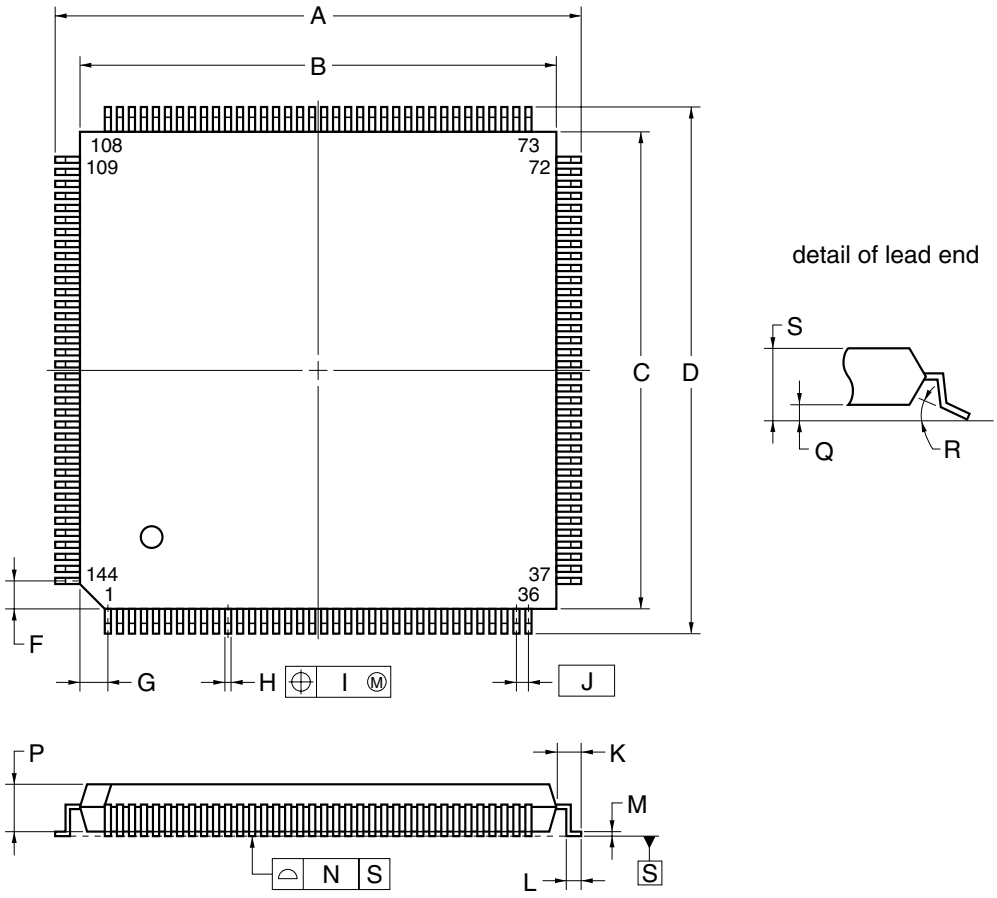
PMD serial interface (receive side)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RCIT(RCIC) cycle time	t_{CYSC}		−0.005UI	6.43	+0.005UI	ns
RDIT(RCIC) setup time	t_{SDISC}		3			ns
RDIT(RCIC) hold time	t_{HDISC}		1			ns



3. PACKAGE DRAWING

144 PIN PLASTIC QFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.3
B	20.0±0.2
C	20.0±0.2
D	22.0±0.3
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	2.7
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.

S144GJ-50-JEU, KEU-1

4. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Surface Mount Type Soldering Conditions

• μPD98404GJ-KEU: 144-pin plastic QFP (fine pitch) (20 × 20)

Soldering method	Soldering conditions	Recommended soldering code
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-203-2
★ VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-203-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

NEASCOT-P30, NEASCOT-S40C, and NEASCOT-X15 are trademarks of NEC Corporation.

- **The information in this document is current as of April, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4