

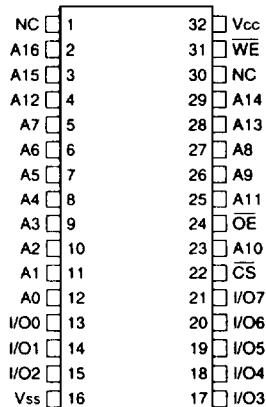


128Kx8 CMOS MONOLITHIC EEPROM

PRELIMINARY*

FIG. 1

PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A ₀₋₁₆	Address Inputs
I/O ₀₋₇	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{cc}	+5.0V Power
V _{ss}	Ground

FEATURES

- Read Access Times of 150, 200, 250 and 300ns
- JEDEC Approved 32 Lead Ceramic SOJ (Package 101)
- Full Military, Industrial, and Commercial Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation:
300µA Standby Typical/80mA Operating
- Automatic Page Write Operation
 - Internal Address and Data Latches for 128 Bytes
 - Internal Control Timer
- Page Write Cycle Time 10mS Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

WHMES023



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T _A	-55 to +125	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Signal Voltage Any Pin	V _G	-0.6 to +6.25	V
Voltage on \overline{OE} and A9		-0.6 to +13.5	V

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

(T_A = 0V, f = 1MHz)

Parameter	Sym	Condition	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1MHz	20	pF
Output Capacitance	C _{OUT}	V _{IO} = 0V, f = 1MHz	20	pF

This parameter is guaranteed by design but not tested.

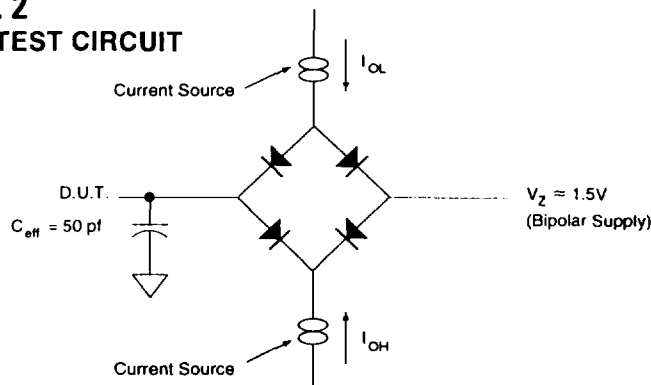
DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions			Unit
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10	μA
Dynamic Supply Current	I _{CC}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		80	mA
Standby Current	I _{SB}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		0.625	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5V		.45	V
Output High Voltage	V _{OH}	I _{OH} = -400μA, V _{CC} = 4.5V	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

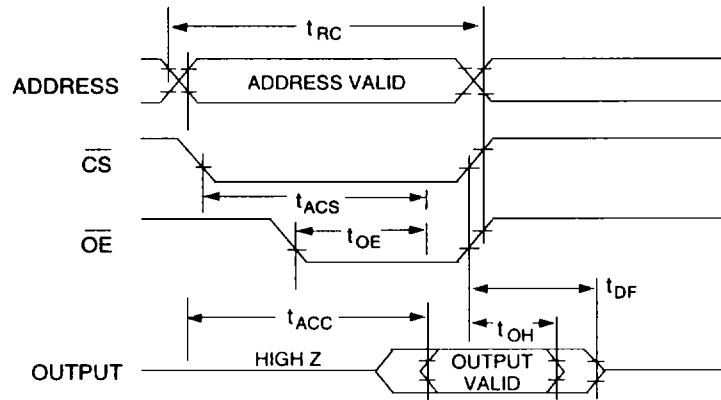
V₂ is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V₂ is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



READ

Figure 3 shows Read cycle waveforms. A read cycle begins with selection address, chip select and output enable. Chip select is accomplished by placing the CS line low. Output enable is done by placing the OE line low. The memory places the selected data byte on I/O0 through I/O7 after the access time. The output of the memory is placed in a high impedance state shortly after either the OE line or CS line is returned to a high level.

FIG. 3 READ WAVEFORMS



NOTE: OE may be delayed up to tACS-tOE after the falling edge of CS without impact on tOE or by tACC-tOE after an address change without impact on tACC.

AC READ CHARACTERISTICS (SEE FIGURE 3) (VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Table with 10 columns: Parameter, Symbol, -150 (Min, Max), -200 (Min, Max), -250 (Min, Max), -300 (Min, Max), Unit. Rows include Read Cycle Time, Address Access Time, Chip Select Access Time, Output Hold from Address Change, Output Enable to Output Valid, and Chip Select or Output Enable to High Z Output.



WRITE

Write operations are initiated when both \overline{CS} and \overline{WE} are low and \overline{OE} is high. The EEPROM devices support both a \overline{CS} and \overline{WE} controlled write cycle. The address is latched by the falling edge of either \overline{CS} or \overline{WE} , whichever occurs last.

The data is latched internally by the rising edge of either \overline{CS} or \overline{WE} , whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the \overline{CS} line low. Write enable consists of setting the \overline{WE} line low. The write cycle begins when the last of either \overline{CS} or \overline{WE} goes low.

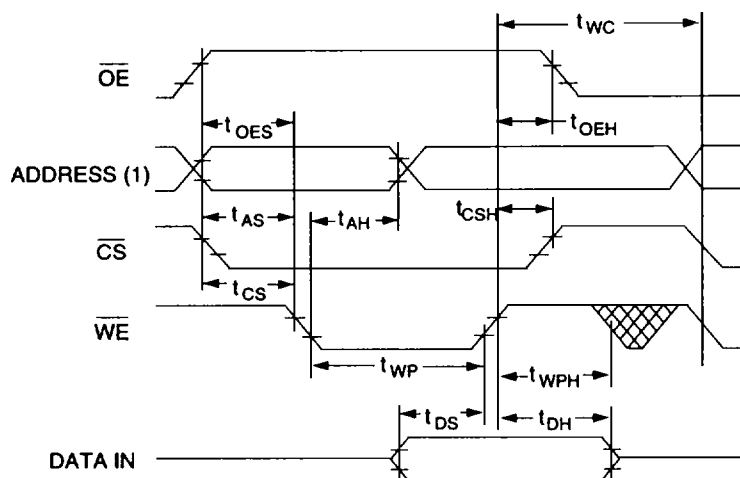
The \overline{WE} line transition from high to low also initiates an internal 150 μ Sec delay timer to permit page mode operation. Each subsequent \overline{WE} transition from high to low that occurs before the completion of the 150 μ Sec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS
(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol			Unit
		Min	Max	
Write Cycle Time, TYP = 6mS	twc		10	mS
Address Set-up Time	tAS	10		nS
Write Pulse Width (\overline{WE} or \overline{CS})	tWP	150		nS
Chip Select Set-up Time	tCS	0		nS
Address Hold Time	tAH	100		nS
Data Hold Time	tDH	10		nS
Chip Select Hold Time	tCH	0		nS
Data Set-up Time	tDS	100		nS
Output Enable Set-up Time	tOES	10		nS
Output Enable Hold Time	tOEH	10		nS
Write Pulse Width High	tWPH	50		nS

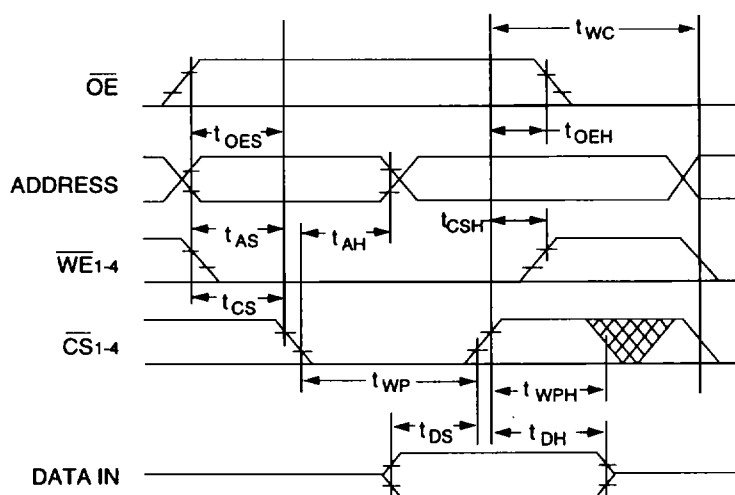


FIG. 4
WRITE WAVEFORMS
WE CONTROLLED



NOTE:
1. Decoded Address Lines must be valid for the duration of the write.

FIG. 5
WRITE WAVEFORMS
CS CONTROLLED





DATA POLLING

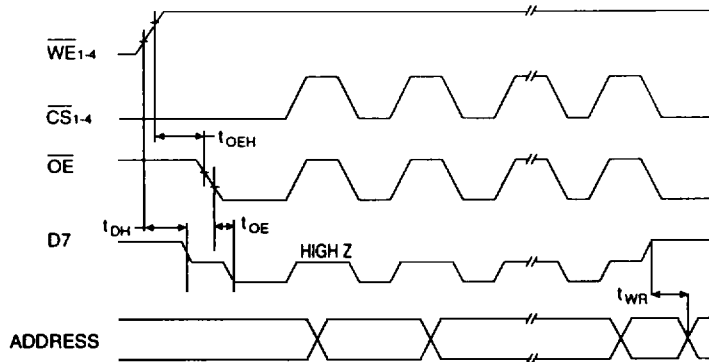
The WME128K8-XDEX offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on I/O7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t _{DH}	10		nS
\overline{OE} Hold Time	t _{OEH}	10		nS
\overline{OE} To Output Valid	t _{OE}		100	nS
Write Recovery Time	t _{WR}	0		nS

FIG. 6
DATA POLLING
WAVEFORMS





PAGE WRITE OPERATION

The WME128K8-XDEX has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µS or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µS time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Page Mode Write Characteristics	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6mS	t _{wc}	10		mS
Address Set-up Time	t _{as}	10		nS
Address Hold Time (1)	t _{ah}	100		nS
Data Set-up Time	t _{ds}	100		nS
Data Hold Time	t _{dh}	10		nS
Write Pulse Width	t _{wp}	150		nS
Byte Load Cycle Time	t _{bLC}		150	µS
Write Pulse Width High	t _{wph}	50		nS

1. Page address must remain valid for duration of write cycle.

FIG. 7
PAGE MODE
WRITE WAVEFORMS

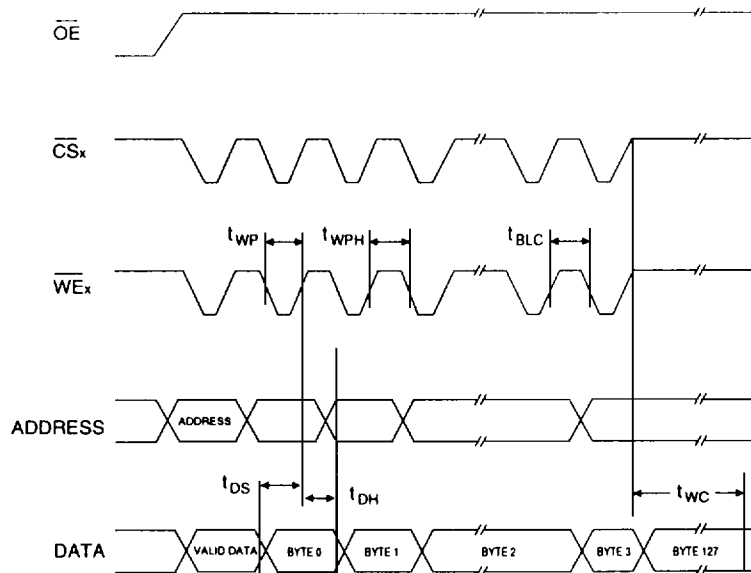
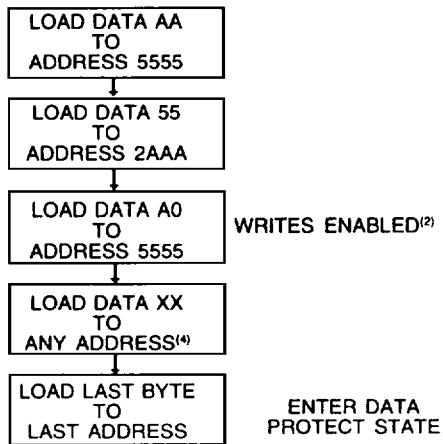




FIG. 8
SOFTWARE DATA PROTECTION
ENABLE ALGORITHM ⁽¹⁾

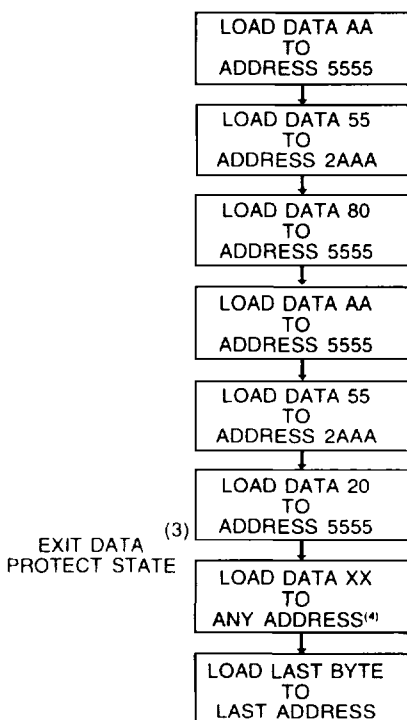


NOTES:

1. Data Format: I/O7-I/O0 (Hex);
Address Format: A16 -A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.



FIG. 9
SOFTWARE BLOCK DATA
PROTECTION DISABLE ALGORITHM



NOTES:

1. Data Format: I/O₇-I/O₀ (Hex); Address Format: A₁₆-A₀ (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WME128K8-XDEX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

The software write protection guards against inadvertent writes during power transitions or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WME128K8-XDEX. These are included to improve reliability during normal operation:

a) Vcc power on delay

As Vcc climbs past 3.8V typical the device will wait 5mSec typical before allowing write cycles

b) Vcc sense

While below 3.8V typical write cycles are inhibited.

c) Write inhibiting

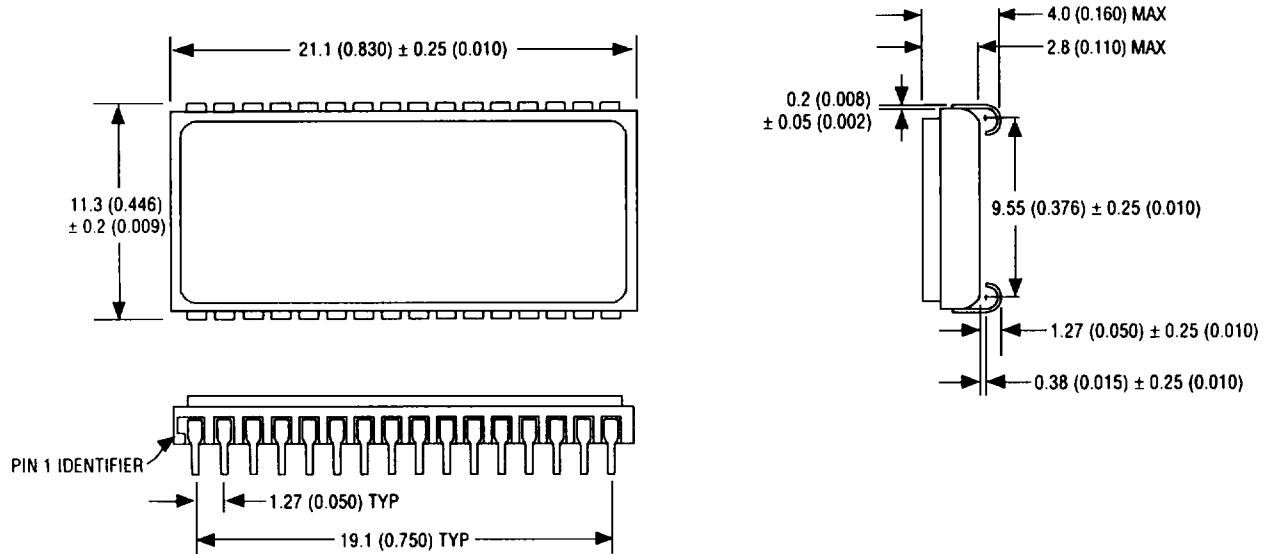
Holding \overline{OE} low and either \overline{CS} or \overline{WE} high inhibits write cycles.

d) Noise filter

Pulses of <15nS (typ) on \overline{WE} or \overline{CS} will not initiate a write cycle.



FIG. 10
PACKAGE 101



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M E 128K8 X - XXX X X

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0 to +70°C

PACKAGE TYPE:

DE = 32 Lead CSOJ (Package 101)

ACCESS TIME in nS

IMPROVEMENT MARK

ORGANIZATION 128K x 8

EEPROM

MONOLITHIC

WHITE MICROELECTRONICS