SONY

CXB1114Q/Q-Y

T-68-11-51

4-bit Demultiplexer

Description

The CXB1114Q is an ultra High speed monolithic ECL Demultiplexer which functions as a 4-bit Serial to Parallel Converter.

The IC converts serial data into 4-bit demultiplexed parallel data. Load Start (ST) input, which starts the demultiplexing, has to be maintained High for at least 3 clock periods. Trigger (TRIG) pulse is provided for an external circuit to fetch the output data.

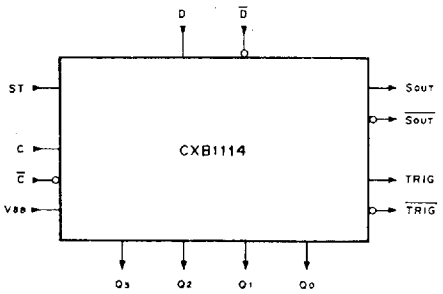
Features

- Typical clock rate up to 2.1GHz
- Differential Clock and Data inputs
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

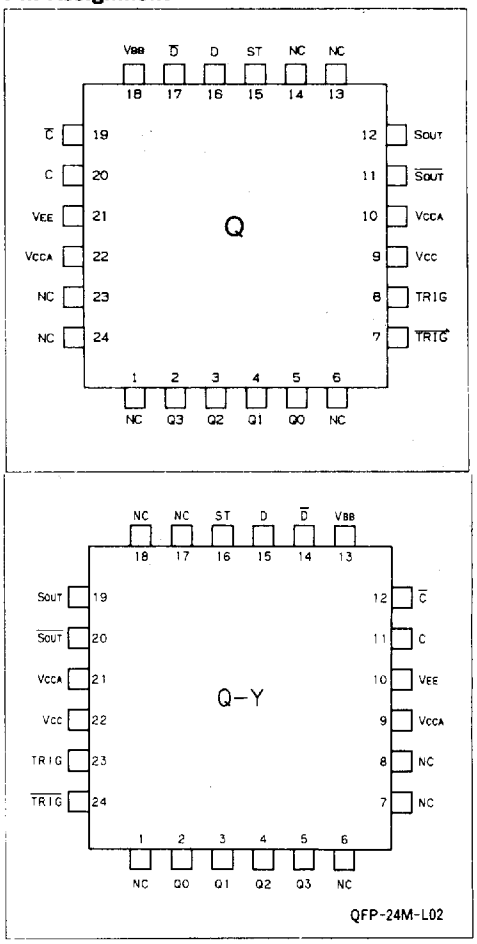
Pin Names

D, $\overline{D}$	Serial Data inputs
ST	Load Start input
C, $\overline{C}$	Clock inputs (positive edge trigger)
Qn	Demultiplexed parallel data outputs
TRIG, $\overline{TRIG}$	Trigger pulse outputs
SOUT, $\overline{SOUT}$	Serial data outputs
V_{BB}	Reference voltage output
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment



Truth Table

ST	C	Function
L	∫	Serial data input, porallel data out
H	∫	Initialize (3 clock period min.)

Note: H; HIGH voltage level
L; LOW voltage level
∫; Positive transition edge

T-68-11-51

DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−297	−218	−152	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

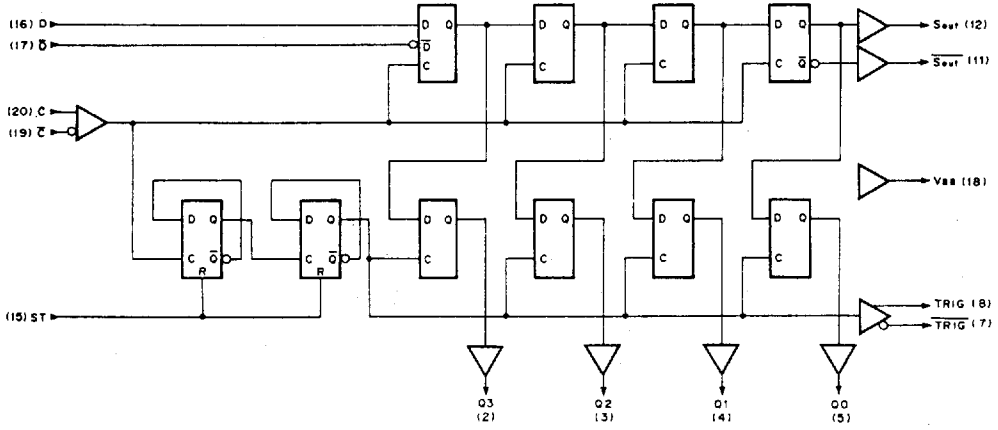
$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	C	Qn		1280	1430	1600	ps
	T_{PHL}				1270	1420	1590	
	T_{PLH}		S_{OUT}		790	940	1110	
	T_{PHL}				820	970	1180	
	T_{PLH}		TRIG		1090	1260	1430	
	T_{PHL}				1150	1320	1490	
Set up time	T_S	D, C	Qn		−20			
Hold time	T_H	C, D			520			
Release time	T_R	R, C			320			
Min. Pulse width	T_{PW}	R	TRIG		330			
Max. Clock frequency	f_{MAX}	C	Qn		1.6	2.1		GHz
Rise time	T_{TLH}		Qn, S_{OUT} TRIG	20% to 80%		400	500	ps
Fall time	T_{THL}					350	430	

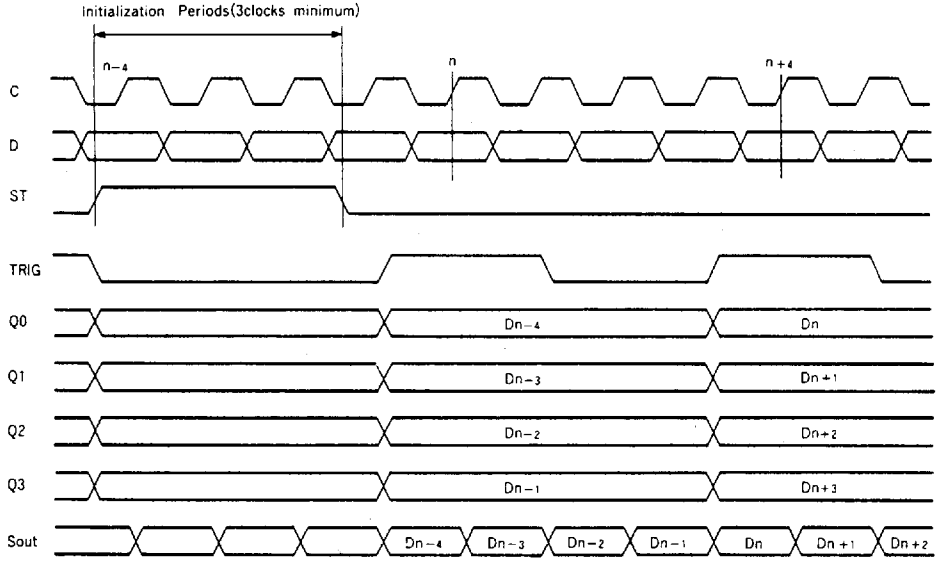
Note: AC test circuit; See pages 4-4 and 4-5.

T-68-11-51

Logic Diagram

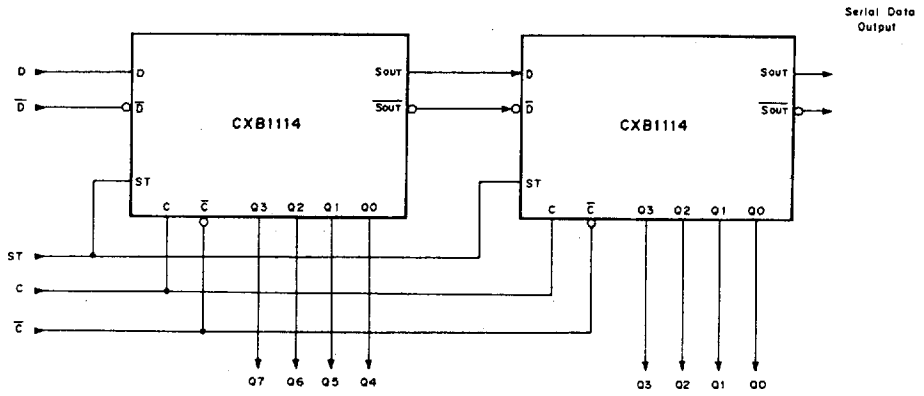


Timing Diagram



T-68-11-51

Typical Application 1 to 8 Demultiplexer/Serial to Parallel Converter



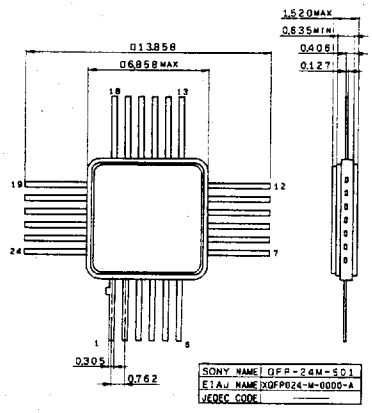
Package Data

T-90-20

Package Outline Uuit: mm

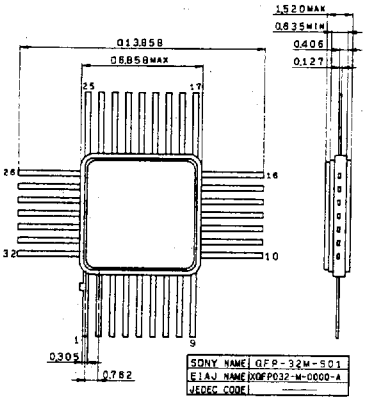
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



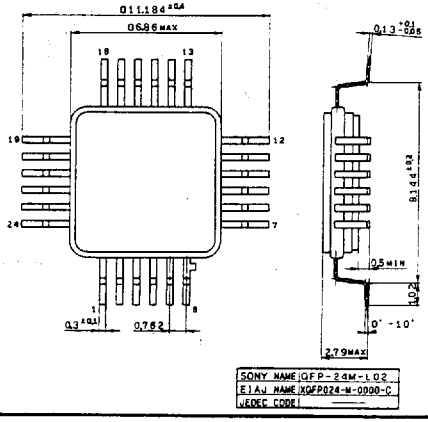
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



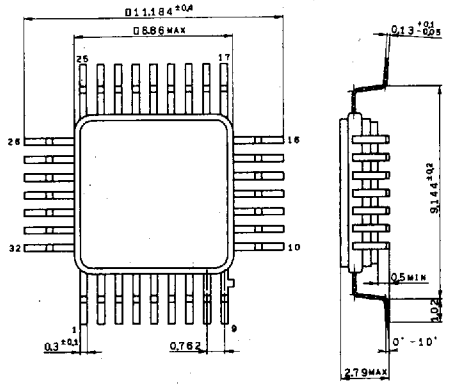
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

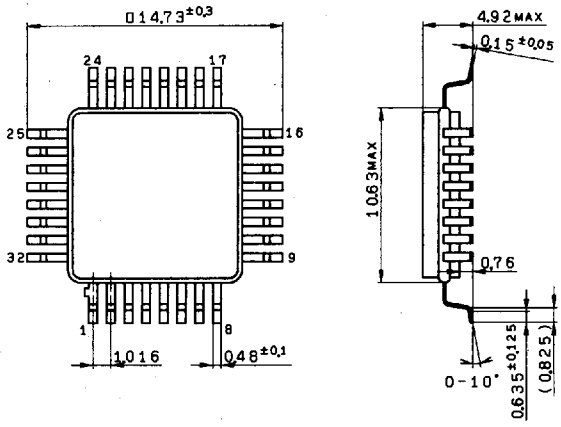
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



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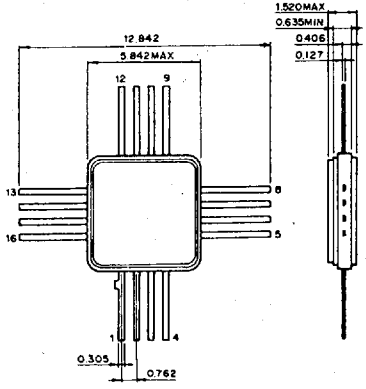
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

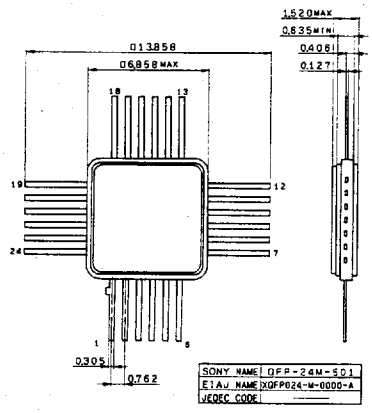
Package Data

T-90-20

Package Outline Uuit: mm

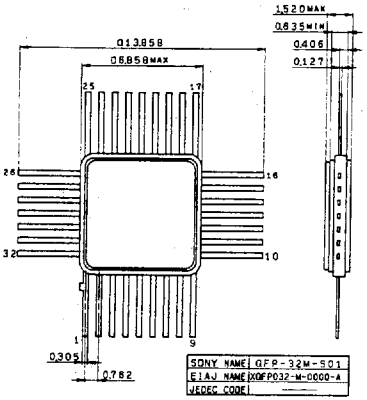
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



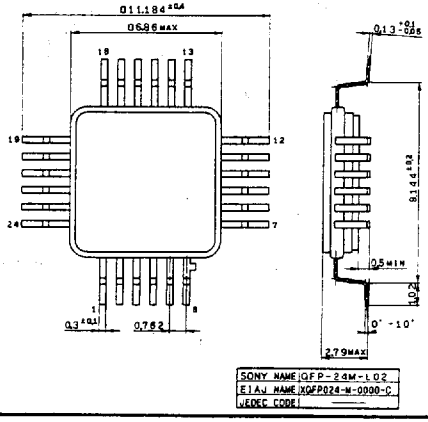
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



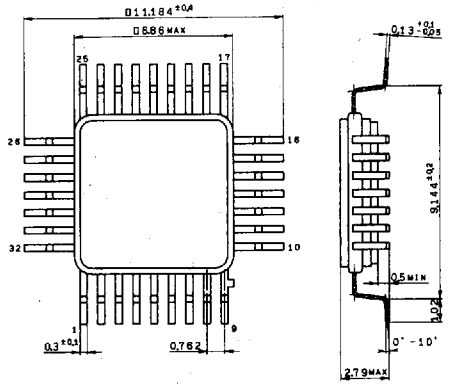
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

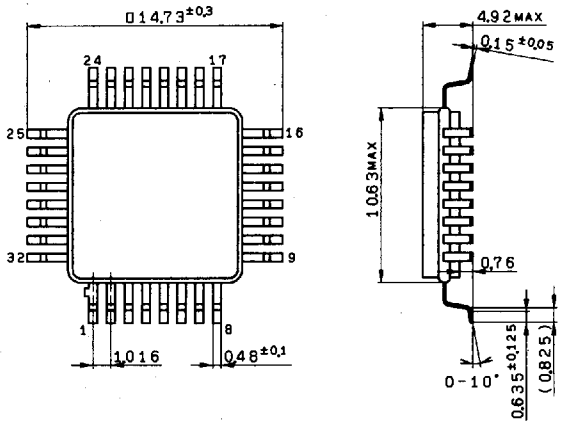
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP