+1.8V, Low Power, Quad-Input, 16-Bit $\sum - \Delta$ A/D Converter with Power Fault Monitor and Microprocessor Reset Circuit

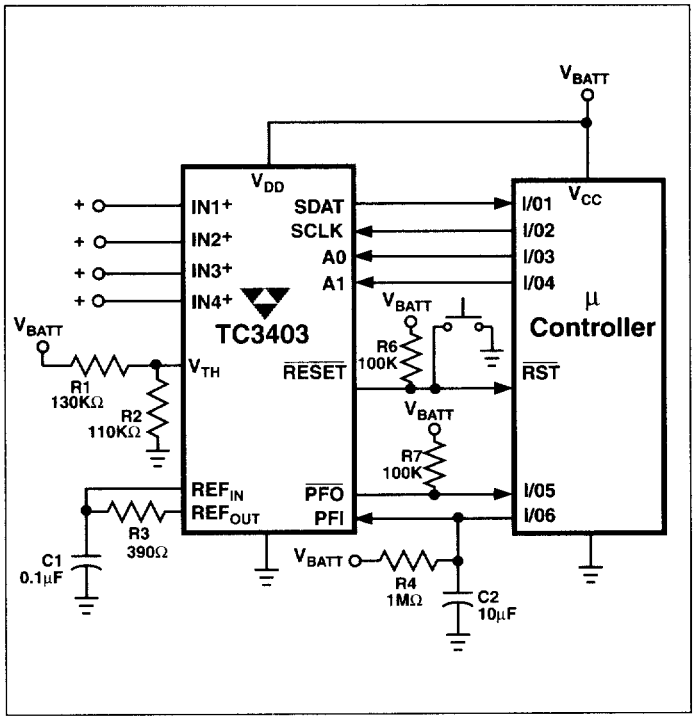
FEATURES

- 16-Bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-Bit Resolution at 512 Conversions Per Second
- 1.8V – 5.5V Operation, Low Power Operating .... 280µA ..... Sleep: 93µA
- Four Single Ended Inputs with Built-In Multiplexer
- MicroPort™ Serial Bus Requires Only Two Interface Lines
- Uses Internal or External Reference
- V_{DD} Monitor and Reset Generator Operational in Shutdown Mode
- Early Warning Power Fail Detector, Also Suitable as Wake-Up Timer Operational in Shutdown Mode
- Automatically Enters Sleep Mode When Not In Use
- 16-Pin QSOP and PDIP Packages

TYPICAL APPLICATIONS

- Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
- Embedded Systems, Data Loggers, Portable Equipment
- Medical Instruments

TYPICAL APPLICATION



GENERAL DESCRIPTION

The TC3403 is a low cost, low power analog-to-digital converter based on TelCom's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3403 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. A V_{DD} monitor with reset generator provides Power-On Reset and Brown-out protection while an extra threshold detector is suitable for use as an early warning power fail detector, or as a wake-up timer.

The TC3403's 2-wire MicroPort™digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

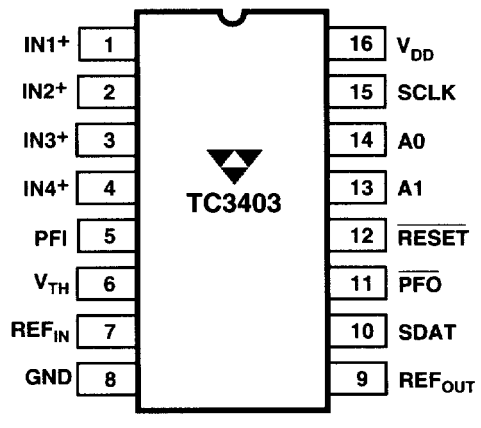
The TC3403 is available in 16-Pin PDIP and 16-Pin QSOP packages.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC3403VPE	16-Pin PDIP (Narrow)	0°C to +85°C
TC3403VQR	16-Pin QSOP (Narrow)	0°C to +85°C

PIN CONFIGURATIONS

16-Pin PDIP/QSOP



PIN DESCRIPTION

TC3403 Pin No.	Name	Description
1,2,3,4	INn+	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. *(See Electrical Characteristics.)*
5	PFI	Analog Input. This is the positive input to an internal comparator used as a threshold detector. The negative input is tied to an internal reference.
6	V_{TH}	Analog Input. This is the positive input to the internal comparator used to monitor the voltage supply. The negative input is tied to an internal reference. When V_{TH} falls below the internal reference, the reset generator drives $\overline{RESET}$ low as specified in the *Electrical Characteristics* section.
7	REF_{IN}	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be connected to REF_{OUT} as shown on page 1 or scaled using a resistor divider. Any user supplied reference voltage or the power supply rail may be used in place of REF_{OUT}.
8	GND	Ground Terminal.
9	REF_{OUT}	Analog Output. The internal reference connects to this pin. It may be scaled externally, if desired, and tied to the REF_{IN} input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin. (See *Electrical Characteristics.*)
10	SDAT	Digital Output (push-pull). This is the MicroPort™ serial data output. SDAT is driven low while the TC3403 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high-to-low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).
11	$\overline{PFO}$	Digital Output (open drain). This is the output of the internal threshold detector. When PFI is less than the internal reference, $\overline{PFO}$ is driven low.
12	$\overline{RESET}$	Digital Output (open drain). This is the output of the V_{DD} monitor reset generator. $\overline{RESET}$ is driven low when a power-on reset or brown-out condition is detected. (See *AC Electrical Characteristics.*)
13	A1	Digital Input. Controls analog multiplexer in conjunction with A0 to select one of the four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
14	A0	Digital Input. Controls analog multiplexer in conjunction with A1 to select one of four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
15	SCLK	Digital Input. This is the MicroPort™ serial clock input. After the conversion starts, each addi tional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
16	V_{DD}	Power Supply Input. (See *Electrical Characteristics* .)