FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-30339-1E

MEMORY

DRAM CARD

JEIDA * [DRAM Card Guide Line Ver. 2.0] conformable

MB98B7515/7516/7517/7518

DYNAMIC RANDOM ACCESS MEMORY CARD
16 M/32 M - BYTE

■ DESCRIPTION

The MB98B7515 is a DRAM Card (4,194,304 words × 32 bits) with eight MB8117400A's mounted.

The MB98B7516 is a DRAM Card (4,194,304 words × 36 bits) with eight MB8117400A's and four MB814100A mounted.

The MB98B7517 is a DRAM Card (8,388,608 words × 32 bits) with sixteen MB8117400A's mounted.

The MB98B7518 is a DRAM Card (8,388,608 words × 36 bits) with sixteen MB8117400A's and eight MB814100A mounted.

The connector used for these series is a 88-pin, two-piece connector.

This card complies with JEIDA [DRAM Card Guide Line Ver. 2.0]

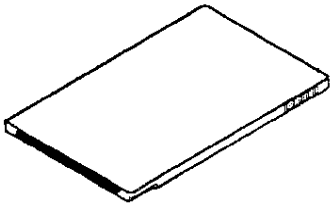
*: Japanese Electronic Industry Development Association (JEIDA).

■ FEATURES

- Outside dimensions: 85.6 mm × 54.0 mm × 3.3 mm
- Supply voltage: +5 V ±5 %
- Input/output level TTL compatible
- 2,048 refresh cycles / 128 ms (dispersion refresh)
- $\overline{CAS}$ before $\overline{RAS}$ Refresh, $\overline{RAS}$ Only Refresh, and Hidden Refresh are possible.
- High-speed Page Mode is available.
- DRAM with Substrate Bias Generator is mounted.
- 88-pin two-piece connector

■ PACKAGE

88-pin DRAM Card

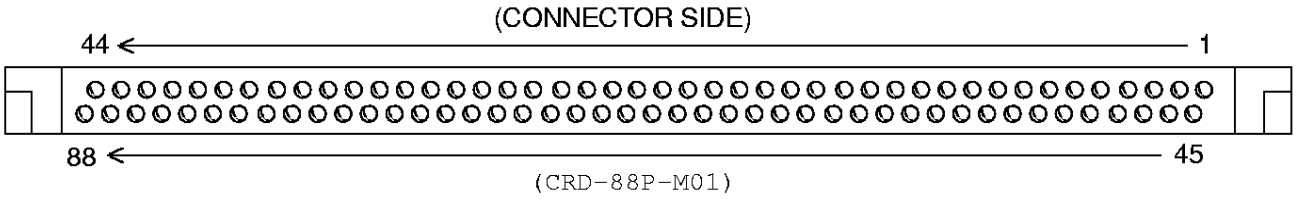


(CRD-88P-M01)

■ PRODUCT CLASS

Part Number	Memory Device	Memory configuration	Access time (max.) ns		Cycle time (min.) ns		Power dissipation (max.) mW		
			Normal Mode	High-speed page mode	Normal Mode	High-speed page mode	Operating	Stand-by	
								TTL	CMOS
MB98B7515-70	MB8117400 A-60 × 8 pcs	4 M × 32	70	45	130	50	4,988	137	47.3
MB98B7516-70	MB8117400 A-60 × 8 pcs MB814100 A-60L × 4 pcs	4 M × 36					7,298	168	52.5
MB98B7517-70	MB8117400 A-60 × 16 pcs	8 M × 32					5,093	221	89.3
MB98B7518-70	MB8117400 A-60 × 16 pcs MB814100 A-60L × 8 pcs	8 M × 36					7,455	284	99.8
MB98B7515-80	MB8117400 A-70 × 8 pcs	4 M × 32	80	50	150	55	4,305	137	47.3
MB98B7516-80	MB8117400 A-70 × 8 pcs MB814100 A-70L × 4 pcs	4 M × 36					6,405	168	52.5
MB98B7517-80	MB8117400 A-70 × 16 pcs	8 M × 32					4,410	221	89.3
MB98B7518-80	MB8117400 A-70 × 16 pcs MB814100 A-70L × 8 pcs	8 M × 36					6,563	284	99.8

■ PIN ASSIGNMENTS



(CRD-88P-M01)

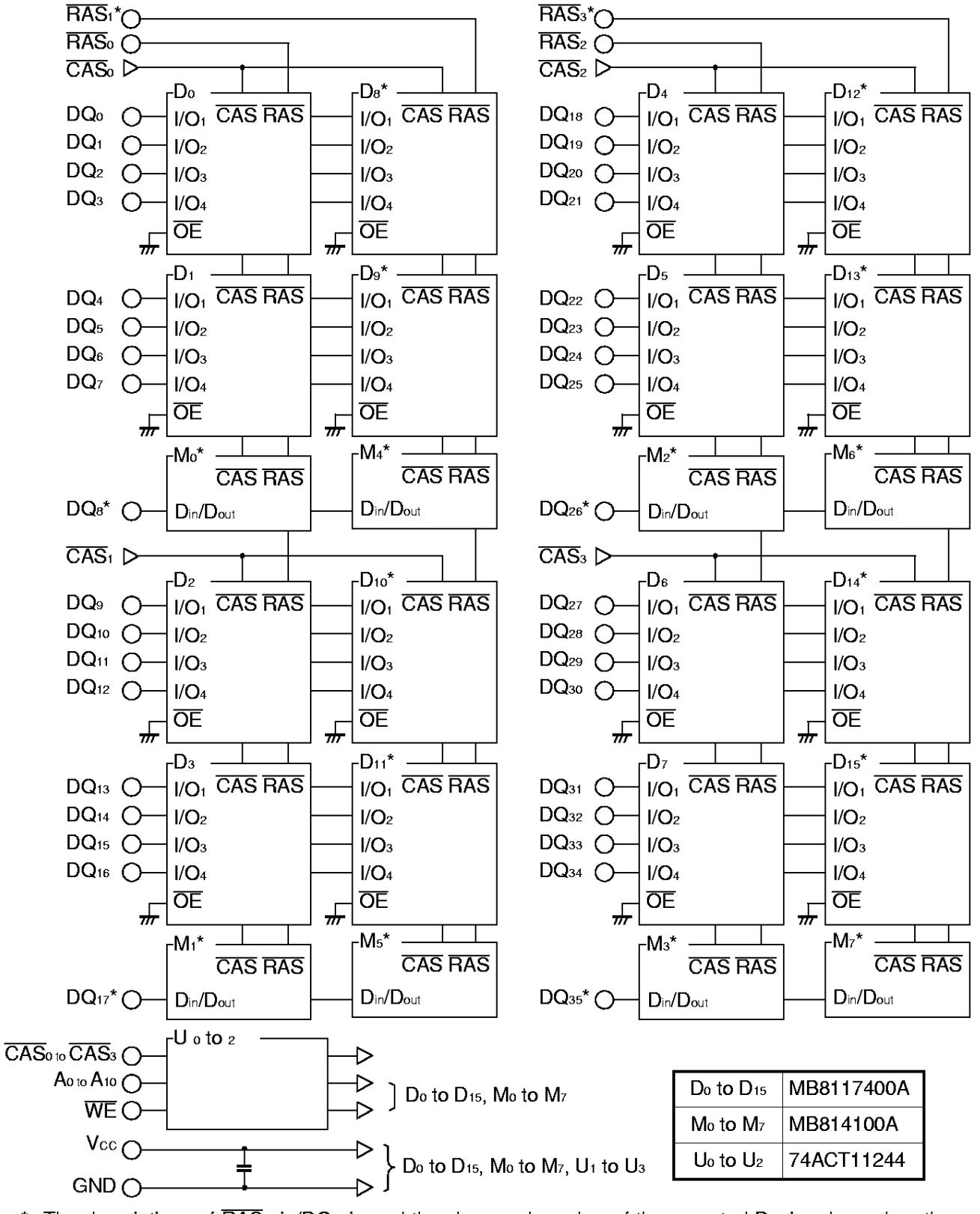
Pin symbol	Pin name
A0 to A_{10}	Address
$\overline{RAS_0}$ to $\overline{RAS_3}$	Load address strobe
$\overline{CAS_0}$ to $\overline{CAS_3}$	Column address strobe
$\overline{WE}$	Write enable
DQ_0 to DQ_{35}	Input/output data
PD_1 to PD_8	Presence detect pin
N.C.	No connection
V_{CC}	Power supply (+ 5 V)
GND	Ground

Pin No	Pin symbol	Pin No	Pin symbol	Pin No	Pin symbol	Pin No	Pin symbol
1	GND	23	$\overline{CAS_0}$	45	GND	67	GND
2	DQ_0	24	$\overline{CAS_1}$	46	DQ_{18}	68	$\overline{CAS_3}$
3	DQ_1	25	N.C.	47	DQ_{19}	69	$\overline{RAS_3}$*1
4	DQ_2	26	$\overline{RAS_2}$	48	DQ_{20}	70	$\overline{WE}$
5	DQ_3	27	V_{CC}	49	DQ_{21}	71	PD_1*2
6	DQ_4	28	PD_2*2	50	DQ_{22}	72	PD_3*2
7	DQ_5	29	PD_4*2	51	DQ_{23}	73	GND
8	DQ_6	30	PD_6*2	52	DQ_{24}	74	PD_5*2
9	V_{CC}	31	N.C.	53	DQ_{25}	75	PD_7*2
10	DQ_7	32	N.C.	54	DQ_{26}*1	76	PD_8*2
11	N.C.	33	DQ_{17}*1	55	N.C.	77	N.C.
12	DQ_8*1	34	DQ_9	56	GND	78	N.C.
13	A_0	35	N.C.	57	A_1	79	DQ_{35}*1
14	A_2	36	DQ_{10}	58	A_3	80	DQ_{27}
15	V_{CC}	37	V_{CC}	59	A_5	81	DQ_{28}
16	A_4	38	DQ_{11}	60	A_7	82	DQ_{29}
17	N.C.	39	DQ_{12}	61	A_9	83	DQ_{30}
18	A_6	40	DQ_{13}	62	N.C	84	DQ_{31}
19	A_8	41	DQ_{14}	63	GND	85	DQ_{32}
20	A_{10}	42	DQ_{15}	64	N.C.	86	DQ_{33}
21	N.C.	43	DQ_{16}	65	$\overline{RAS_1}$*1	87	DQ_{34}
22	$\overline{RAS_0}$	44	GND	66	$\overline{CAS_2}$	88	GND

*1: The descriptions of $\overline{RAS}$ pin/DQ pin depend on the series. Refer to "■ Differences among the Series" for details.

*2: The description of PD pin depends on the series. Refer to "■About PD pin" for details.

■ BLOCK DIAGRAM



D0 to D15	MB8117400A
M0 to M7	MB814100A
U0 to U2	74ACT11244

* : The descriptions of $\overline{RAS}$ pin/DQ pin and the class and number of the mounted Device depend on the series. Refer to "■ Differences among the Series" for details.

■ DIFFERENCES AMONG THE SERIES

1. List of Pins and Mounted Devices

Series	Part Number	MB98B7515	MB98B7516	MB98B7517	MB98B7518
Pin	$\overline{RAS_0}$	○	○	○	○
	$\overline{RAS_1}$	—	—		
	$\overline{RAS_2}$	○	○		
	$\overline{RAS_3}$	—	—		
	DQ_0 to DQ_7	○	○	○	○
	DQ_8	—		—	
	DQ_9 to DQ_{16}	○		○	
	DQ_{17}	—		—	
	DQ_{18} to DQ_{25}	○		○	
	DQ_{26}	—		—	
	DQ_{27} to DQ_{34}	○		○	
	DQ_{35}	—		—	
Device	D_0 to D_1	○	○	○	○
	D_8 to D_{15}	—	—		
	M_0 to M_3	—	○	—	○
	M_4 to M_7		—		

○ : Mounted — : Not mounted

■ FUNCTIONAL TRUTH TABLE

1. Read/Write Modes

$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$	$\overline{CAS}_{0,1}$	$\overline{CAS}_{2,3}$	Active memory	DQ_0 to DQ_{17}	DQ_{18} to DQ_{35}
H	H	H	H	H	H	—	High-Z	High-Z
L	H	H	H	L	H	D_0 to D_3, $M_{0,1}$	I/O data	High-Z
H	L	H	H	L	H	D_8 to D_{11}, $M_{4,5}$	I/O data	High-Z
H	H	L	H	H	L	D_4 to D_7, $M_{2,3}$	High-Z	I/O data
H	H	H	L	H	L	D_{12} to D_{15}, $M_{6,7}$	High-Z	I/O data
L	H	L	H	L	L	D_0 to D_7, M_0 to M_3	I/O data	
L	L	X	X	X	X	Prohibited operation		
H	L	H	L	L	L	D_0 to D_7, M_0 to M_3	I/O data	
X	X	L	L	X	X	Prohibited operation		

2. $\overline{RAS}$ Only Refresh Mode

$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$	$\overline{CAS}_{0,1}$	$\overline{CAS}_{2,3}$	Active memory	DQ_0 to DQ_{17}	DQ_{18} to DQ_{35}
L	H	H	H	H	H	D_0 to D_3, $M_{0,1}$	High-Z	
H	L	H	H	H	H	D_8 to D_{11}, $M_{4,5}$	High-Z	
H	H	L	H	H	H	D_4 to D_7, $M_{2,3}$	High-Z	
H	H	H	L	H	H	D_{12} to D_{15}, $M_{6,7}$	High-Z	
L	H	L	H	H	H	D_0 to D_7, M_0 to M_3	High-Z	
L	L	X	X	X	X	Prohibited operation		
H	L	H	L	H	H	D_8 to D_{15}, M_4 to M_7	High-Z	
X	X	L	L	X	X	Prohibited operation		

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh Mode

$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$	$\overline{CAS}_{0,1}$	$\overline{CAS}_{2,3}$	Active memory	DQ_0 to DQ_{17}	DQ_{18} to DQ_{35}
L	H	H	H	L	H	D_0 to D_3, $M_{0,1}$	High-Z	
H	L	H	H	L	H	D_8 to D_{11}, $M_{4,5}$	High-Z	
H	H	L	H	H	L	D_4 to D_7, $M_{2,3}$	High-Z	
H	H	H	L	H	L	D_{12} to D_{15}, $M_{6,7}$	High-Z	
L	H	L	H	L	L	D_0 to D_7, M_0 to M_3	High-Z	
L	L	X	X	X	X	Prohibited operation		
H	L	H	L	L	L	D_8 to D_{15}, M_4 to M_7	High-Z	
X	X	L	L	X	X	Prohibited operation		

4. Hidden Refresh Mode

$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$	$\overline{CAS}_{0,1}$	$\overline{CAS}_{2,3}$	Active memory	DQ_0 to DQ_{17}	DQ_{18} to DQ_{35}
H→L	H	H	H	L	H	D_0 to D_3, $M_{0,1}$	I/O data	High-Z
H	H→L	H	H	L	H	D_8 to D_{11}, $M_{4,5}$	I/O data	High-Z
H	H	H→L	H	H	L	D_4 to D_7, $M_{2,3}$	High-Z	I/O data
H	H	H	H→L	H	L	D_{12} to D_{15}, $M_{6,7}$	High-Z	I/O data
H→L	H	H→L	H	L	L	D_0 to D_7, M_0 to M_3	I/O data	
H→L	H→L	X	X	X	X	Prohibited operation		
H	H→L	H	H→L	L	L	D_8 to D_{15}, M_4 to M_7	I/O data	
X	X	H→L	H→L	X	X	Prohibited operation		

X: "H" or "L".

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

(Voltage is with reference to the GND (ground))

Parameter	Symbol	Value				Unit
		MB98B7515	MB98B7516	MB98B7517	MB98B7518	
Supply Voltage	V_{CC}	−0.5 to +6.0				V
Input Voltage	V_{IN}	0 to V_{CC}				V
Output Voltage	V_{OUT}	0 to V_{CC}				V
Storage Temperature	T_{stg}	−30 to +70				°C
Power Dissipation	P_D	8	12	16	24	W
Output Current (D.C.)	I_{OUT}	50				mA

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Voltage is with reference to the GND (ground))

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +55°C
	V_{SS}	0	0	0		
"High" Level Input Voltage (All Input Pins)	V_{IH}	2.4	—	V_{CC}	V	
"Low" Level Input Voltage (All Input Pins)	V_{IL}	0	—	0.8	V	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) MB98B7515 NOTE 3

(On the recommended operating conditions)

Parameter	Notes		Symbol	Min.	Max.	Unit	Measuring conditions
Supply Current (When Normally Operating)	*2		I_{CC1}	—	660	mA	Average supply current t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling
Supply Current (When Stand-by)		TTL	I_{CC2}	—	20	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
		CMOS		—	9		$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Supply Current (On $\overline{RAS}$ Only Refresh)	*2		I_{CC3}	—	660	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$
Supply Current (In High-speed Page Mode)	*2		I_{CC4}	—	660	mA	Average supply current t_{PC} = min. $\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling
Supply Current (On $\overline{CAS}$ Before $\overline{RAS}$ Refresh)	*2		I_{CC5}	—	660	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$
Input Leakage Current		$\overline{CAS_0}$ to $\overline{CAS_3}$ A_0 to A_{10}, $\overline{WE}$	$I_{I(L)}$	–10	10	µA	(0 V ≤ V_{IN} ≤ 5.25 V) (0 V except the measured pin, 4.75 V ≤ V_{CC} ≤ 5.25 V)
		$\overline{RAS_0}$, $\overline{RAS_2}$		–30	30		
Output Leakage Current		DQ_0 to DQ_7, DQ_9 to DQ_{16} DQ_{18} to DQ_{25}, DQ_{27} to DQ_{34}	$I_{O(L)}$	–10	10	µA	(With output impedance high 0 V ≤ V_{OUT} ≤ 5.25 V)
		—		—	—		
"High" Level Output Voltage	*1		V_{OH}	2.4	—	V	(I_{OH} = –5 mA)
"Low" Level Output Voltage	*1		V_{OL}	—	0.4	V	(I_{OL} = 4.2 mA)

(2) MB98B7516 NOTE 3

(On the recommended operating conditions)

Parameter	Notes		Symbol	Min.	Max.	Unit	Measuring conditions
Supply Current (When Normally Operating)	*2		I_{CC1}	—	1060	mA	Average supply current t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling
Supply Current (When Stand-by)		TTL	I_{CC2}	—	25	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
		CMOS		—	10		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V
Supply Current (On $\overline{RAS}$ Only Refresh)	*2		I_{CC3}	—	1060	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}
Supply Current (In High-speed Page Mode)	*2		I_{CC4}	—	860	mA	Average supply current t_{PC} = min. $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling
Supply Current (On $\overline{CAS}$ Before $\overline{RAS}$ Refresh)	*2		I_{CC5}	—	980	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$
Input Leakage Current		$\overline{CAS_0}$ to $\overline{CAS_3}$ A_0 to A_{10}, $\overline{WE}$	$I_{I(L)}$	–10	10	µA	(0 V ≤ V_{IN} ≤ 5.25 V) (0 V except the measured pin, 4.75 V ≤ V_{CC} ≤ 5.25 V)
		$\overline{RAS_0}$, $\overline{RAS_2}$		–40	40		
Output Leakage Current		DQ_0 to DQ_7, DQ_9 to DQ_{16} DQ_{18} to DQ_{25}, DQ_{27} to DQ_{34}	$I_{O(L)}$	–10	10	µA	(With output impedance high 0 V ≤ V_{OUT} ≤ 5.25 V)
		DQ_8, DQ_{17}, DQ_{26}, DQ_{35}		–20	20		
"High" Level Output Voltage	*1		V_{OH}	2.4	—	V	(I_{OH} = –5 mA)
"Low" Level Output Voltage	*1		V_{OL}	—	0.4	V	(I_{OL} = 4.2 mA)

(3) MB98B7517 NOTES 3, 19

(On the recommended operating conditions)

Parameter	Notes		Symbol	Min.	Max.	Unit	Measuring conditions
Supply Current (When Normally Operating)	*2		I_{CC1}	—	680	mA	Average supply current t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling
Supply Current (When Stand-by)		TTL	I_{CC2}	—	35	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
		CMOS		—	17		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V
Supply Current (On $\overline{RAS}$ Only Refresh)	*2		I_{CC3}	—	680	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}
Supply Current (In High-speed Page Mode)	*2		I_{CC4}	—	680	mA	Average supply current t_{PC} = min. $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling
Supply Current (On $\overline{CAS}$ Before $\overline{RAS}$ Refresh)	*2		I_{CC5}	—	680	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$
Input Leakage Current		$\overline{CAS_0}$ to $\overline{CAS_3}$ A_0 to A_{10}, $\overline{WE}$	$I_{I(L)}$	–10	10	µA	(0 V ≤ V_{IN} ≤ 5.25 V) (0 V except the measured pin, 4.75 V ≤ V_{CC} ≤ 5.25 V)
		$\overline{RAS_0}$ to $\overline{RAS_3}$		–30	30		
OutpuT Leakage Current		DQ_0 to DQ_7, DQ_9 to DQ_{16} DQ_{18} to DQ_{25}, DQ_{27} to DQ_{34}	$I_{O(L)}$	–20	20	µA	(With output impedance high 0 V ≤ V_{OUT} ≤ 5.25 V)
		—		—	—		
"High" Level Output Voltage	*1		V_{OH}	2.4	—	V	(I_{OH} = –5 mA)
"Low" Level Output Voltage	*1		V_{OL}	—	0.4	V	(I_{OL} = 4.2 mA)

(4) MB98B7518 NOTES 3, 19

(On the recommended operating conditions)

Parameter	Notes		Symbol	Min.	Max.	Unit	Measuring conditions
Supply Current (When Normally Operating)	*2		I_{CC1}	—	1080	mA	Average supply current t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling
Supply Current (When Stand-by)		TTL	I_{CC2}	—	45	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
		CMOS		—	19		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V
Supply Current (On $\overline{RAS}$ Only Refresh)	*2		I_{CC3}	—	1080	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}
Supply Current (In High-speed Page Mode)	*2		I_{CC4}	—	880	mA	Average supply current t_{PC} = min. $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling
Supply Current (On $\overline{CAS}$ Before $\overline{RAS}$ Refresh)	*2		I_{CC5}	—	1000	mA	Average supply current t_{RC} = min. $\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$
Input Leakage Current		$\overline{CAS_0}$ to $\overline{CAS_3}$ A_0 to A_{10}, $\overline{WE}$	$I_{I(L)}$	–10	10	µA	(0 V ≤ V_{IN} ≤ 5.25 V) (0 V except the measured pin, 4.75 V ≤ V_{CC} ≤ 5.25 V)
		$\overline{RAS_0}$ to $\overline{RAS_3}$		–40	40		
Output Leakage Current		DQ_0 to DQ_7, DQ_9 to DQ_{16} DQ_{18} to DQ_{25}, DQ_{27} to DQ_{34}	$I_{O(L)}$	–20	20	µA	(With output impedance high 0 V ≤ V_{OUT} ≤ 5.25 V)
		DQ_8, DQ_{17}, DQ_{26}, DQ_{35}		–30	30		
"High" Level Output Voltage	*1		V_{OH}	2.4	—	V	(I_{OH} = –5 mA)
"Low" Level Output Voltage	*1		V_{OL}	—	0.4	V	(I_{OL} = 4.2 mA)

2. AC Characteristics NOTES 3, 4, 5

(1) MB98B7515/6/7/8-70

(On the recommended operating conditions)

No.	Parameter	Notes	Symbol	Min.	Max.	Unit
1	Refresh Interval		t_{REF}	—	128	ms
2	Random Read/write Cycle Time		t_{RC}	130	—	ns
3	Access Time from $\overline{RAS}$	*6,9	t_{RAC}	—	70	ns
4	Access Time from $\overline{CAS}$	*7,9	t_{CAC}	—	25	ns
5	Column Address Access Time	*8,9	t_{AA}	—	40	ns
6	Output Data Hold Time		t_{OH}	2	—	ns
7	Output Turn On Delay Time		t_{ON}	2	—	ns
8	Output Turn Off Delay Time	*10	t_{OFF}	—	25	ns
9	Turn On/turn Off Periods		t_T	5	50	ns
10	$\overline{RAS}$ Precharge Time		t_{RP}	50	—	ns
11	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	ns
12	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	ns
13	$\overline{RAS} \cdot \overline{CAS}$ Precharge Time		t_{CRP}	15	—	ns
14	$\overline{RAS} \cdot \overline{CAS}$ Delay Time	*11,12	t_{RCD}	20	45	ns
15	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	ns
16	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	ns
17	$\overline{CAS}$ Precharge Time	*17	t_{CPN}	10	—	ns
18	Low Address Setup Time		t_{ASR}	10	—	ns
19	Low Address Hold Time		t_{RAH}	10	—	ns
20	Column Address Setup Time		t_{ASC}	2	—	ns
21	Column Address Hold Time		t_{CAH}	15	—	ns
22	$\overline{RAS}$ Column Address Delay Time	*13	t_{RAD}	15	30	ns
23	Column Address $\overline{RAS}$ Read Time		t_{RAL}	40	—	ns
24	Column Address $\overline{CAS}$ Read Time		t_{CAL}	40	—	ns
25	Read Instruction Setup Time		t_{RCS}	0	—	ns
26	Read Instruction Hold Time from $\overline{RAS}$	*14	t_{RRH}	0	—	ns
27	Read Instruction Hold Time	*14	t_{RCH}	0	—	ns
28	Write Instruction Setup Time	*15	t_{WCS}	2	—	ns
29	Write Instruction Hold Time		t_{WCH}	15	—	ns
30	Write Instruction Pulse Width		t_{WP}	15	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	Min.	Max.	Unit
31	Write Instruction · $\overline{RAS}$ Read Time		t_{RWL}	25	—	ns
32	Write Instruction · $\overline{CAS}$ Read Time		t_{CWL}	25	—	ns
33	Data Input Setup Time		t_{DS}	0	—	ns
34	Data Input Hold Time		t_{DH}	25	—	ns
35	$\overline{CAS}$ Active Display from $\overline{RAS}$ Precharge		t_{RPC}	5	—	ns
36	$\overline{RAS}$ · $\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$)		t_{CSR}	10	—	ns
37	$\overline{RAS}$ · $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)		t_{CHR}	10	—	ns
38	$\overline{WE}$ Setup Time from $\overline{RAS}$	*18	t_{WSR}	10	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$	*18	t_{WHR}	10	—	ns
40	Data Input $\overline{CAS}$ Delay Time		t_{DZC}	0	—	ns
41	High-speed Page Mode Read/write Cycle Time		t_{PC}	50	—	ns
42	Access Time from High-speed Page Mode $\overline{CAS}$ Precharge	*9,16	t_{CPA}	—	45	ns
43	High-speed Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	ns
44	$\overline{RAS}$ Hold Time From High-speed Page Mode $\overline{CAS}$ Precharge		t_{RHCP}	40	—	ns

(2) MB98B7515/6/7/8-80

(On the recommended operating conditions)

No.	Parameter	Notes	Symbol	Min.	Max.	Unit
1	Refresh Interval		t_{REF}	—	128	ms
2	Random Read/Write Cycle Time		t_{RC}	150	—	ns
3	Access Time from $\overline{RAS}$	*6,9	t_{RAC}	—	80	ns
4	Access Time from $\overline{CAS}$	*7,9	t_{CAC}	—	30	ns
5	Column Address Access Time	*8,9	t_{AA}	—	45	ns
6	Output Data Hold Time		t_{OH}	2	—	ns
7	Output Turn On Delay Time		t_{ON}	2	—	ns
8	Output Turn Off Delay Time	*10	t_{OFF}	—	30	ns
9	Turn On/turn Off Periods		t_T	5	50	ns
10	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	ns
11	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	ns
12	$\overline{RAS}$ Hold Time		t_{RSH}	30	—	ns
13	$\overline{RAS} \cdot \overline{CAS}$ Precharge Time		t_{CRP}	15	—	ns
14	$\overline{RAS} \cdot \overline{CAS}$ Delay Time	*11,12	t_{RCD}	20	50	ns
15	$\overline{CAS}$ Pulse Width		t_{CAS}	30	—	ns
16	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	ns
17	$\overline{CAS}$ Precharge Time	*17	t_{CPN}	10	—	ns
18	Low Address Setup Time		t_{ASR}	10	—	ns
19	Low Address Hold Time		t_{RAH}	10	—	ns
20	Column Address Setup Time		t_{ASC}	2	—	ns
21	Column Address Hold Time		t_{CAH}	15	—	ns
22	$\overline{RAS}$ Column Address Delay Time	*13	t_{RAD}	15	35	ns
23	Column Address $\overline{RAS}$ Read Time		t_{RAL}	45	—	ns
24	Column Address $\overline{CAS}$ Read Time		t_{CAL}	45	—	ns
25	Read Instruction Setup Time		t_{RCS}	0	—	ns
26	Read Instruction Hold Time from $\overline{RAS}$	*14	t_{RRH}	0	—	ns
27	Read Instruction Hold Time	*14	t_{RCH}	0	—	ns
28	Write Instruction Setup Time	*15	t_{WCS}	2	—	ns
29	Write Instruction Hold Time		t_{WCH}	15	—	ns
30	Write Instruction Pulse Width		t_{WP}	15	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	Min.	Max.	Unit
31	Write Instruction · $\overline{RAS}$ Read Time		t_{RWL}	30	—	ns
32	Write Instruction · $\overline{CAS}$ Read Time		t_{CWL}	30	—	ns
33	Data Input Setup Time		t_{DS}	0	—	ns
34	Data Input Hold Time		t_{DH}	25	—	ns
35	$\overline{CAS}$ Active Display from $\overline{RAS}$ Precharge		t_{RPC}	5	—	ns
36	$\overline{RAS}$ · $\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$)		t_{CSR}	10	—	ns
37	$\overline{RAS}$ · $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)		t_{CHR}	12	—	ns
38	$\overline{WE}$ Setup Time from $\overline{RAS}$	*18	t_{WSR}	10	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$	*18	t_{WHR}	10	—	ns
40	Data Input $\overline{CAS}$ Delay Time		t_{DZC}	0	—	ns
41	High-speed Page Mode Read/write Cycle Time		t_{PC}	55	—	ns
42	Access Time from High-speed Page Mode $\overline{Cas}$ Precharge	*9,16	t_{CPA}	—	50	ns
43	High-speed Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	ns
44	$\overline{RAS}$ Hold Time From High-speed Page Mode $\overline{CAS}$ Precharge		t_{RHCP}	50	—	ns

Notes: *1. Voltage reference is V_{SS}.

*2. Output pin is open. Supply current depends on cycle time and output load. If $V_{IL} > -0.5$ V, $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, supply current depends on the number of address changes. If $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, the value of either I_{CC1}, I_{CC3}, I_{CC4} or I_{CC5} indicates that the address change has occurred only one time.

*3. A time delay of 200 µs (called the pause time) plus the dummy cycles (shown below) is necessary for these elements to function after power on. The dummy cycles are one of the following: eight $\overline{RAS}$ Only Refresh cycles, or eight $\overline{CAS}$ before $\overline{RAS}$ Refresh cycles ($\overline{WE}$ = "H"). If using the internal refresh counter, equal to or more than eight $\overline{CAS}$ before $\overline{RAS}$ Refresh cycles must be used for the dummy cycles.

*4. AC characteristics must be measured by using t_T = 5 ns.

*5. Input reference levels for specifying the timing are the V_{IH} (min.) and V_{IL} (max.).The transition time (t_T) is the time for a output voltage to switch from V_{IH} toV_{IL}.

*6. The t_{RAC} (max.) is guaranteed on the condition that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).Therefore, if $t_{RCD} > t_{RCD}$ (max.) and $t_{RAD} > t_{RAD}$ (max.), t_{RAC} will appear after the delay time equivalent to the difference between t_{RCD} and t_{RCD} (max.) or t_{RAD} and t_{RAD} (max.).

*7. If $t_{ASC} \geq t_{AA} - t_{CAC} - (t_T)$ with $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.), the access time is dependent of the $\overline{CAS}$.

*8. If $t_{ASC} \leq t_{AA} - t_{CAC} - (t_T)$ with $t_{RAD} \geq t_{RAD}$ (max.), the access time is dependent of the column address.

*9. 2TTL + 100PF load.

*10. The t_{OFF} is defined while the internal output buffer is in high impedance.

*11. The t_{RCD} (max.) is not a critical operating point, but a max. t_{RCD} value that guarantees t_{RAC} (max.). In case $t_{RCD} > t_{RCD}$ (max.), the access time depends on the t_{CAC} or t_{AA}.

*12. The t_{RCD} (min.) = t_{RAH} (min.) + 2t_T + t_{ASC} (min.).

*13. The t_{RAD} (max.) is not a critical operating point, but a max.t_{RAD} value that guarantees t_{RAC} (max.). In case $t_{RAD} > t_{RCD}$ (max.), the access time depends on the t_{CAC} or t_{AA}.

*14. Operation is guaranteed if one of the t_{RCH} or t_{RRH} is met.

*15. If $t_{WCS} \geq t_{WCS}$ (min.), the DQ(output) pin shows open (high impedance) during this cycle.

*16. The t_{CPA} regulates the access time if the $\overline{CAS}$ releases the column address latch, and this release consequently permits a new column address to be selected. Therefore, the t_{CPA} gets longer than t_{CPA} (max.) if the t_{CP} is long.

*17. Only $\overline{CAS}$ before $\overline{RAS}$ Refresh cycle is defined.

*18. The test mode is defined.

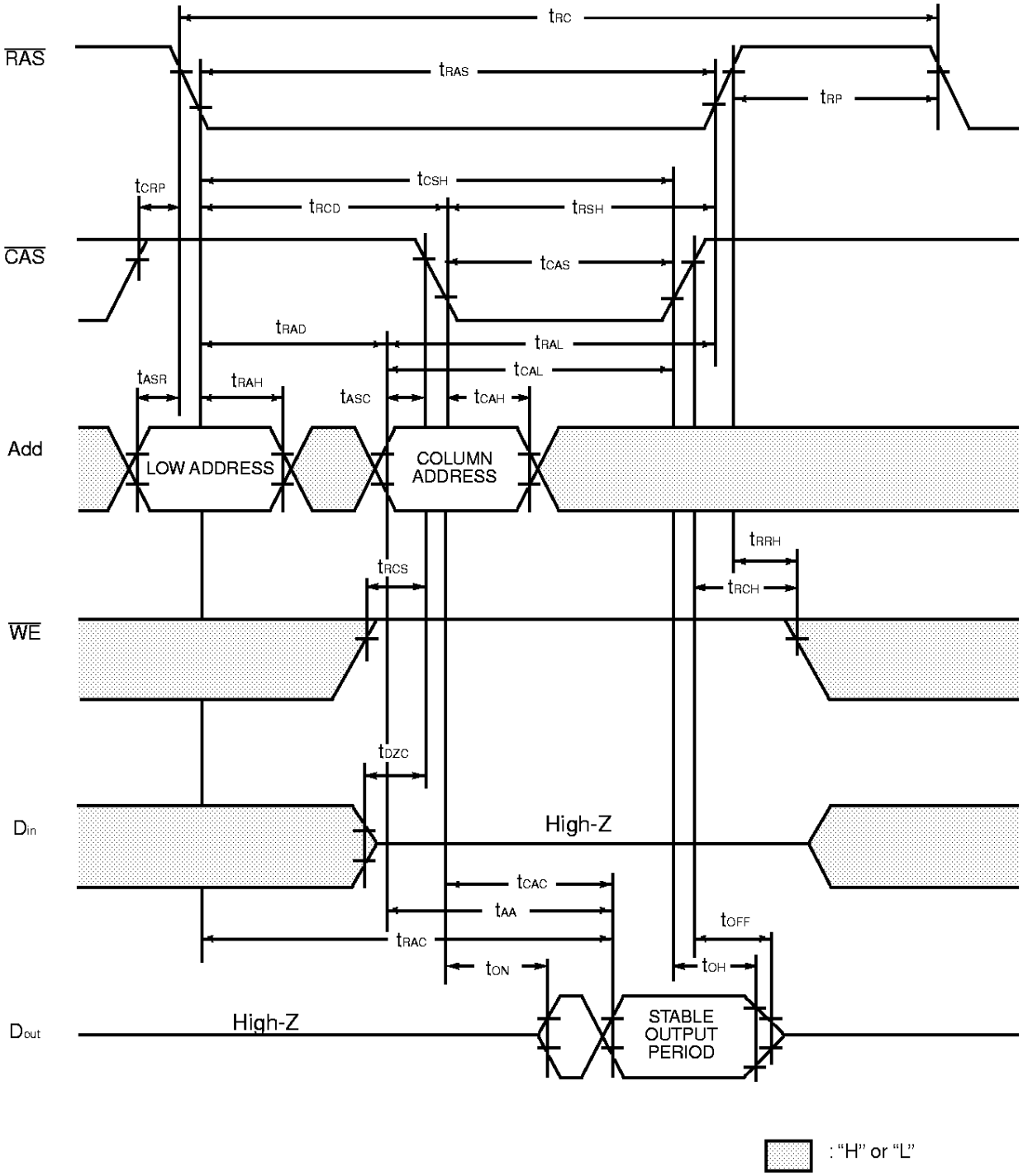
*19. On reading, the Bank 1 (controlled by $\overline{RAS_0}$ and $\overline{RAS_2}$)and Bank 2 (controlled by $\overline{RAS_1}$ and $\overline{RAS_3}$) must not work at the same time because the DQ pin is common to both the Bank 1 and Bank 2 (the other must be in stand-by).

3. Capacity between Pins

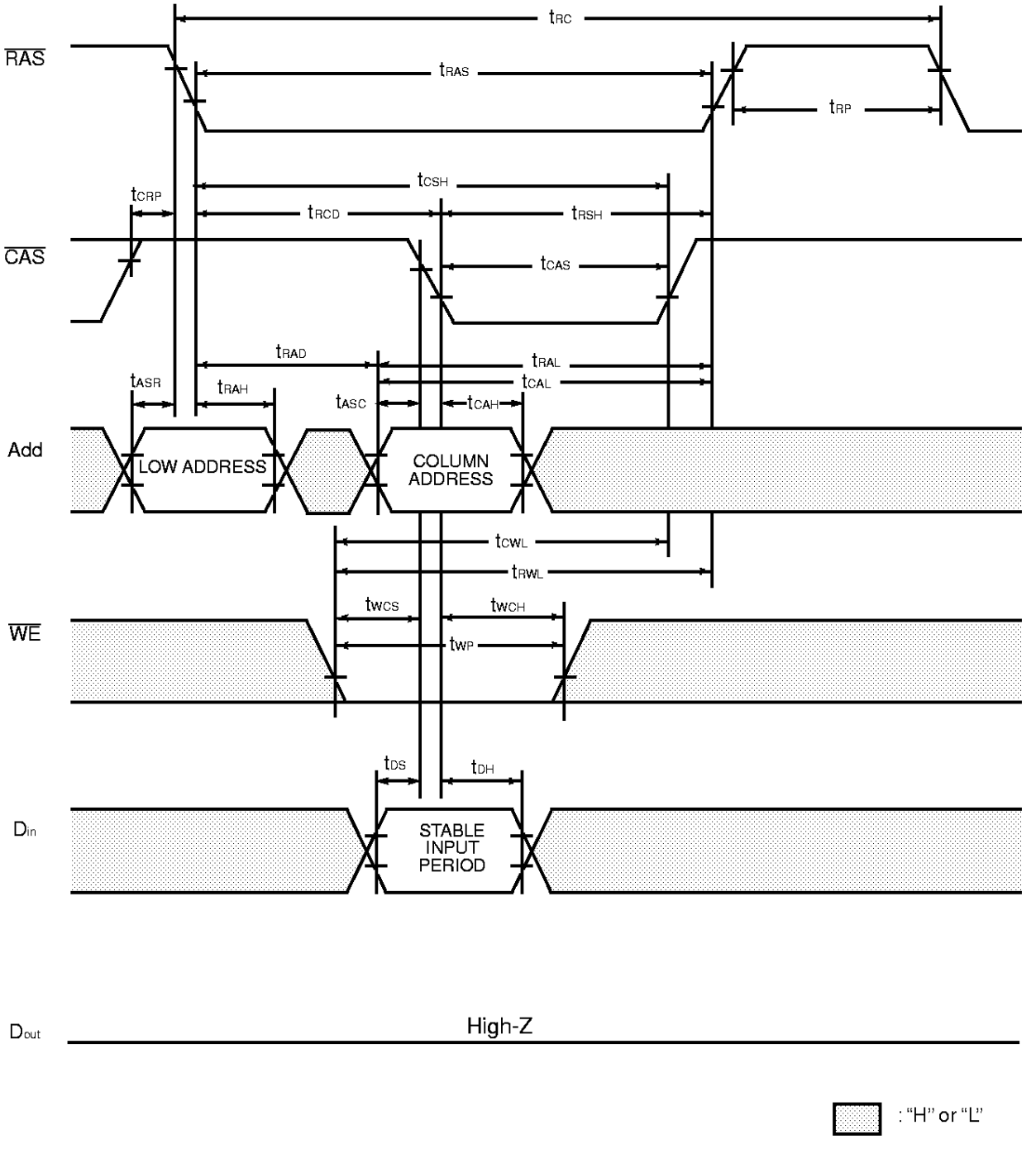
Parameter	Symbol	Series	Min.	Max.	Units
Input Capacity (A_0 to A_9, $\overline{WE}$, $\overline{CAS_0}$ to $\overline{CAS_3}$)	C_{IN1}	Common to series	—	20	pF
Input Capacity ($\overline{RAS_0}$ to $\overline{RAS_3}$)	C_{IN2}	MB98B7515,7517	—	45	pF
		MB98B7516,7518		55	pF
Input/Output Capacity (DQ_0 to DQ_7, DQ_9 to DQ_{16}, DQ_{18} to DQ_{25}, DQ_{27} to DQ_{34})	C_{DQ1}	MB98B7515,7517	—	30	pF
		MB98B7516,7518		35	pF
Input/Output Capacity (DQ_8, DQ_{17}, DQ_{26}, DQ_{35})	C_{DQ2}	MB98B7516	—	30	pF
		MB98B7518		35	pF

■ TIMING DIAGRAM

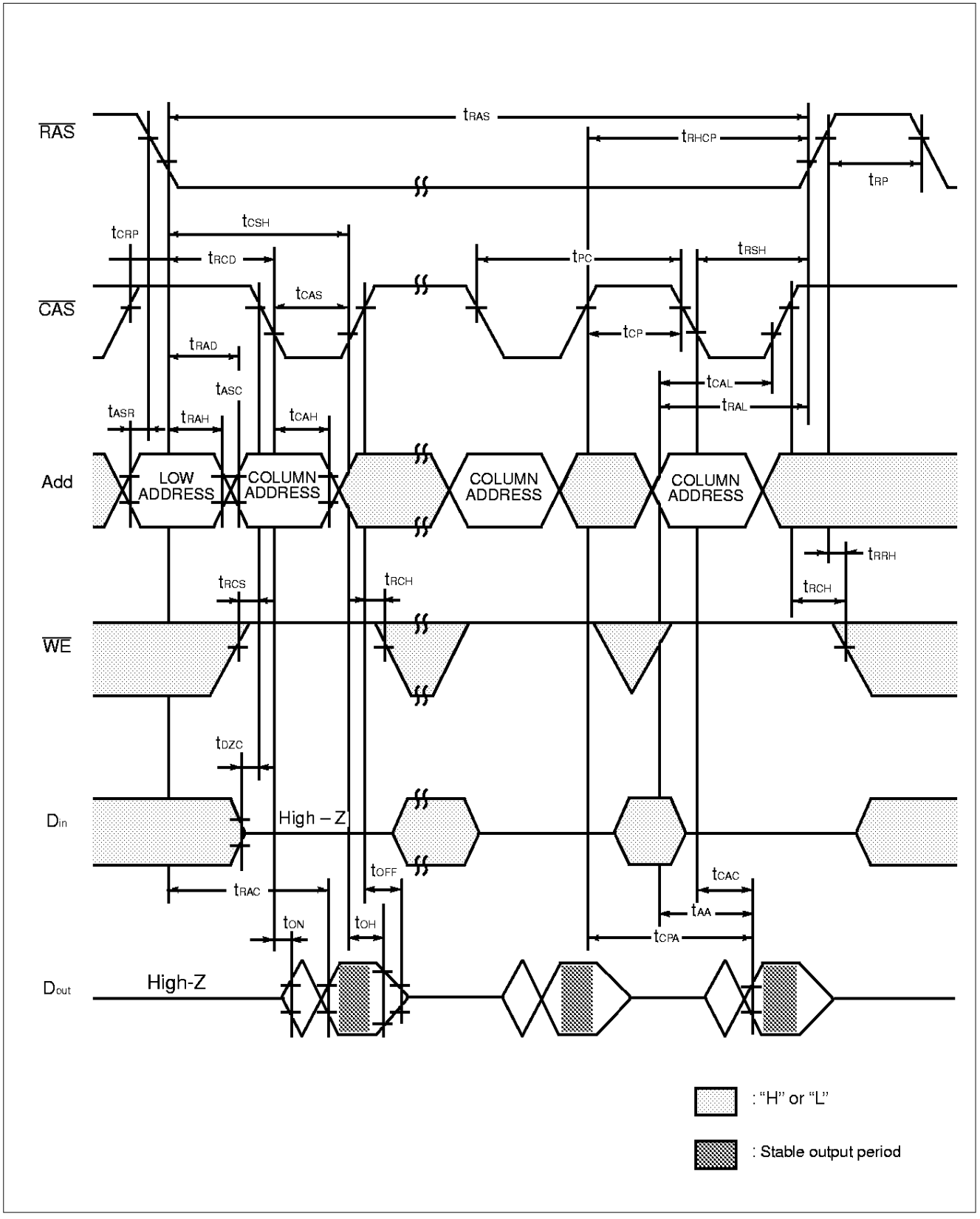
1. Read Cycle



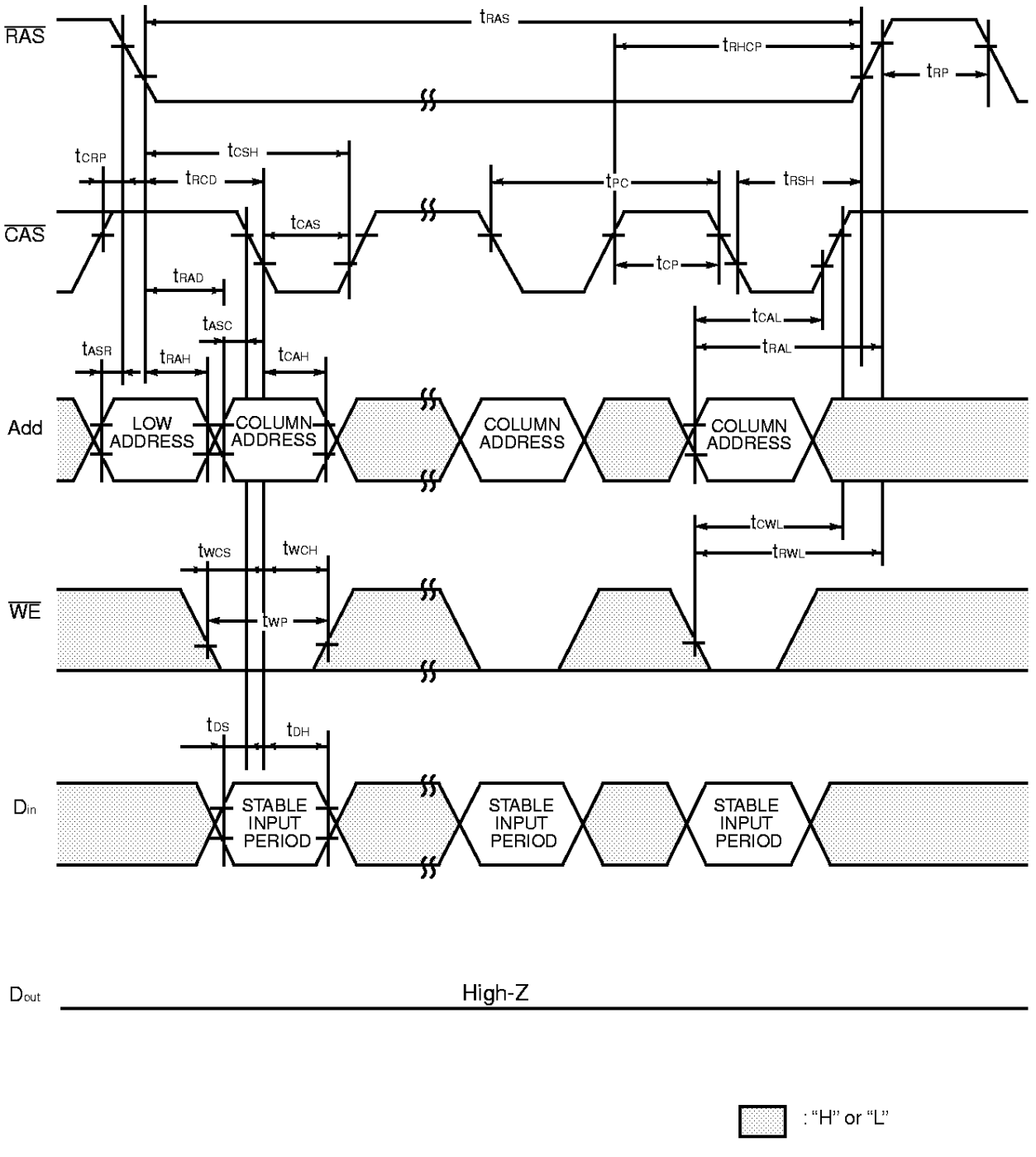
2. Write Cycle



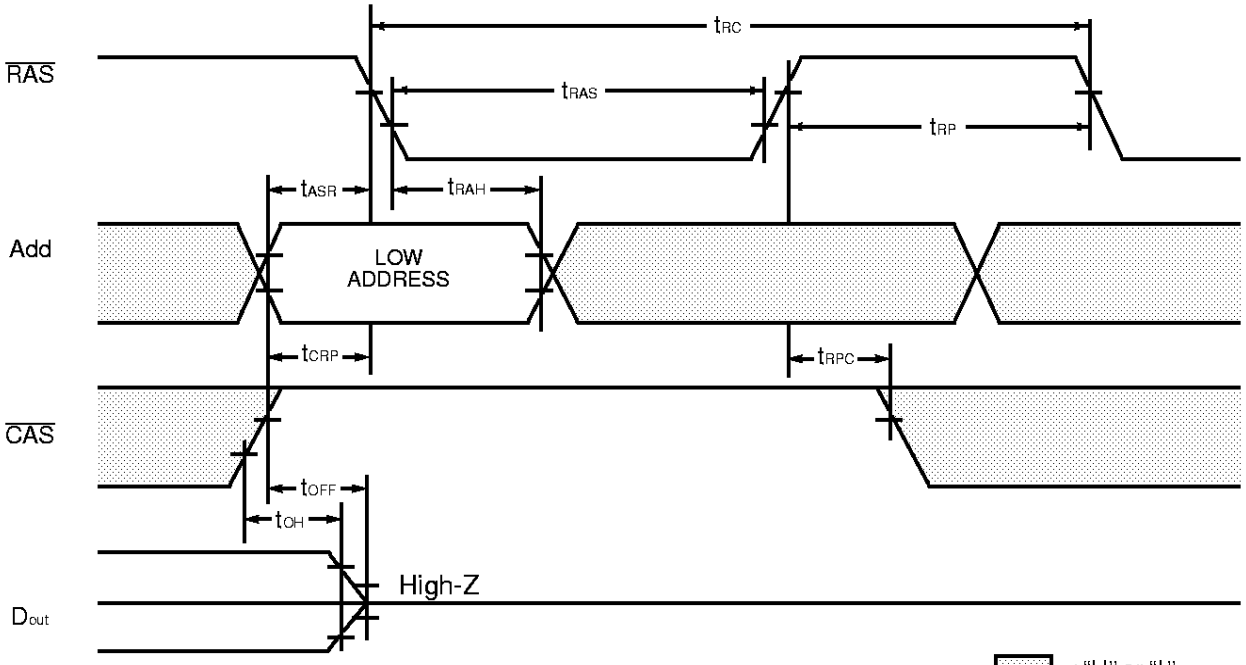
3. High-speed Page Mode Read Cycle



4. High-speed Page Mode Write Cycle

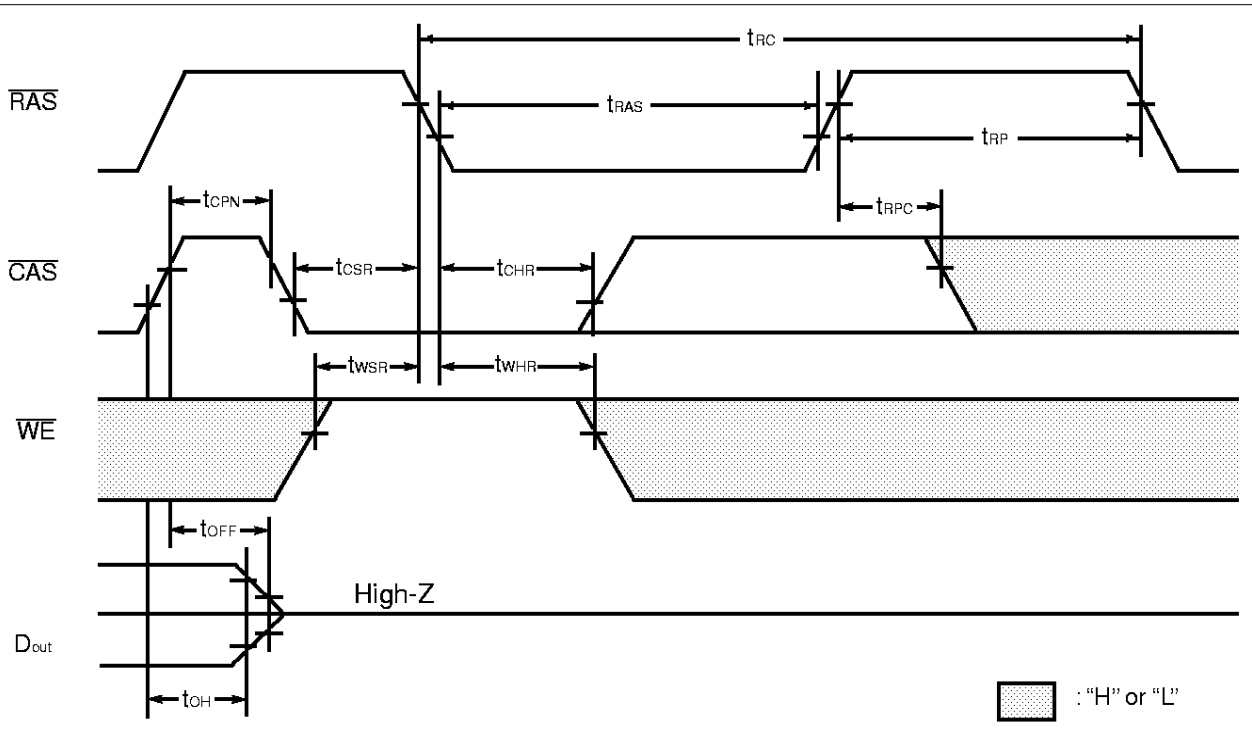


5. $\overline{RAS}$ Only Refresh Cycle



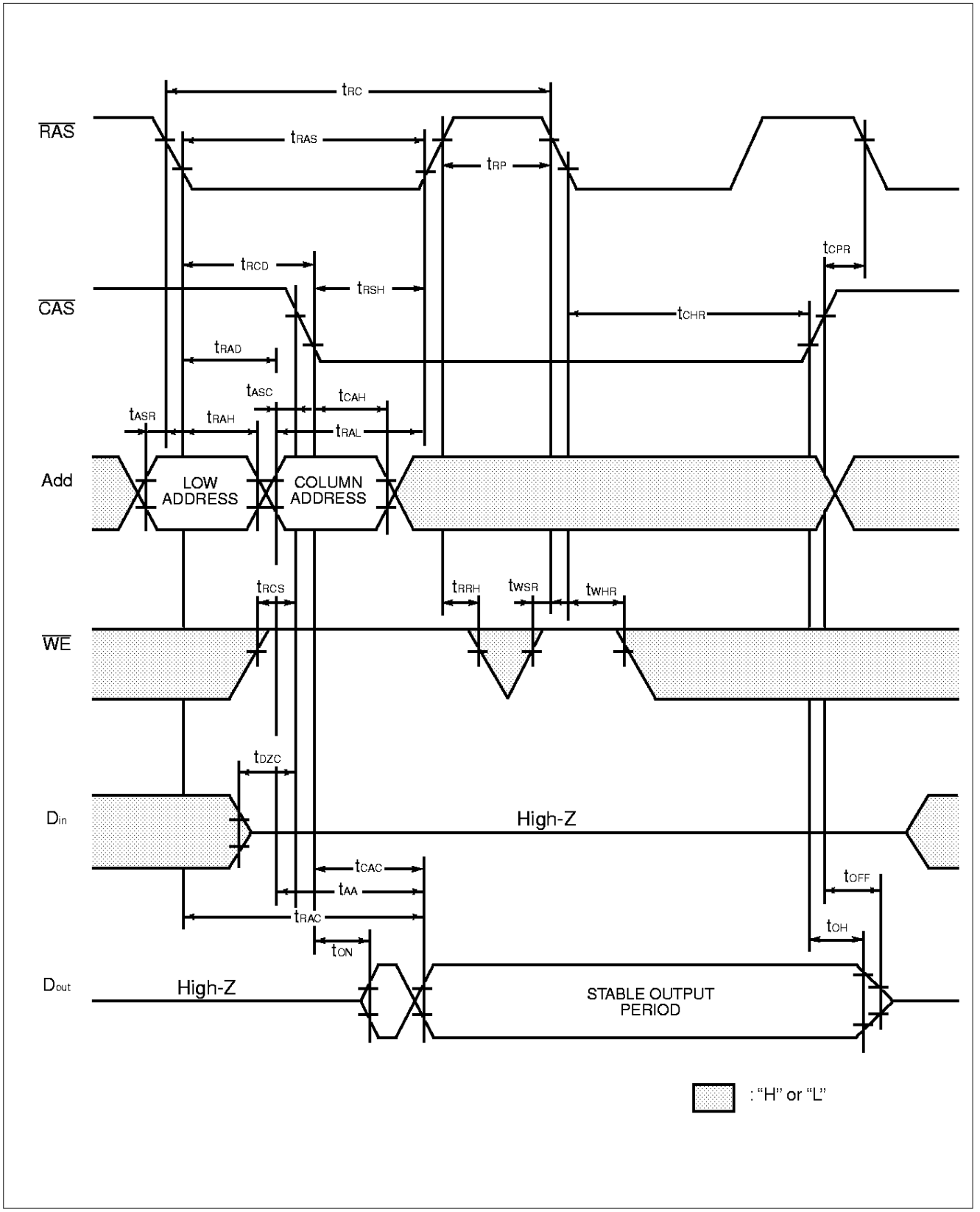
NOTE: $\overline{WE}$ is "H" or "L".

6. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



NOTE: Add is "H" or "L".

7. Hidden Refresh Cycle



■ PD PIN

1. List of Pins

Part Number \ PD pin	PD_1	PD_2	PD_3	PD_4	PD_5	PD_6	PD_7	PD_8
MB98B7515-70	GND	GND	N.C.	GND	N.C.	GND	N.C.	N.C.
MB98B7516-70								
MB98B7517-70					GND			
MB98B7518-70								
MB98B7515-80					N.C.	N.C.	GND	
MB98B7516-80								
MB98B7517-80					GND			
MB98B7518-80								

2. Functional Table

Parameters \ Part Number		MB98B7515	MB98B7516	MB98B7517	MB98B7518	
Device Class	Data	4 M × 4	4 M × 4	4 M × 4	4 M × 4	PD_1 PD_2 PD_3 PD_4
	Parity	—	4 M × 1	—	4 M × 1	
Address (quantity)	Data	11/11 Low/Column				
	Parity	11/11 Low/Column				
Number of Banks		1		2		PD_5
Access Time		70/80 ns				PD_6 PD_7
Refresh		Slow Refresh				PD_8

* : Refer to the “DRAM Card Guide Line Ver 2.0” by the JEIDA for details of PD pins.

■ LABEL INDICATION (FOR REFERENCE)

The label indication is as follows by the JEIDA specifications:

1. Label Specifications

No.	Parameter	MB98B7515	MB98B7516	MB98B7517	MB98B7518
1	Connector Type	Type A (5 V, 3.3 V)			
2	Address Area	4 M words		8 M words	
3	Bit Width	32 bits	36 bits	32 bits	36 bits
4	Circuit Configuration	RAS/CAS = 2/4		RAS/CAS = 4/4	
5	Address Composition	ROW/COL = 11/11			
6	Access Time	t_{RAC} = 80 ns			
7	Refresh Type	Slow Refresh			
8	Operation Mode	High-speed Page Mode			
9	Supply Voltage	V_{CC} = 5 V			
10	Expansion PD Pin	Not Applicable			

2. Label Format

MB98B7515 • • • □ 016M32R2C4A0 – 08 F0 P 5 □
MB98B7516 • • • □ 016M36R2C4A0 – 08 F0 P 5 □
MB98B7517 • • • □ 032M32R4C4A0 – 08 F0 P 5 □
MB98B7518 • • • □ 032M36R4C4A0 – 08 F0 P 5 □

*: □ * is blank.

(1) (2) (3) (4) (5) (6) (7) (8)(9)(10)

* : Refer to the “DRAM Card Guide Line Ver 2.0” by the JEIDA for details Label Specifications.

■ DEVICE HANDLING PRECAUTIONS

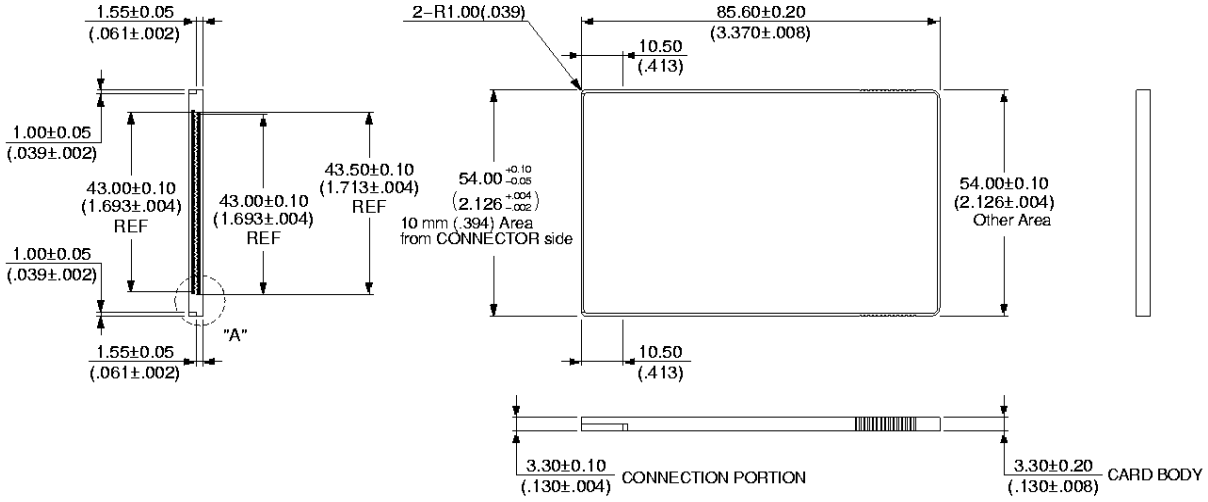
This device in composed of fine electronic parts, so take care in handling or keeping it as below.

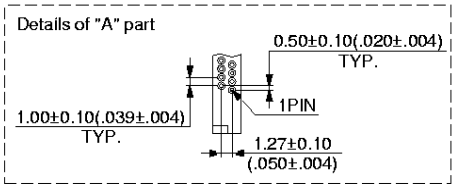
- The card is made fine, so do not keep it in the high temperature nor high humidity, place line in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

■ PACKAGE DIMENSIONS

88-pin DRAM Card
(CRD-88P-M01)

Note: Dimensions conform with JEIDA DRAM CARD Ver.2.0.





Dimensions in mm (inches)

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