HARRIS

# 2N6790

## N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

### Features

- 3.5A, 200V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

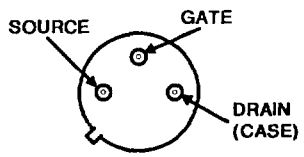
### Description

The 2N6790 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6790 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

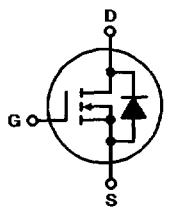
### Package

TO-205AF
BOTTOM VIEW




### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE




4 N-CHANNEL POWER MOSFETs

### Absolute Maximum Ratings ($T_C$ = +25°C) Unless Otherwise Specified

| | | 2N6790 | UNITS |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 200* | V |
| Drain-Gate Voltage ($R_{GS}$ = 20kΩ) | $V_{DGR}$ | 200* | V |
| Continuous Drain Current | | | |
| $T_C$ = +25°C | $I_D$ | 3.5* | A |
| $T_C$ = +100°C | $I_D$ | 2.25* | A |
| Pulsed Drain Current | $I_{DM}$ | 14* | A |
| Gate-Source Voltage | $V_{GS}$ | ±20* | V |
| Continuous Source Current (Body Diode) | $I_S$ | 3.5* | A |
| Pulse Source Current (Body Diode) (Note 2) | $I_{SM}$ | 14* | A |
| Maximum Power Dissipation | | | |
| $T_C$ = +25°C (See Figure 14) | $P_D$ | 20* | W |
| Above $T_C$ = +25°C, Derate Linearly (See Figure 14) | | 0.16* | W/°C |
| Inductive Current, Clamped (L = 100μH) | $I_{LM}$ | 14 | A |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{STG}$ | -55 to +150* | °C |
| Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) | $T_L$ | 300* | °C |

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.



File Number 1900.1

## Electrical Characteristics @ $T_C$ = 25°C (Unless Otherwise Specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain - Source Breakdown Voltage | 200* | – | – | V | $V_{GS}$ = 0V, $I_D$ = 0.25 mA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0* | – | 4.0* | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA |
| $I_{GSS}$ | Gate - Source Leakage Forward | – | – | 100* | nA | $V_{GS}$ = 20V, $V_{DS}$ = 0V |
| $I_{GSS}$ | Gate - Source Leakage Reverse | – | – | 100* | nA | $V_{GS}$ = −20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | – | – | 250* | μA | $V_{DS}$ = 200V, $V_{GS}$ = 0V |
| | | – | – | 1000* | μA | $V_{DS}$ = 160V, $V_{GS}$ = 0V, $T_C$ = 125°C |
| $V_{DS(on)}$ | On-State Voltage[a] | – | – | 2.8* | V | $V_{GS}$ = 10V, $I_D$ = 3.5A |
| $R_{DS(on)}$ | Static Drain-Source On-State Resistance[a] | – | 0.50 | 0.80* | Ω | $V_{GS}$ = 10V, $I_D$ = 2.25A, $T_A$ = 25°C |
| | | – | – | 1.50* | Ω | $V_{GS}$ = 10V, $I_D$ = 2.25A, $T_A$ = 125°C |
| $V_{SD}$ | Diode Forward Voltage[a] | 0.7* | – | 1.5* | V | $T_C$ = 25°C, $I_S$ = 3.5A, $V_{GS}$ = 0V |
| $g_{fs}$ | Forward Transconductance[a] | 1.5* | 2.25 | 4.5* | S(℧) | $V_{DS}$ = 5V, $I_D$ = 2.25A |
| $C_{iss}$ | Input Capacitance | 200* | 450 | 600* | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1.0 MHz |
| $C_{oss}$ | Output Capacitance | 60* | 150 | 300* | pF | See Fig. 10 |
| $C_{rss}$ | Reverse Transfer Capacitance | 15* | 40 | 80* | pF | |
| $t_{d(on)}$ | Turn-On Delay Time | – | – | 40* | ns | $V_{DD}$ ≅ 74V, $I_D$ = 2.25A, $Z_o$ = 50Ω |
| $t_r$ | Rise Time | – | – | 50* | ns | See Fig. 15 |
| $t_{d(off)}$ | Turn-Off Delay Time | – | – | 50* | ns | (MOSFET switching times are essentially independent |
| $t_f$ | Fall Time | – | – | 50* | ns | of operating temperature.) |
| SOA | Safe Operating Area | 20 | – | – | W | $V_{DS}$ = 160V, $I_D$ = 125 mA, See Fig. 16. |
| | | 20 | – | – | W | $V_{DS}$ = 5.7V, $I_D$ = 3.5A, See Fig. 16. |

## Thermal Resistance

| | | | | | | |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | – | – | 6.25* | °C/W | |
| $R_{thJA}$ | Junction-to-Ambient | – | – | 175 | °C/W | Free Air Operation |

## Source-Drain Diode Switching Characteristics (Typical)

| | | | | |
|---|---|---|---|---|
| $t_{rr}$ | Reverse Recovery Time | 350 | ns | $T_J$ = 150°C, $I_F$ = 3.5A, $dI_F/dt$ = 100A/μs |
| $Q_{RR}$ | Reverse Recovered Charge | 2.3 | μC | $T_J$ = 150°C, $I_F$ = 3.5A, $dI_F/dt$ = 100A/μs |
| $t_{on}$ | Forward Turn-on Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | |

*JEDEC registered value

aPulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

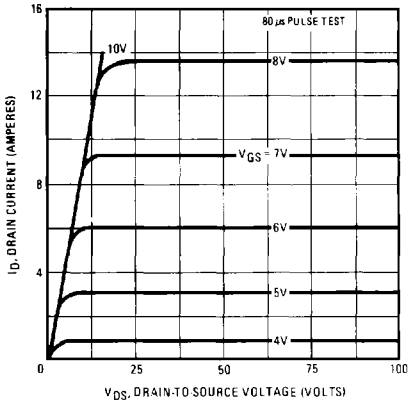



*Fig. 1 - Typical output characteristics.*

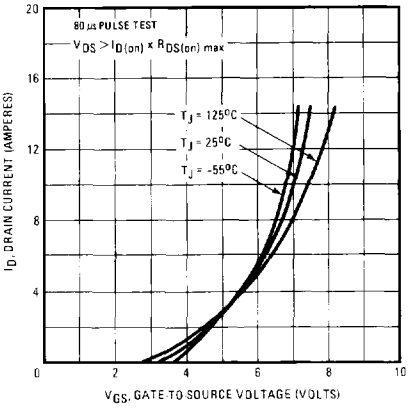



*Fig. 2 - Typical transfer characteristics.*

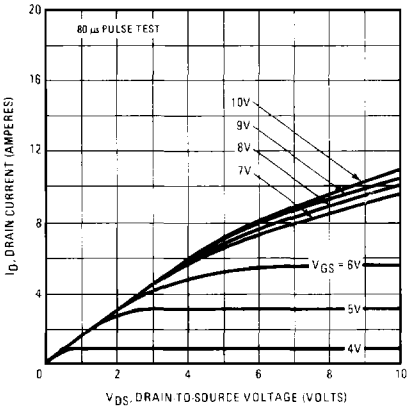



*Fig. 3 - Typical saturation characteristics.*

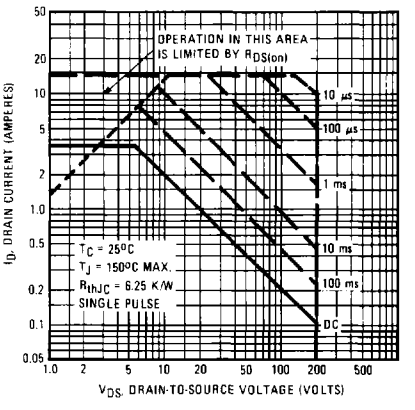



*Fig. 4 - Maximum safe operating area.*



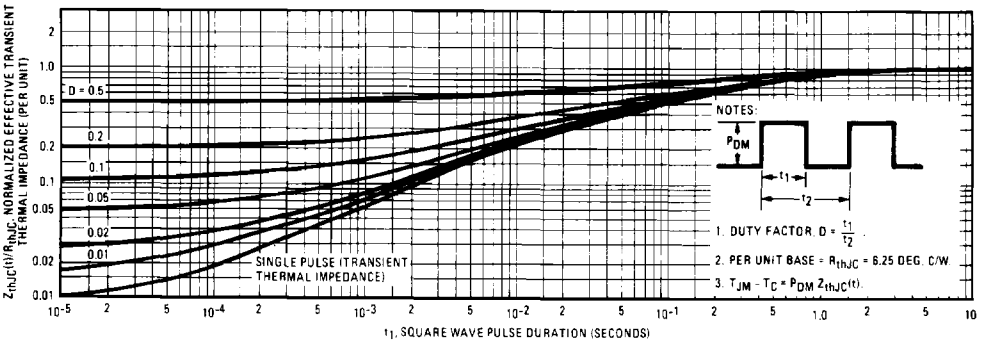



*Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.*

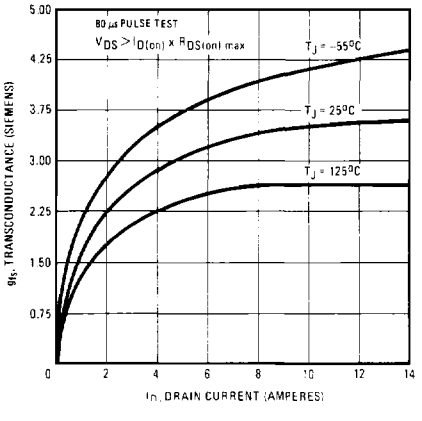



*Fig. 6 - Typical transconductance versus drain current.*

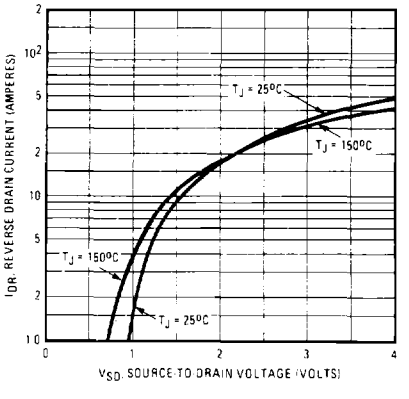



*Fig. 7 - Typical source-drain diode forward voltage.*

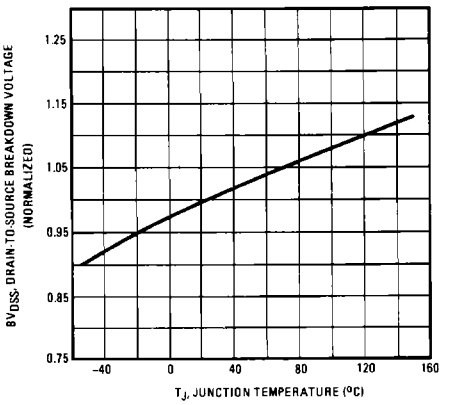



*Fig. 8 - Breakdown voltage versus temperature.*

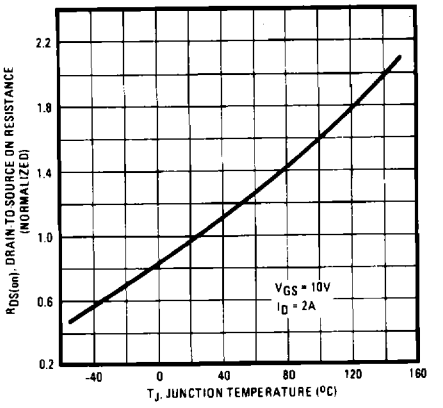



*Fig. 9 - Typical normalized on-resistance versus temperature.*

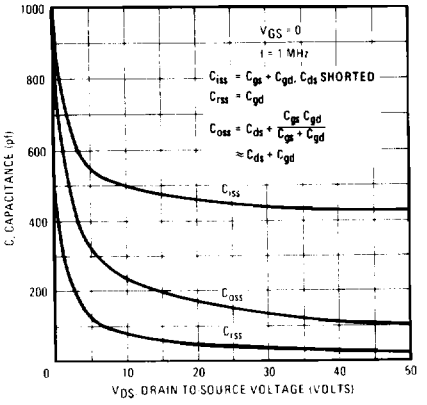



*Fig. 10 - Typical capacitance versus drain-to-source voltage.*

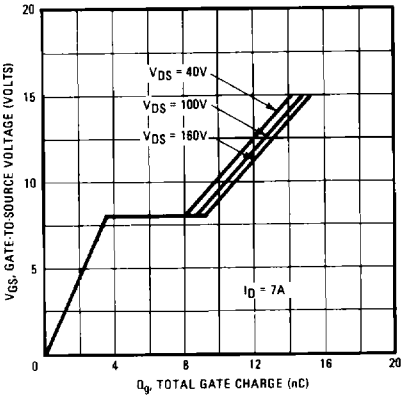



*Fig. 11 - Typical gate charge versus gate-to-source voltage.*

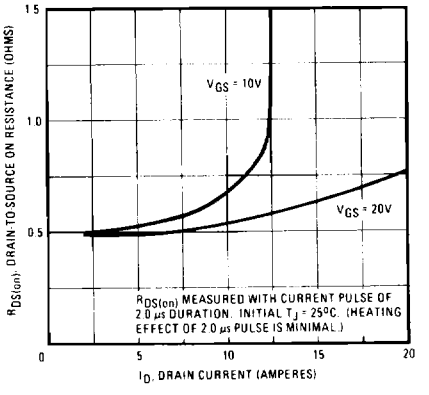



*Fig. 12 - Typical on-resistance versus drain current.*

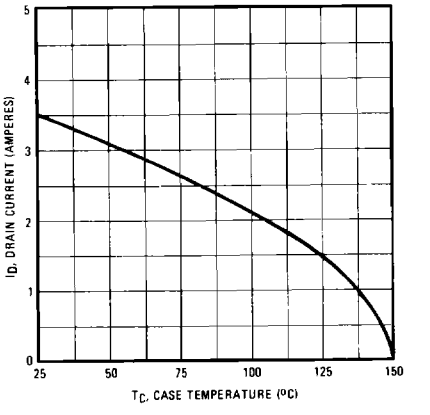



*Fig. 13 - Maximum drain current versus case temperature.*

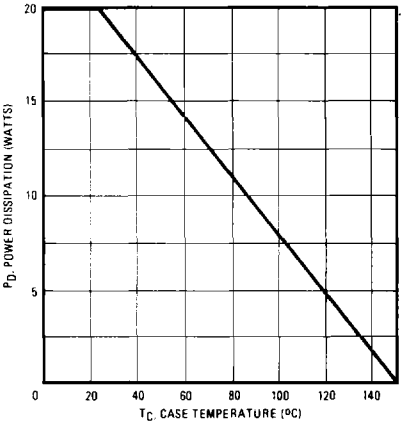
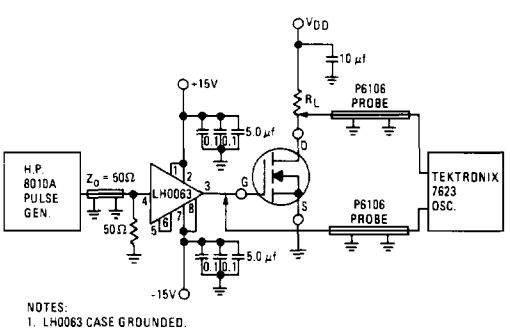
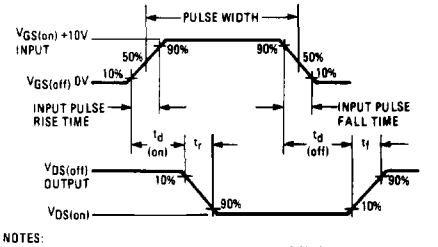



*Fig. 14 - Power versus temperature derating curve.*



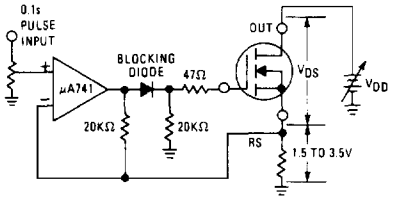



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.




NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

*Fig. 15 - Switching time test circuit.*




NOTES:
1. SET $V_{DS}$ TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE $V_{GS}$ UNTIL THE SPECIFIED VALUE OF $I_D$ AND $V_{DS}$ ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT $R_S$ SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

*Fig. 16 - Safe operating area test circuit.*