PMC
PMC-SIERRA

November 21, 2006

Notice – PMC Product Support Scope for Specified HDMP Part Numbers

Distribution:

This notice has been added to the front of the datasheets for the “Devices Affected” listed below.

Description:

PMC-Sierra has acquired the Fibre Channel/Storage and Gigabit Ethernet Port Bypass Controllers and SERDES/PHY products of Agilent/Avago Technologies. This notice is to inform customers that PMC-Sierra is supporting these devices for existing production designs only. PMC-Sierra will only provide support for the migration of an existing design from a Pb package to a Pb-free package. The devices are not intended for new designs and PMC-Sierra will not provide support for new designs.

Devices Affected:

Device	Data Sheet	Device	Data Sheet	Device	Data Sheet
HDMP-0421G	PMC-2060481*	HDMP-1022G	PMC-2060487	HDMP-1638G	PMC-2060490
HDMP-0422G	PMC-2060482*	HDMP-1024G	PMC-2060487	HDMP-1646AG	PMC-2060491
HDMP-0450G	PMC-2060483	HDMP-1032AG	PMC-2060488	HDMP-1646AGR1	PMC-2060491
HDMP-0451G	PMC-2060484	HDMP-1034AG	PMC-2060488	HDMP-1687G	PMC-2060493
HDMP-0452G	PMC-2060485*	HDMP-1536AG	PMC-2060489	HDMP-T1636AG	PMC-2060491
HDMP-0480G	PMC-2062505*	HDMP-1636AG	PMC-2060491		
HDMP-0482G	PMC-2060486	HDMP-1636AGR1	PMC-2060491		

* Note – These data sheets have part numbers that reference Pb packaging. All part numbers listed above are for Pb-free packaging.

Customer Response

This notice is for customer information only and no customer response is required. If you have any questions or concerns please contact your local PMC-Sierra Sales Representative listed at this link http://www.pmc-sierra.com/contactSales/

Agilent HDMP-0480
Octal Cell Port Bypass Circuit
without Clock and Data Recovery
Data Sheet

Description
The HDMP-0480 is an Octal Cell Port Bypass Circuit (PBC). This device minimizes part count, cost and jitter accumulation. Port Bypass Circuits are used in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. By using Port Bypass Circuits, hard disks may be pulled out or swapped while other disks in the array are available to the system.

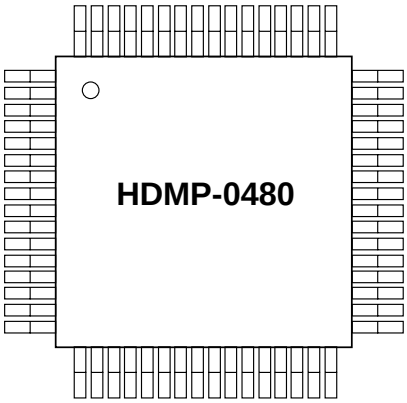
A Port Bypass Circuit (PBC) consists of multiple 2:1 multiplexers daisy chained along with a CDR. Each port has two modes of operation: “disk in loop” and “disk by-passed”. When the “disk in loop” mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0480’s TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC’s (e.g. an HDMP-1636A) Rx± differential input pins. Data from the Disk Drive Transceiver IC’s Tx± differential outputs goes to the HDMP- 0480’s FM_NODE[n]± differential input pins. When the “disk bypassed” mode is selected, the disk drive is either absent or non-functional and the loop bypasses the hard disk.

The “disk bypassed” mode is enabled by pulling the BYPASS[n]- pin low. Leave BYPASS[n]- floating to enable the “disk in loop” mode. HDMP-0480’s may be cascaded with other members of the HDMP-04XX/HDMP-05XX family through the FM_NODE and TO_NODE pins to accommodate any number of hard disks. The unused cells in this PBC may be bypassed by using pulldown resistors on the BYPASS[n]- pins for these cells.

An HDMP-0480 may also be used as eight 1:1 buffers. In addition, an HDMP-0480 may be configured as four 2:1 multiplexers or as four 1:2 buffers.

Features
- **Supports 1.0625 GBd fibre channel operation**
- **Supports 1.25 GBd gigabit Ethernet (GE) operation**
- **Octal cell PBC in one package**
- **Valid amplitude detection on FM_NODE[7] input**
- **Equalizers on all inputs**
- **High speed LVPECL I/O**
- **Buffered Line Logic (BLL) outputs (no external bias resistors required)**
- **0.76 W typical power at Vcc = 3.3V**
- **64 Pin, 10 mm, low cost plastic QFP package**

Applications
- **RAID, JBOD, BTS cabinets**
- **Four 2:1 muxes**
- **Four 1:2 buffers**
- **1 = > N gigabit serial buffer**
- **N = > 1 gigabit serial mux**



CAUTION: As with all semiconductor ICs, it is advised that normal static precautions be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

Agilent Technologies

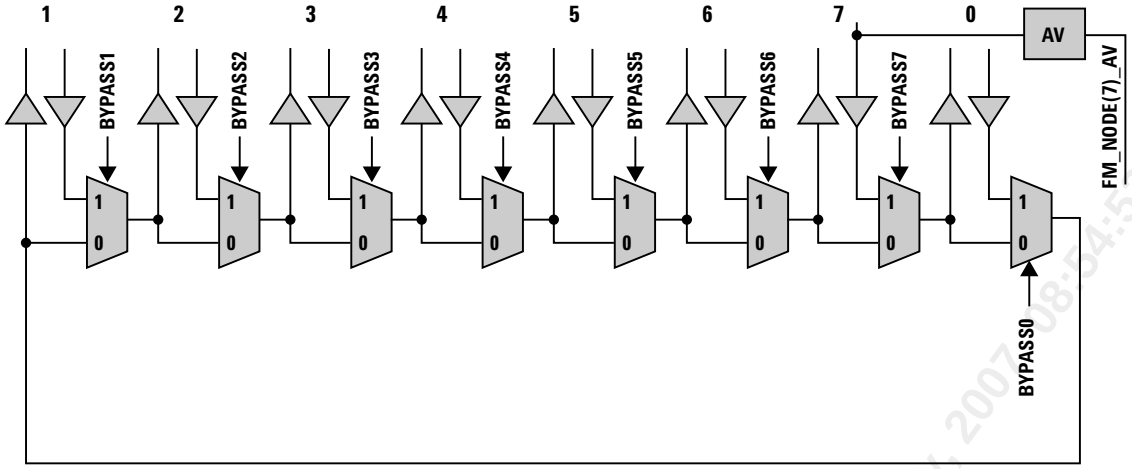


Figure 1. Block Diagram of HDMP-0480.

HDMP-0480 Block Diagram

AV Output

The Amplitude Valid (AV) block detects if the incoming data on FM_NODE[7]± is valid by examining the differential amplitude of that input. The incoming data is considered valid, and FM_NODE[7]_AV is driven high, as long as the amplitude is greater than 400 mV (differential peak-to-peak). FM_NODE[7]_AV is driven low as long as the amplitude of the input signal is less than 100 mV (differential peak-to-peak). When the amplitude of the input signal is between 100-400 mV (differential peak-to-peak), FM_NODE[7]_AV is unpredictable.

BLL Output

All TO_NODE[n]± high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination, so no external bias resistors are required. The BLL Outputs on the HDMP-0480 are of equal strength and can drive in excess of 120 inches of FR-4 PCB trace. Unused outputs should not be left unconnected. Ideally, unused outputs should have their differential pins shorted together with a short PCB trace. If transmission lines are connected to the output pins, the lines should be differentially terminated with an appropriate resistor. The value of the termination resistor should match the PCB trace differential impedance.

EQU Input

All FM_NODE[n]± high-speed differential inputs have an Equalization (EQU) buffer to offset the effects of skin loss and dispersion on PCBs. An external termination resistor is required across all high-speed inputs.

BYPASS[N]- Input

The active low BYPASS[n]- inputs control the data flow through the HDMP-0480. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]- pin should be connected to GND through a 1kΩ resistor. Otherwise, the BYPASS[n]- inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

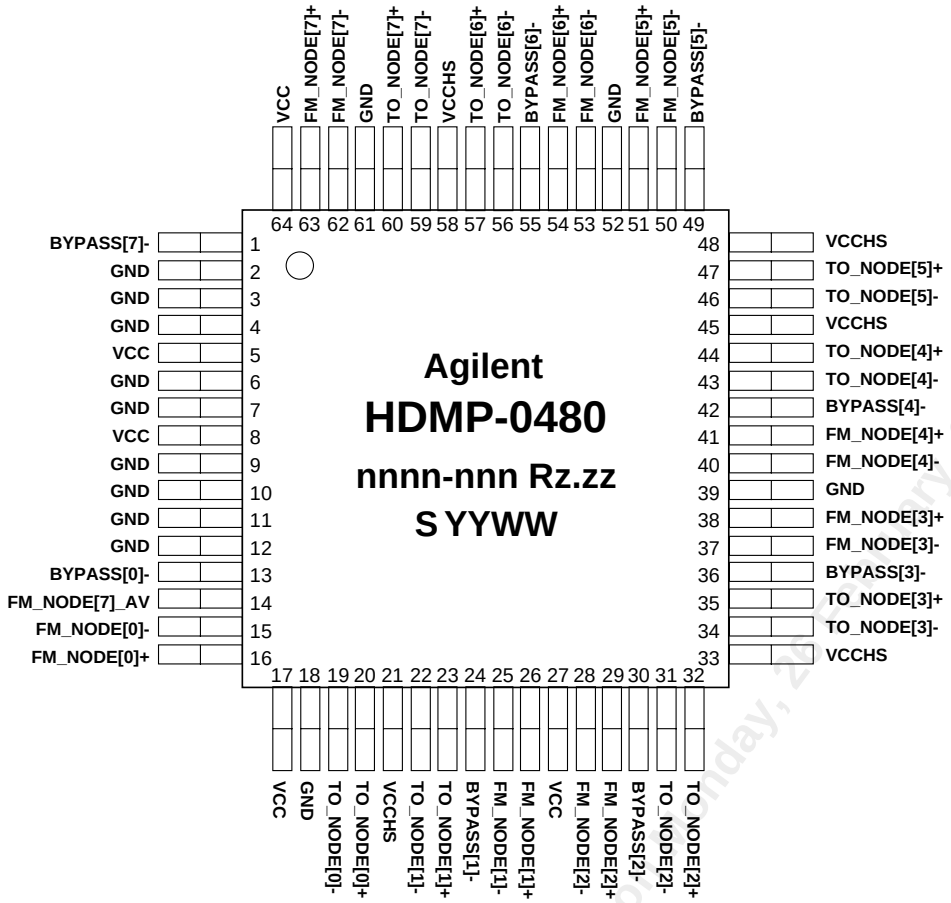


Figure 2. HDMP-0480 Package Layout and Marking, Top View.
nnnn-nnn = wafer lot - build number; Rz.zz = Die Revision; S = Supplier Code; YYWW = Date Code (YY = year, WW = work week); COUNTRY = country of manufacture (on back side).

I/O Type Definitions

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High Speed Output, LVPECL Compatible
HS_IN	High Speed Input
C	External circuit node
S	Power supply or ground

Table 1. Pin Definitions for HDMP-0480.

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+	20	HS_OUT	**Serial Data Outputs**: High-speed outputs to a hard disk drive or to a cable input.
TO_NODE[0]-	19		
TO_NODE[1]+	23		
TO_NODE[1]-	22		
TO_NODE[2]+	32		
TO_NODE[2]-	31		
TO_NODE[3]+	35		
TO_NODE[3]-	34		
TO_NODE[4]+	44		
TO_NODE[4]-	43		
TO_NODE[5]+	47		
TO_NODE[5]-	46		
TO_NODE[6]+	57		
TO_NODE[6]-	56		
TO_NODE[7]+	60		
TO_NODE[7]-	59		
FM_NODE[0]+	16	HS_IN	**Serial Data Inputs**: High-speed inputs from a hard disk drive or from a cable output.
FM_NODE[0]-	15		
FM_NODE[1]+	26		
FM_NODE[1]-	25		
FM_NODE[2]+	29		
FM_NODE[2]-	28		
FM_NODE[3]+	38		
FM_NODE[3]-	37		
FM_NODE[4]+	41		
FM_NODE[4]-	40		
FM_NODE[5]+	51		
FM_NODE[5]-	50		
FM_NODE[6]+	54		
FM_NODE[6]-	53		
FM_NODE[7]+	63		
FM_NODE[7]-	62		
BYPASS[0]-	13	I-LVTTL	**Bypass Inputs**: For “disk bypassed” mode, connect BYPASS[n]- to GND through a1k resistor. For “disk in loop” mode, float HIGH.
BYPASS[1]-	24		
BYPASS[2]-	30		
BYPASS[3]-	36		
BYPASS[4]-	42		
BYPASS[5]-	49		
BYPASS[6]-	55		
BYPASS[7]-	1		
FM_NODE[7]_AV	14	O-LVTTL	**Amplitude Valid**: Indicates acceptable signal amplitude on the FM_NODE[7]± inputs. If (FM_NODE[7]+ - FM_NODE[7]-) >= 400 mV peak-to-peak, FM_NODE[7]_AV = 1 If 400 mV > (FM_NODE[7]+ - FM_NODE[7]-) > 100 mV, FM_NODE[7]_AV = unpredictable If 100 mV >= (FM_NODE[7]+ - FM_NODE[7]-), FM_NODE[7]_AV = 0

Table 1 is continued on next page.

Table 1. Pin Definitions for HDMP-0480, continued

Pin Name	Pin	Pin Type	Pin Description
GND	2 3 4 6 7 9 10 11 12 18 39 52 61	S	**Ground**: Normally 0 volts. See Figure 7 for Recommended Power Supply Filtering.
VCCHS[0,1] VCCHS[2,3] VCCHS[4] VCCHS[5] VCCHS[6,7]	21 33 45 48 58	S	**High Speed Supply**: Normally 3.3 volts. Used only for high-speed outputs (TO_NODE[n]). See Figure 7 for Recommended Power Supply Filtering.
VCC	5 8 17 27 64	S	**Logic Power Supply**: Normally 3.3 volts. Used for internal logic. See Figure 7 for Recommended Power Supply Filtering.

HDMP-0480 Absolute Maximum Ratings

T_a=25°C, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device. T_a refers to the ambient temperature for the board upon which the parametric measurements were taken.

Symbol	Parameters	Units	Min.	Max.
V_{CC}	Supply Voltage	V	-0.7	4.0
$V_{IN, LVTTL}$	LVTTL Input Voltage	V	-0.7	4.0
V_{IN, HS_IN}	HS_IN Input Voltage	V	1.3	V_{CC}
$I_{O, LVTTL}$	LVTTL Output Voltage	mA		±13
T_{stg}	Storage Temperature	°C	-65	+150
T_j	Junction Temperature	°C	0	+125

HDMP-0480 Guaranteed Operating Rates, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Serial Clock Rate FC (MBd)		Serial Clock Rate GE (MBd)	
Min.	Max.	Min.	Max.
1,040	1,080	1,240	1,260

HDMP-0480 DC Electrical Specifications, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameters	Min.	Typ.	Max.	Units
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	2.0		4.0	V
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	0		0.8	V
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = -400 µA	2.2		3.45	V
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	0		0.6	V
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4V, V_{CC} = 3.45V		.003	40	µA
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4V, V_{CC} = 3.45V		300	600	µA
I_{CC}	Total Supply Current, T_a = 25°C		230	280	mA

HDMP-0480 AC Electrical Specifications, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{loop}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]		0.9	2.0	ns
t_{cell}	Per Cell Latency from FM_NODE[7] to TO_NODE[0]		0.5	0.8	ns
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8V to 2.0V		2		ns
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0V to 0.8V		2		ns
t_{rs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20%-80%		200	350	ps
t_{fs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20%-80%		200	350	ps
t_{rd,HS_OUT}	HS_OUT Differential Rise Time, 20%-80%		200	350	ps
t_{fd,HS_OUT}	HS_OUT Differential Rise Time, 20%-80%		200	350	ps
V_{IP,HS_IN}	HS_IN Input Peak to Peak Required Differential Voltage Range	200	1200	2000	mV
V_{OP,HS_OUT}	HS_OUT Output Pk-Pk Diff. Voltage Range (Z0 = 75Ω, Fig. 5)	1100	1400	2000	mV

HDMP-0480 Power Dissipation, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameters	Unit	Typ.	Max.
P_D	Power Dissipation	mW	760	970

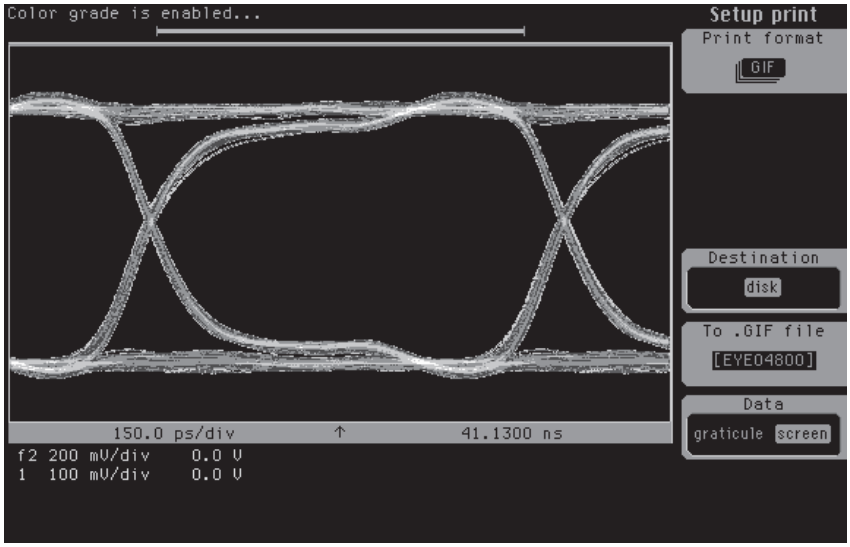


Figure 3. Eye Diagram of TO_NODE[1]± High Speed Differential Output.

Note: Measurement taken with a 2^7-1 PRBS input to FM_NODE[0]±.

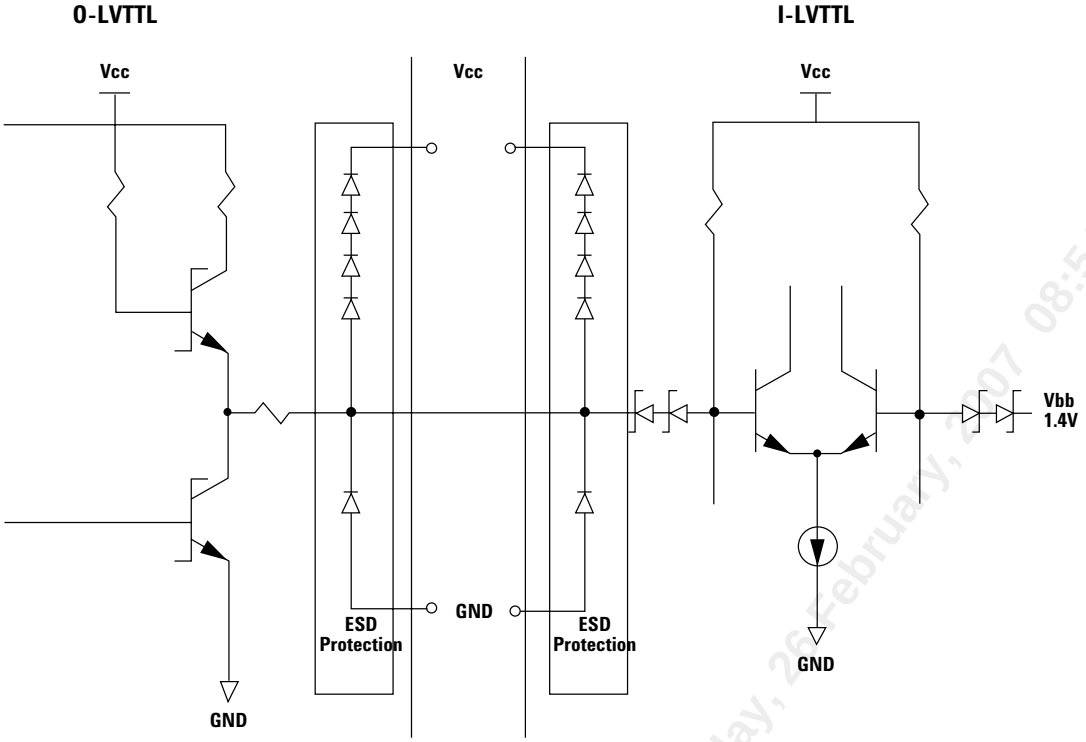


Figure 4. O-LVTTL and I-LVTTL Simplified Circuit Schematic.

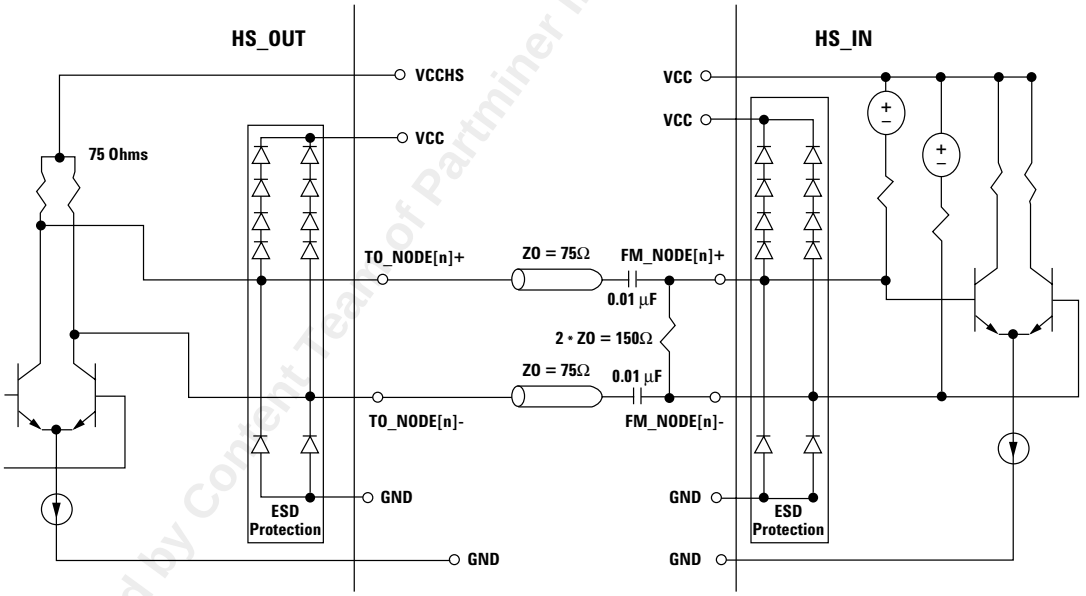


Figure 5. HS_OUT and HS_IN Simplified Circuit Schematic.

Note: FM_NODE[n] inputs should never be connected to ground as permanent damage to the device may result.

Package Information

HDMP-0480 Thermal Characteristics, $T_C = 0°C$ to $+85°C$, $V_{CC} = 3.15V$ to $3.45V$

Symbol	Parameter	Unit	Typ.	Max.
θ_{jc}	Thermal Resistance, Junction to Case	°C/W	10	—

Note: Based on independent testing by Agilent. θ_{ja} for these devices is 56°C/W for the HDMP-0480. θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following equation: $T_j = T_C + (\theta_{jc} \times P_D)$, where T_C is the case temperature measured on the top center of the package, and P_D is the power being dissipated.

Item	Details
Package Material	Plastic
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	300–800 micro-inches
Lead Skew	0.08 mm max.
Lead Coplanarity (Seating Plane Method)	0.08 mm max.

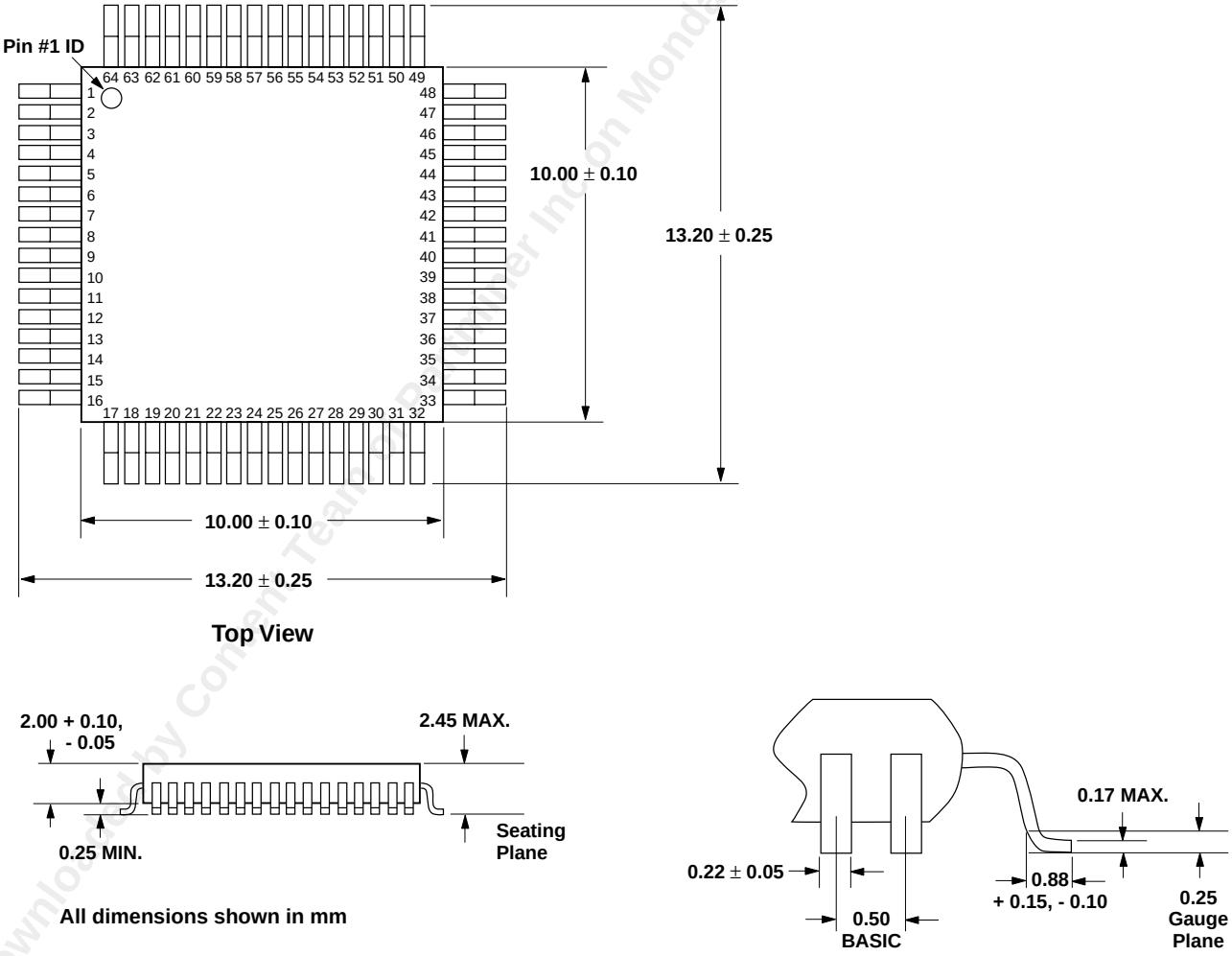


Figure 6. HDMP-0480 Package Drawing.

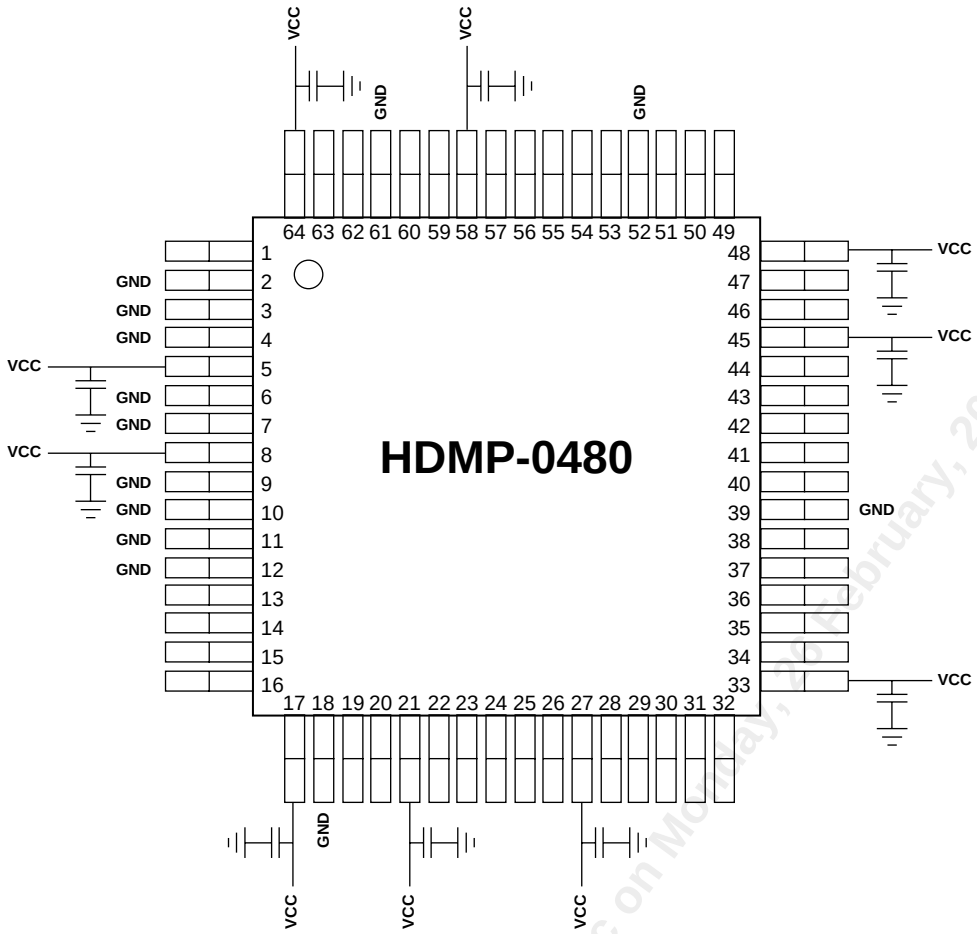


Figure 7. Recommended Power Supply Filtering. Capacitors = 0.1 µF.

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