

96-BIT AC-PDP DRIVER

DESCRIPTION

The μ PD16342 is a high withstand voltage CMOS driver designed for use with a flat display panel such as a PDP, VFD, or EL panel. It consists of a 96-bit bi-directional shift register, 96-bit latch and high withstand voltage CMOS driver. The logic block operates with a 5-V power supply interface (CMOS level input) so that it can be directly connected to a gate array and CPU. The driver block provides a high withstand voltage output: 80 V, +15/-30 mA MAX. The logic and driver blocks are made of CMOS circuits, consuming lower power.

FEATURES

- Circuit configuration switched by the IBS pin between three 32-bit bi-directional shift registers and six 16-bit bi-directional shift registers.
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{MAX.} = 40$ MHz MIN. at data latch)
($f_{MAX.} = 25$ MHz MIN. at cascade connection)
- High withstand output voltage (80 V, +15/-30 mA MAX.)
- High withstand voltage CMOS structure

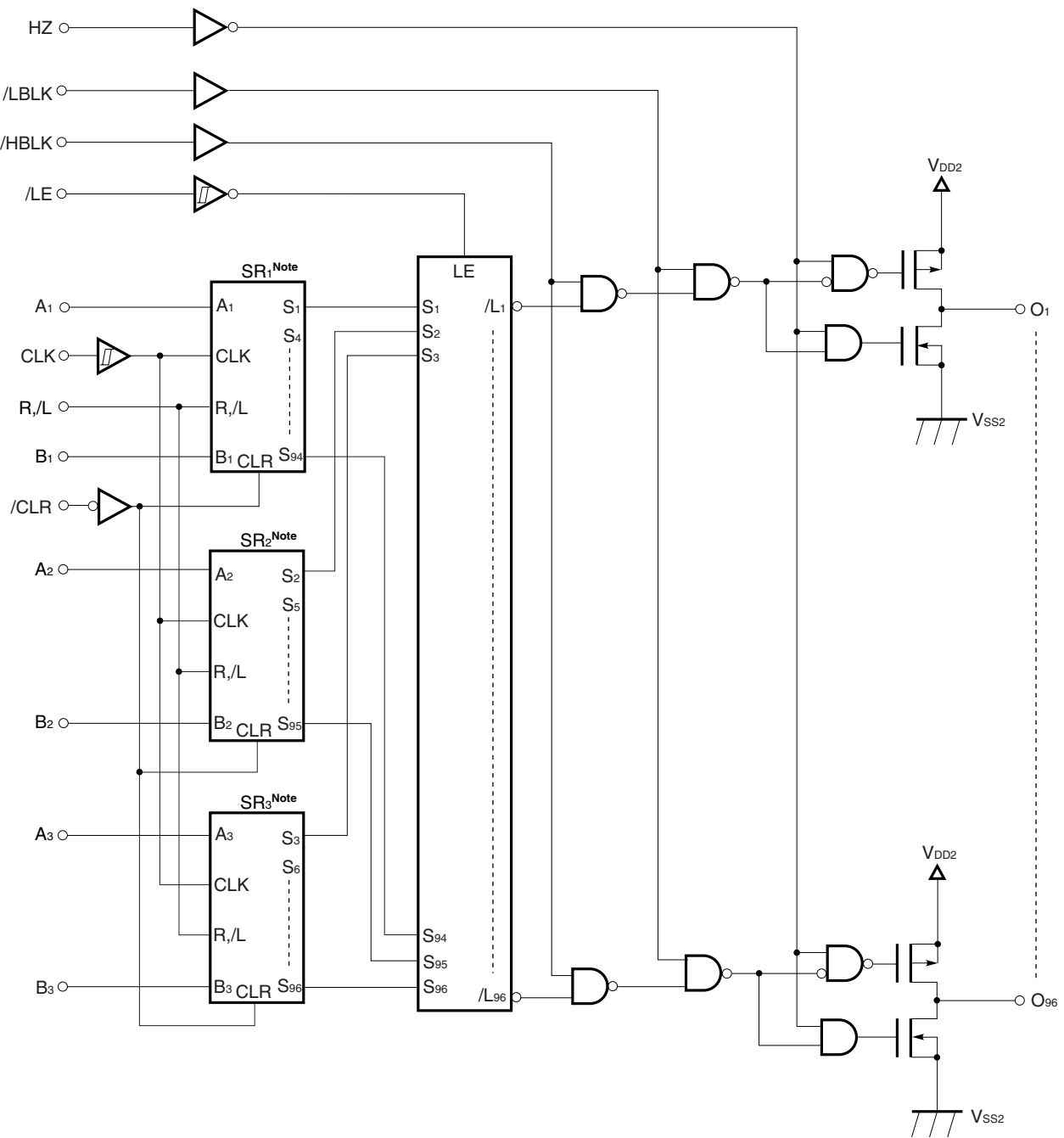
ORDERING INFORMATION

| Part Number | Package |
|---------------|------------|
| μ PD16342 | Module/TCP |

Remark Consult an our sales representative regarding the module. Since the module characteristics is based on the module specifications, there may be differences between the contents written in this document and real characteristics.

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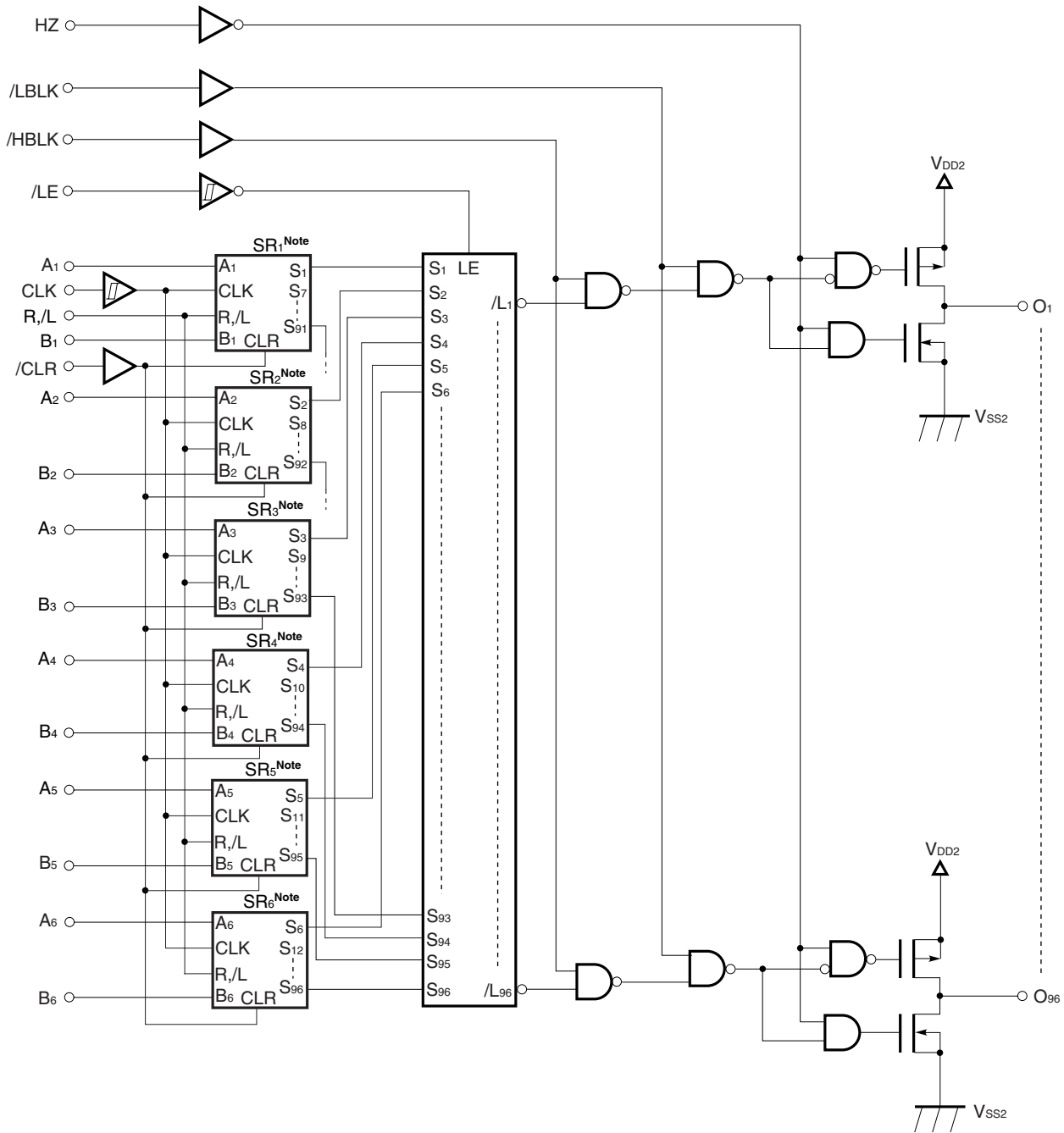
★ 1. BLOCK DIAGRAM (1) (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



Note SR_n: 32-bit shift register

Remark /xxx indicates active low signal.

1. BLOCK DIAGRAM (2) (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



Note SR_n: 16-bit shift register

2. PIN FUNCTIONS

| Symbol | Pin Name | I/O | Description |
|-------------------------------------|------------------------|---------------------|--|
| /LBLK | Low blanking | Input | /LBLK = L: All output = L |
| /HBLK | High blanking | Input | /HBLK = L: All output = H |
| /LE | Latch enable | Input | Latch on a falling edge |
| HZ | Output high impedance | Input | H: All output set to the high-impedance state |
| /CLR | Register clear | Input | L: All shift register data cleared to the L level |
| A ₁ to A ₃₍₆₎ | RIGHT data | I/O ^{Note} | R,/L = H, A ₁ to A ₃₍₆₎ : Input, B ₁ to B ₃₍₆₎ : Output The parenthesized pins are used in 6-bit input mode. |
| B ₁ to B ₃₍₆₎ | LEFT data | I/O ^{Note} | R,/L = L, A ₁ to A ₃₍₆₎ : Output, B ₁ to B ₃₍₆₎ : Input The parenthesized pins are used in 6-bit input mode. |
| CLK | Clock | Input | Shift on a rising edge |
| R,/L | Shift control | Input | H: Right shift mode SR ₁ : A ₁ → S ₁S ₉₄ → B ₁ (SR ₂ and SR ₆ also shift in the same direction.) Left shift mode SR ₁ : B ₁ → S ₉₄S ₁ → A ₁ (SR ₂ and SR ₆ also shift in the same direction.) |
| IBS | Input mode switch | Input | H: 32-bit shift registers, 3-bit input mode L: 16-bit shift registers, 6-bit input mode |
| O ₁ to O ₉₆ | High withstand voltage | Output | 80 V, +15/-30 mA MAX. |
| V _{DD1} | Logic power supply | - | 5 V ± 5% |
| V _{DD2} | Driver power supply | - | 15 to 70 V |
| V _{SS1} | Logic ground | - | Connect to system ground |
| V _{SS2} | Driver ground | - | Connect to system ground |

Note In 3-bit input mode, unused I/O pins must be held at the L level.

To use for module, the back side of IC chip must be held at the V_{SS} (GND) level.

3. TRUTH TABLE

Shift Register Block

| Input | | Output | | Shift Register |
|-------|--------|-------------------------|-------------------------|---------------------------------|
| R,/L | CLK | A | B | |
| H | ↑ | Input | Output ^{Note1} | Right shift operation performed |
| H | H or L | | Output | Hold |
| L | ↑ | Output ^{Note2} | Input | Left shift operation performed |
| L | H or L | Output | | Hold |

- Notes**
1. On the rising edge of the clock, the data of S₉₁ to S₉₃ (S₈₅ to S₉₀) is shifted to S₉₄ to S₉₆ (S₉₁ to S₉₆), and is output from B₁ to B₃ (B₁ to B₆) (The parenthesized pins are used in 6-bit input mode.).
 2. On the rising edge of the clock, the data of S₄ to S₆ (S₇ to S₁₂) is shifted to S₁ to S₃ (S₁ to S₆), and is output from A₁ to A₃ (A₁ to A₆) (The parenthesized pins are used in 6-bit input mode.).

Latch Block

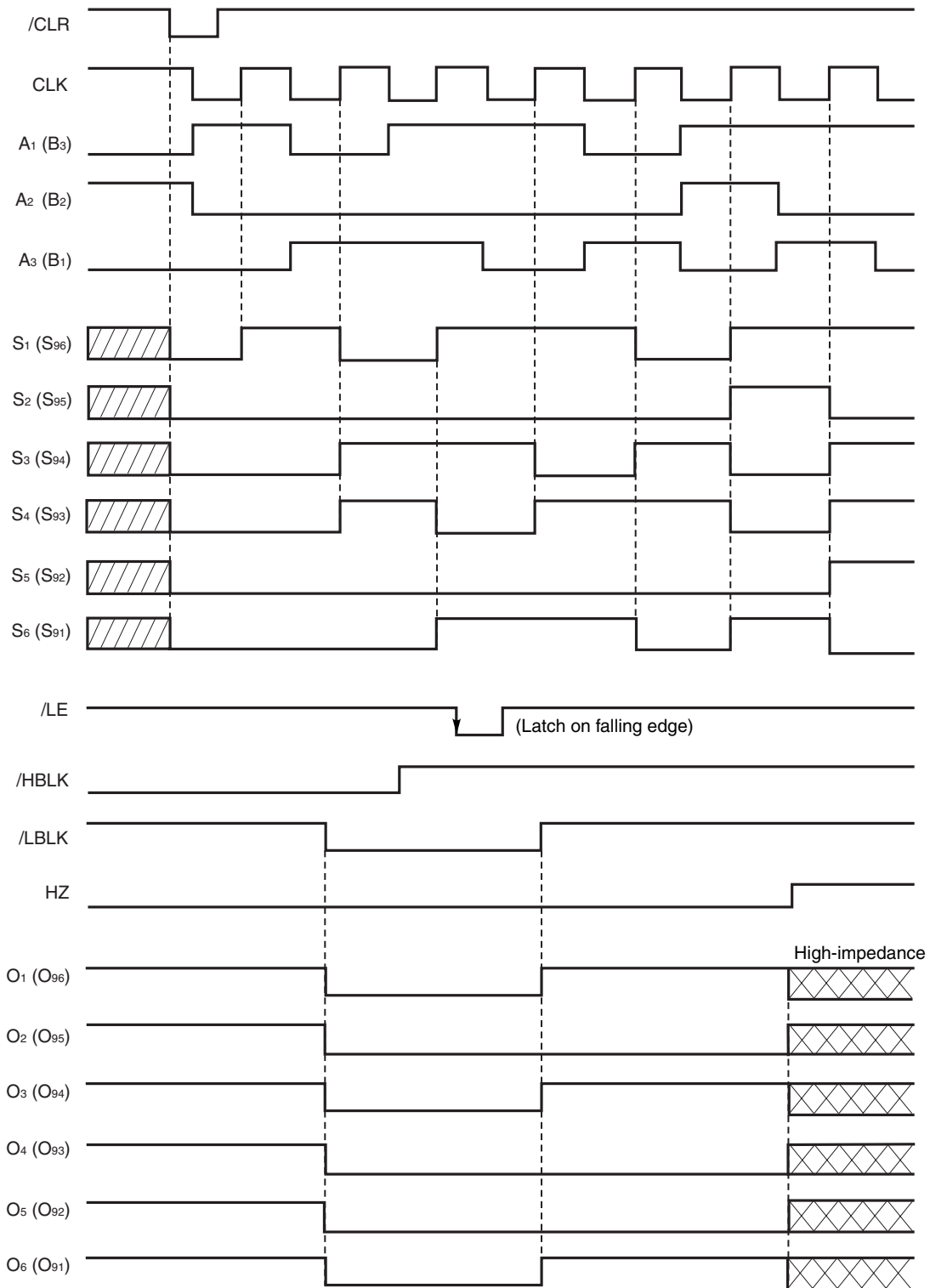
| /LE | Output State of Latch Section (/L _n) |
|--------|--|
| ↓ | Latch S _n data |
| H or L | Hold latch (output) data |

Driver Block

| A (B) | /HBLK | /LBLK | HZ | Output State of Driver Block |
|-------|-------|-------|----|-----------------------------------|
| x | L | H | L | All driver output: H |
| x | x | L | L | All driver output: L |
| x | x | x | H | All driver output: High Impedance |
| L | H | H | L | L |
| H | H | H | L | H |

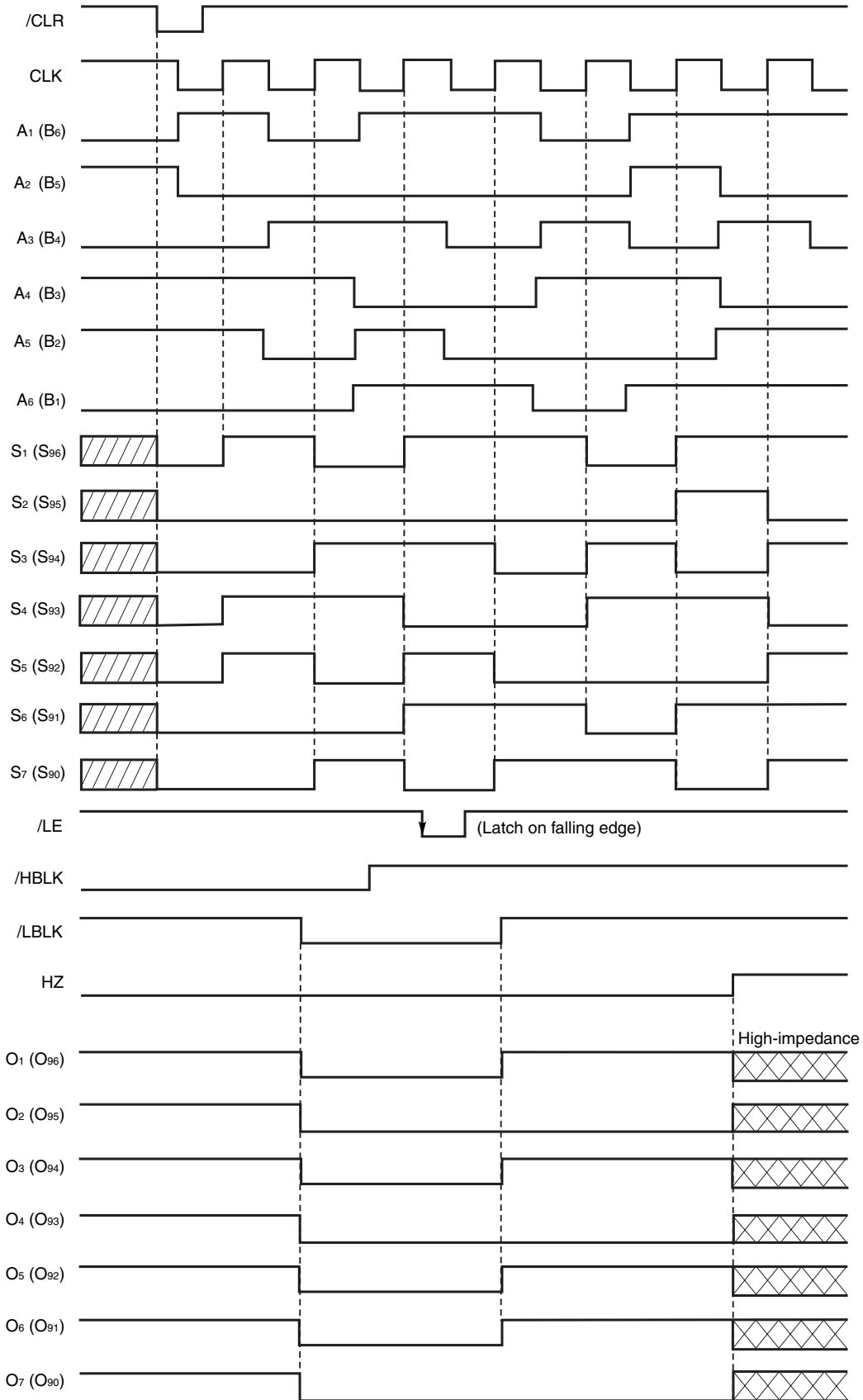
Remark x: H or L, H: High level, L: Low level

Timing Chart (1) (IBS = H, 3-bit input, right shift)



Remark Values in parentheses are when R,/L = L.

Timing Chart (2) (IBS = L, 6-bit input, right shift)



Remark Values in parentheses are when R,/L = L.

4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | Ratings | Unit |
|--------------------------------|------------------|--------------------------------|------|
| Logic Supply Voltage | V _{DD1} | -0.5 to +6.0 | V |
| Driver Supply Voltage | V _{DD2} | -0.5 to +80 | V |
| Logic Input Voltage | V _I | -0.5 to V _{DD1} + 0.5 | V |
| Driver Output Current | I _{O2} | +15/-30 | mA |
| Operating Junction Temperature | T _J | +125 | °C |
| Storage Temperature | T _{stg} | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|------------------|------------|------|------|------------------|------|
| Logic Supply Voltage | V _{DD1} | | 4.75 | 5.0 | 5.25 | V |
| Driver Supply Voltage | V _{DD2} | | 15 | | 70 | V |
| High-Level Input Voltage | V _{IH} | | 2.7 | | V _{DD1} | V |
| Low-Level Input Voltage | V _{IL} | | 0 | | 0.6 | V |
| Driver Output Current | I _{OH2} | | | | -24 | mA |
| | I _{OL2} | | | | +13 | mA |

Electrical Characteristics (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|-------------------|---|----------------------|------|----------------------|------|
| High-Level Output Voltage | V _{OH1} | Logic, I _{OH1} = -1.0 mA | 0.9 V _{DD1} | | V _{DD1} | V |
| Low-Level Output Voltage | V _{OL1} | Logic, I _{OL1} = 1.0 mA | 0 | | 0.1 V _{DD1} | V |
| High-Level Output Voltage | V _{OH21} | O ₁ to O ₉₆ , I _{OH2} = -0.52 mA | 69 | | | V |
| | V _{OH22} | O ₁ to O ₉₆ , I _{OH2} = -5.2 mA | 65 | | | V |
| Low-Level Output Voltage | V _{OL21} | O ₁ to O ₉₆ , I _{OL2} = 1.6 mA | | | 1.0 | V |
| | V _{OL22} | O ₁ to O ₉₆ , I _{OL2} = 13 mA | | | 10 | V |
| Input Leakage Current | I _{IL} | V ₁ = V _{DD1} or V _{SS1} | | | ±1.0 | μA |
| High-Level Input Voltage | V _{IH} | V _{DD1} = 4.75 to 5.25 V | 2.7 | | V _{DD1} | V |
| Low-Level Input Voltage | V _{IL} | V _{DD1} = 4.75 to 5.25 V | 0 | | 0.6 | V |
| Static Current Dissipation | I _{DD11} | Logic, T _A = -40 to +85°C | | | 500 | μA |
| | | Logic, T _A = 25°C | | | 300 | μA |
| | I _{DD12} | Logic, T _A = -40 to +85°C | | | 10 ^{Note} | mA |
| | | Logic, T _A = 25°C | | | 10 ^{Note} | mA |
| | I _{DD2} | Driver, T _A = -40 to +85°C | | | 1000 | μA |
| | | Driver, T _A = 25°C | | | 100 | μA |

Note When input all input high-level (V_{IH} = 2.7 V to V_{DD1}, but both R/L and IBS pin are fixed by V_I = V_{SS1} or V_{DD1})

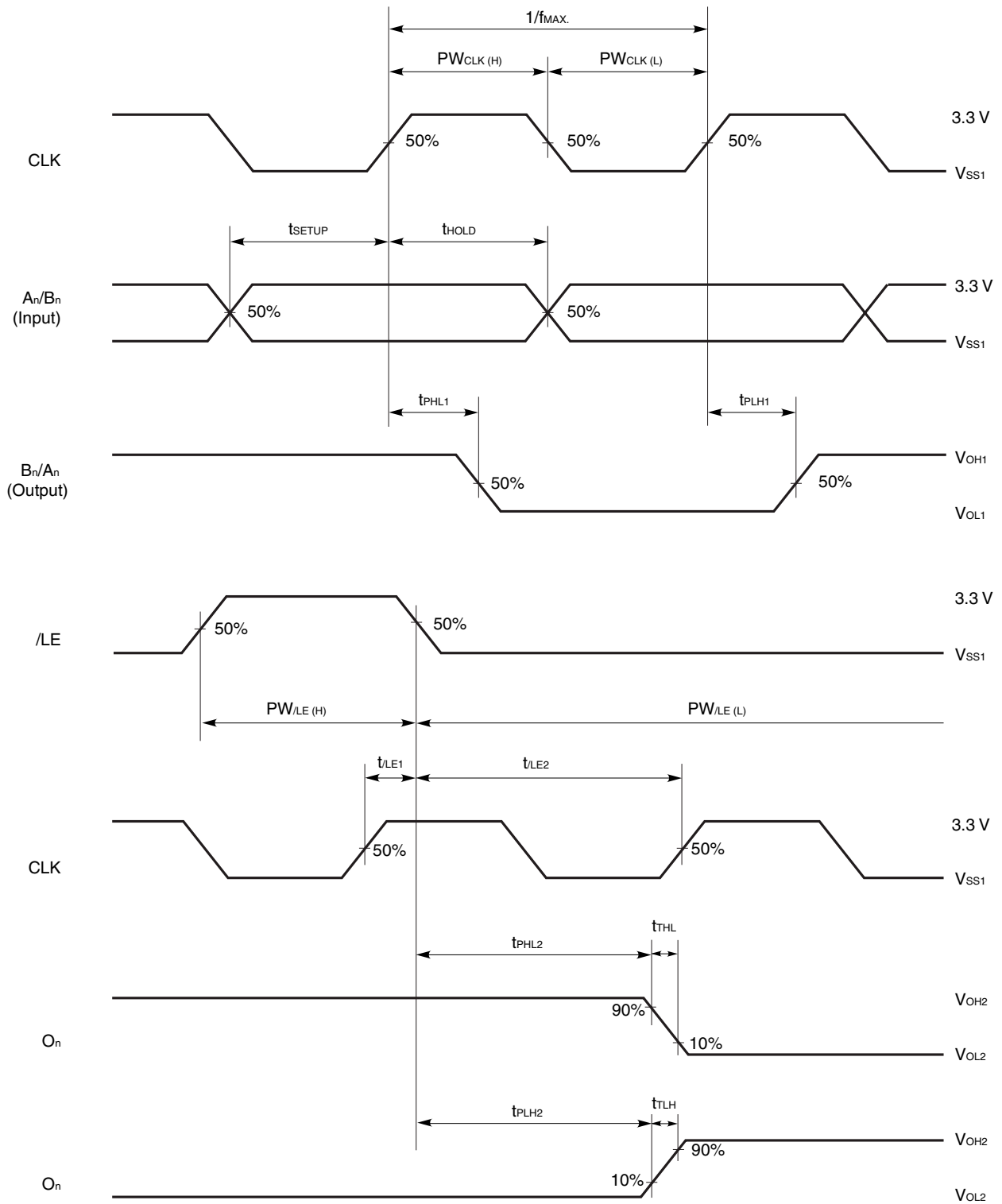
Switching Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 70\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$, Logic $C_L = 15\text{ pF}$,
 Driver $C_L = 50\text{ pF}$, $t_r = t_f = 6.0\text{ ns}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|------------|--|------|------|------|---------------|
| Propagation Delay Time | t_{PHL1} | CLK $\uparrow \rightarrow$ A/B | | | 34 | ns |
| | t_{PLH1} | | | | 34 | ns |
| | t_{PHL2} | /LE $\downarrow \rightarrow$ O ₁ to O ₉₆ | | | 220 | ns |
| | t_{PLH2} | | | | 220 | ns |
| | t_{PHL3} | /HBLK \rightarrow O ₁ to O ₉₆ | | | 205 | ns |
| | t_{PLH3} | | | | 205 | ns |
| | t_{PHL4} | /LBLK \rightarrow O ₁ to O ₉₆ | | | 200 | ns |
| | t_{PLH4} | | | | 200 | ns |
| | t_{PHZ} | HZ \rightarrow O ₁ to O ₉₆ , | | | 340 | ns |
| | t_{PZH} | $R_L = 10\text{ k}\Omega$ | | | 220 | ns |
| | t_{PLZ} | | | | 340 | ns |
| | t_{PZL} | | | | 220 | ns |
| Rise Time | t_{TLH} | O ₁ to O ₉₆ | | | 220 | ns |
| | t_{TLZ} | O ₁ to O ₉₆ , | | | 3 | μs |
| | t_{TZH} | $R_L = 10\text{ k}\Omega$ | | | 220 | ns |
| Fall Time | t_{THL} | O ₁ to O ₉₆ | | | 350 | ns |
| | t_{THZ} | O ₁ to O ₉₆ , | | | 3 | μs |
| | t_{TZL} | $R_L = 10\text{ k}\Omega$ | | | 350 | ns |
| Maximum Clock Frequency | f_{MAX} | Data latch, duty = 50% | 40 | | | MHz |
| | | Cascade connection, duty = 50% | 25 | | | MHz |
| Input Capacitance | C_i | | | | 15 | pF |

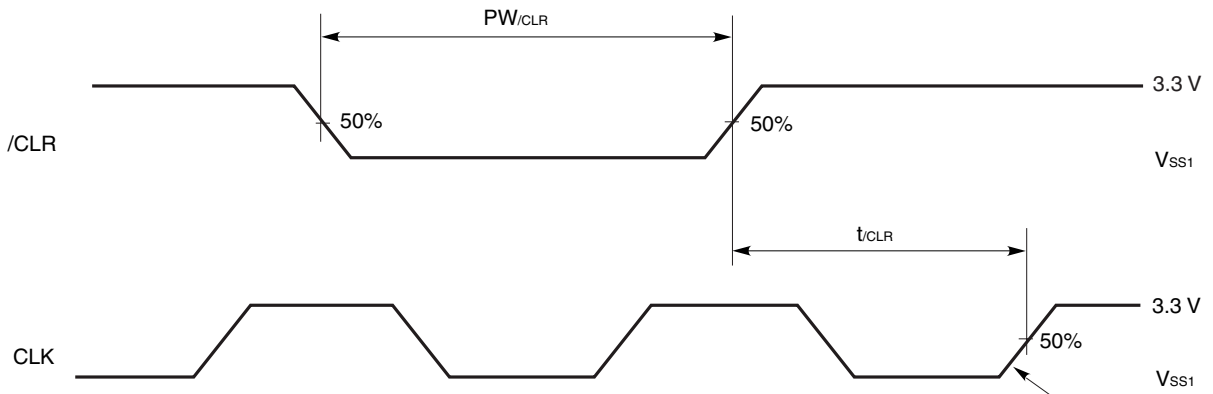
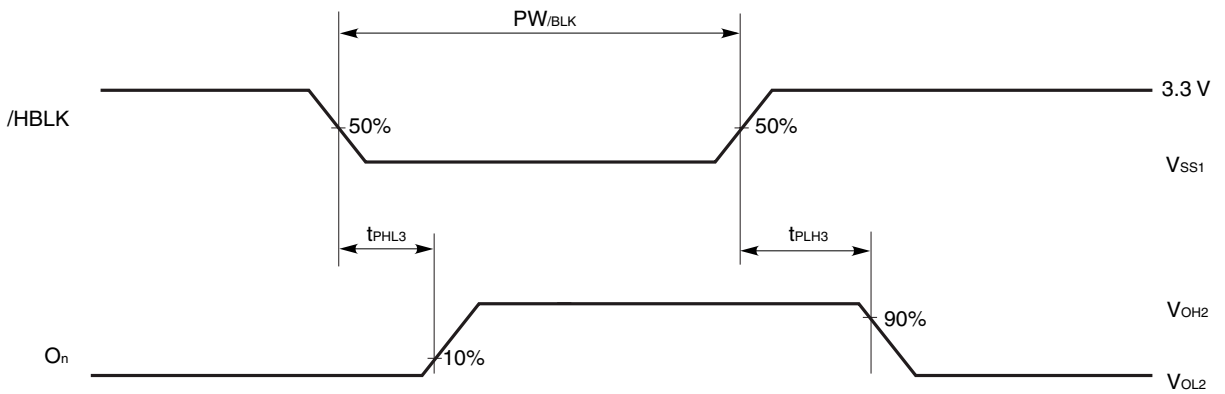
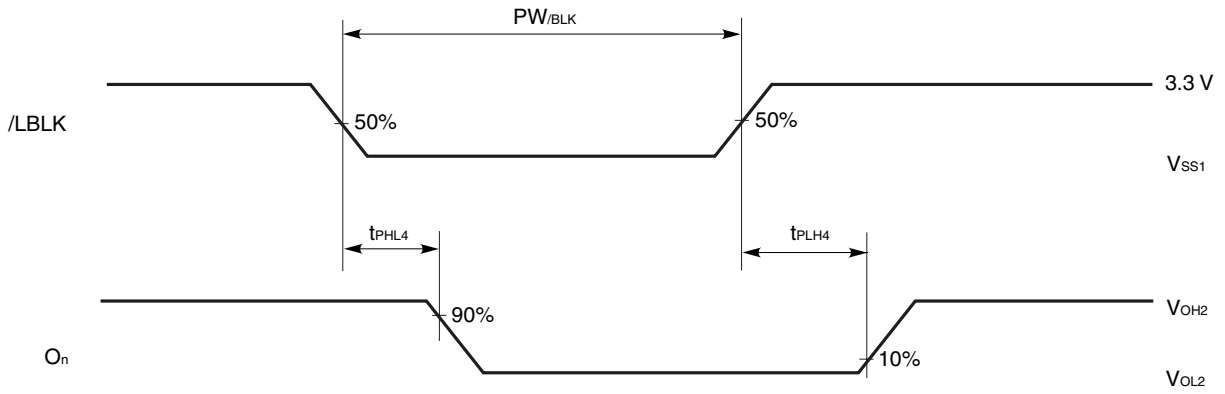
Timing Requirement ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD1} = 4.75$ to 5.25 V, $V_{SS1} = V_{SS2} = 0$ V, $t_r = t_f = 6.0$ ns)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|---------------|---------------------------|------|------|------|------|
| Clock Pulse Width | $PW_{CLK(H)}$ | | 12 | | | ns |
| | $PW_{CLK(L)}$ | | | | | |
| Latch Enable Pulse Width | $PW_{/LE(H)}$ | | 12 | | | ns |
| | $PW_{/LE(L)}$ | | | | | |
| Blank Pulse Width | $PW_{/BLK}$ | /HBLK, /LBLK | 600 | | | ns |
| HZ Pulse Width | PW_{HZ} | $R_L = 10\text{ k}\Omega$ | 3.3 | | | μs |
| /CLR Pulse Width | $PW_{/CLR}$ | | 12 | | | ns |
| Data Setup Time | t_{SETUP} | | 4 | | | ns |
| Data Hold Time | t_{HOLD} | | 6 | | | ns |
| Latch Enable Time | t_{LE1} | | 12 | | | ns |
| | t_{LE2} | | 12 | | | ns |
| /CLR Timing | t_{CLR} | | 6 | | | ns |

★ Switching Characteristics Waveform (1/3)

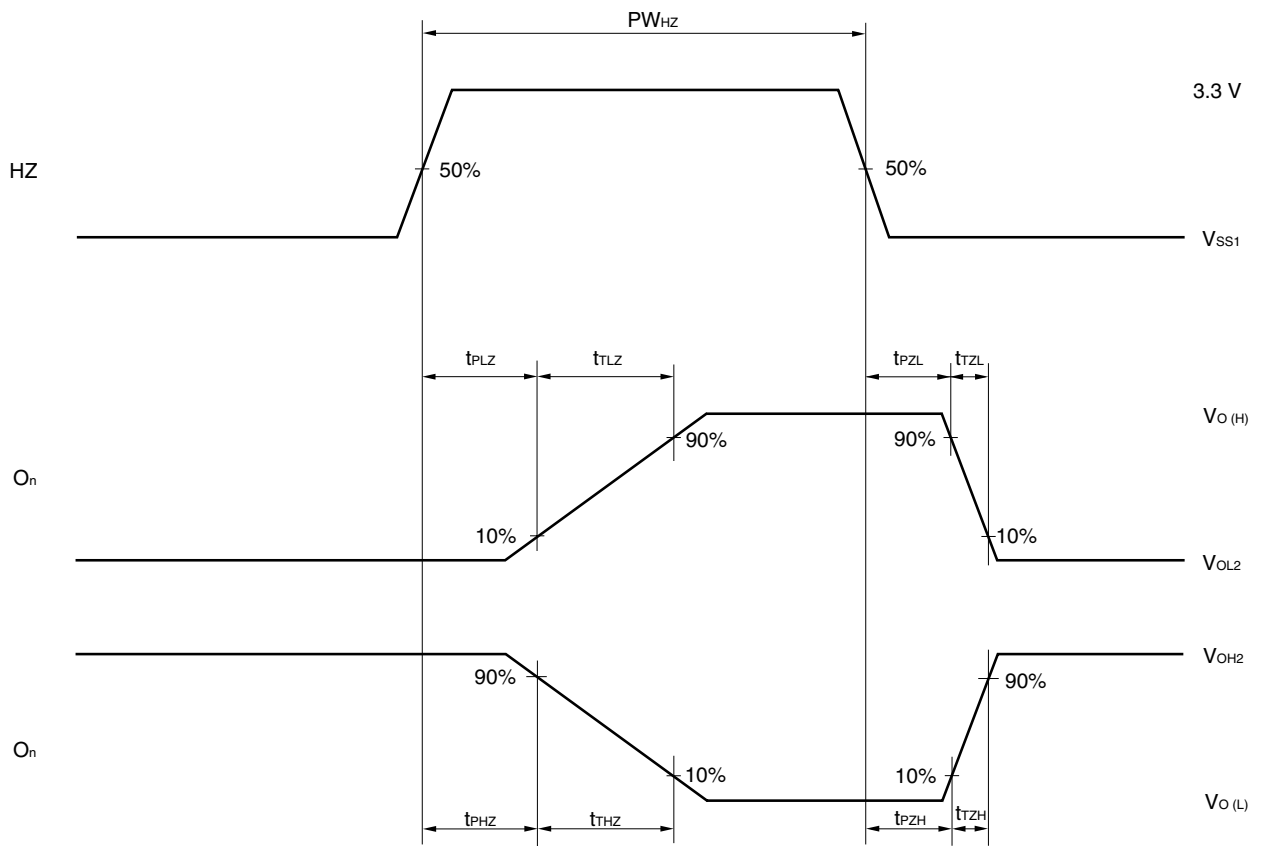


★ Switching Characteristics Waveform (2/3)



Clock rising edge for valid data

★ Switching Characteristics Waveform (3/3)



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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