NEC Electronics Inc.

MC-42256A36, -424256A36
262,144 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-42256A36 and the MC-424256A36 are dynamic RAM modules organized as 264,144 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_8 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains 12 DRAMs and 12 power supply decoupling capacitors. The complement of DRAMs (μPD424256, 41256, 42256, 421000) and the operating mode (fast-page, page) are summarized below.

Module	DRAMs (Qty) 256K x 4	256K x 1	1M x 1
MC-42256A36 B/F (fast-page)	(8) μPD424256	(4) μPD42256	
MC-424256A36 BH/FH (fast-page)	(8) μPD424256		(4) μPD421000
MC-424256A36 B/F (page)	(8) μPD424256	(4) μPD41256	

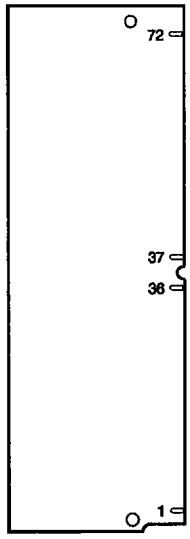
Features

- 262,144-word by 36-bit organization
- Single +5-volt power supply
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging
- Fast-page mode operation (MC-42256A36B/F and MC-424256A36BH/FH)
- Page mode operation (MC-424256A36B/F)

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	NC
33	NC
34	$\overline{RAS}_2$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	GND
68	NC
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 69 and 70 are defined by access time:

Pin	70 ns	80/85 ns	100 ns
69	GND	NC	GND
70	NC	GND	GND

83FM-6344A

Ordering Information

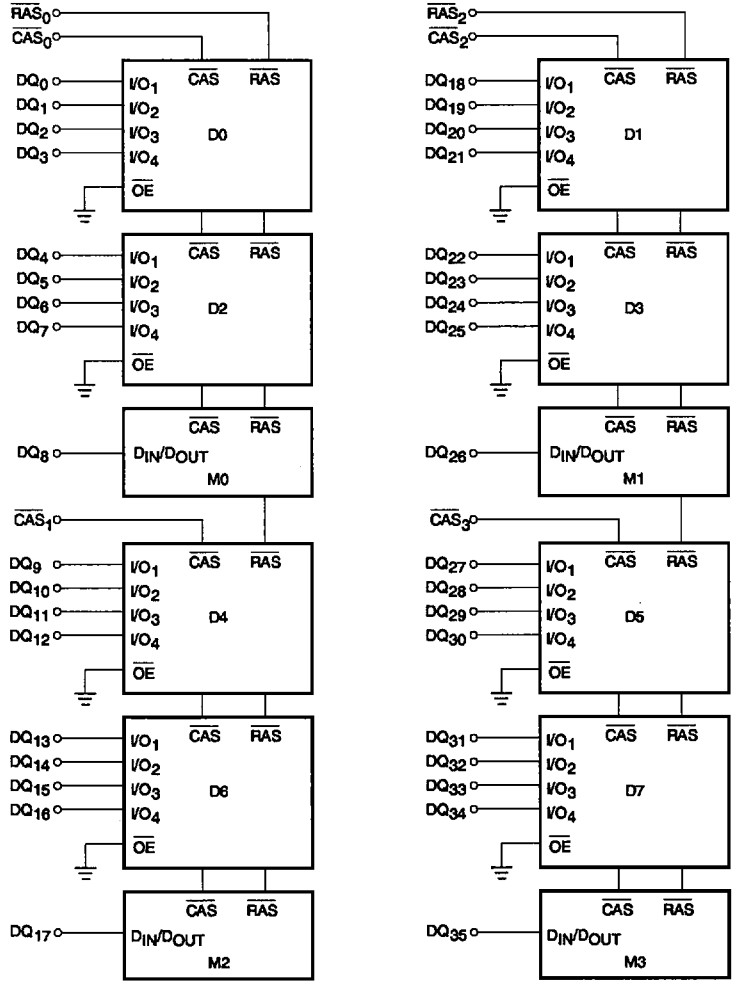
Part Number	Access Time (max)	Package	Operation	Height	Thickness	DRAMs
MC-42256A36B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	25.4 mm (1.00 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD42256L
B-80	80 ns					
B-10	100 ns					
MC-42256A36F-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
F-80	80 ns					
F-10	100 ns					
MC-424256A36BH-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	31.75 mm (1.25 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD421000LA
BH-80	80 ns					
BH-10	100 ns					
MC-424256A36FH-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
FH-80	80 ns					
FH-10	100 ns					
MC-424256A36B-80	80 ns	72-pin socket-mountable SIMM (solder plating)	Page	25.4 mm (1.00 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD41256L
B-85	85 ns					
B-10	100 ns					
MC-424256A36F-80	80 ns	72-pin socket-mountable SIMM (gold plating)				
F-85	85 ns					
F-10	100 ns					

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

9d

Connection Diagram; MC-42256A36, -424256A36



Desig	DRAM	Used On
D0-D7	μPD424256LA	All
M0-M3	μPD421000LA	MC-424256A36BH/FH
	μPD42256LA	MC-42256A36B/F
	μPD41256L	MC-424256A36B/F

83IH-83468

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_8
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (Note 17)		960		840		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (Note 18)		920		800		680	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (Note 17)		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (Note 18)		920		800		680	mA	
Operating current, fast-page cycle, average	I_{CC4} (Note 17)		840		720		600	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (Note 18)		800		680		560	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (Note 17)		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (Note 18)		920		800		560	mA	
Access time from column address	t_{AA}		35		45		50	ns	(Notes 7, 9)

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, + 4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) MC-424256A36BH/FH

(18) MC-42256A36B/F

DC Characteristics 2 (MC-424256A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		36	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
			8	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	$I_{I(L)}$	–120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics 2 (MC-424256A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		960		808		680	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		916		764		660	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time	t_{CP}	20		20		40		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	

AC Characteristics 2 (MC-424256A36B/F) (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

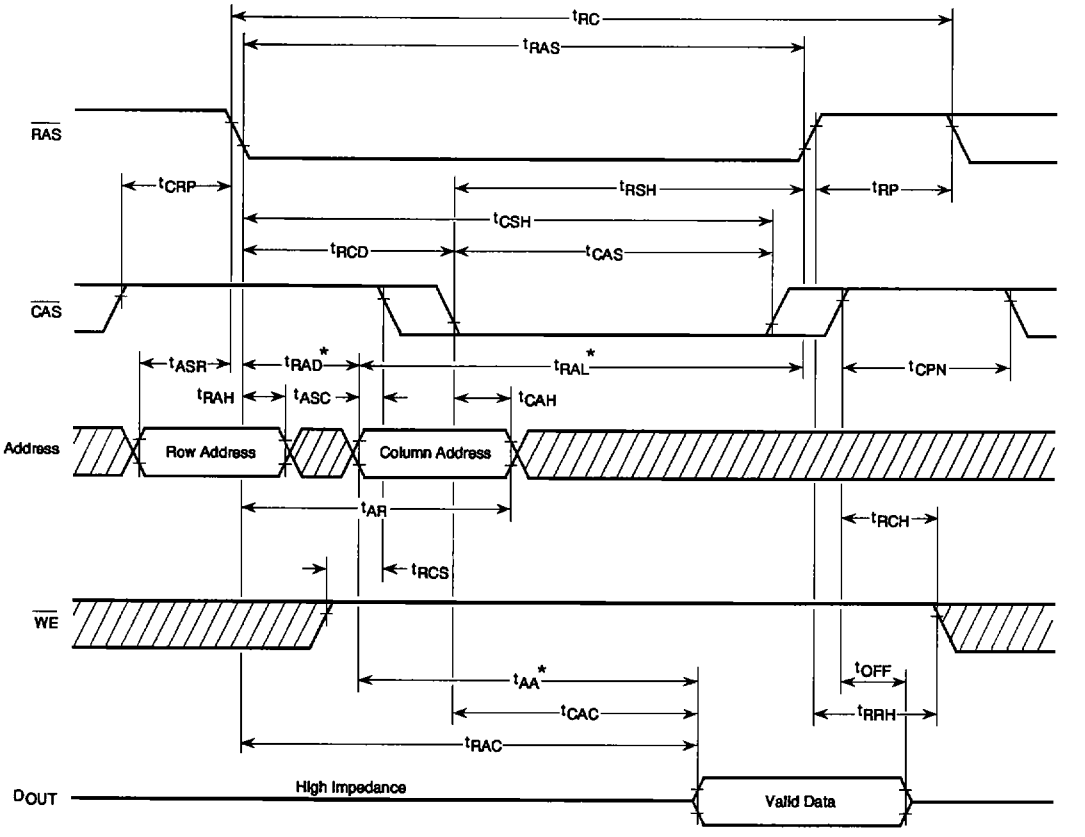
(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

9d

Timing Waveforms

Read Cycle



*These parameters are not applicable to the MC-424256A36B/F.

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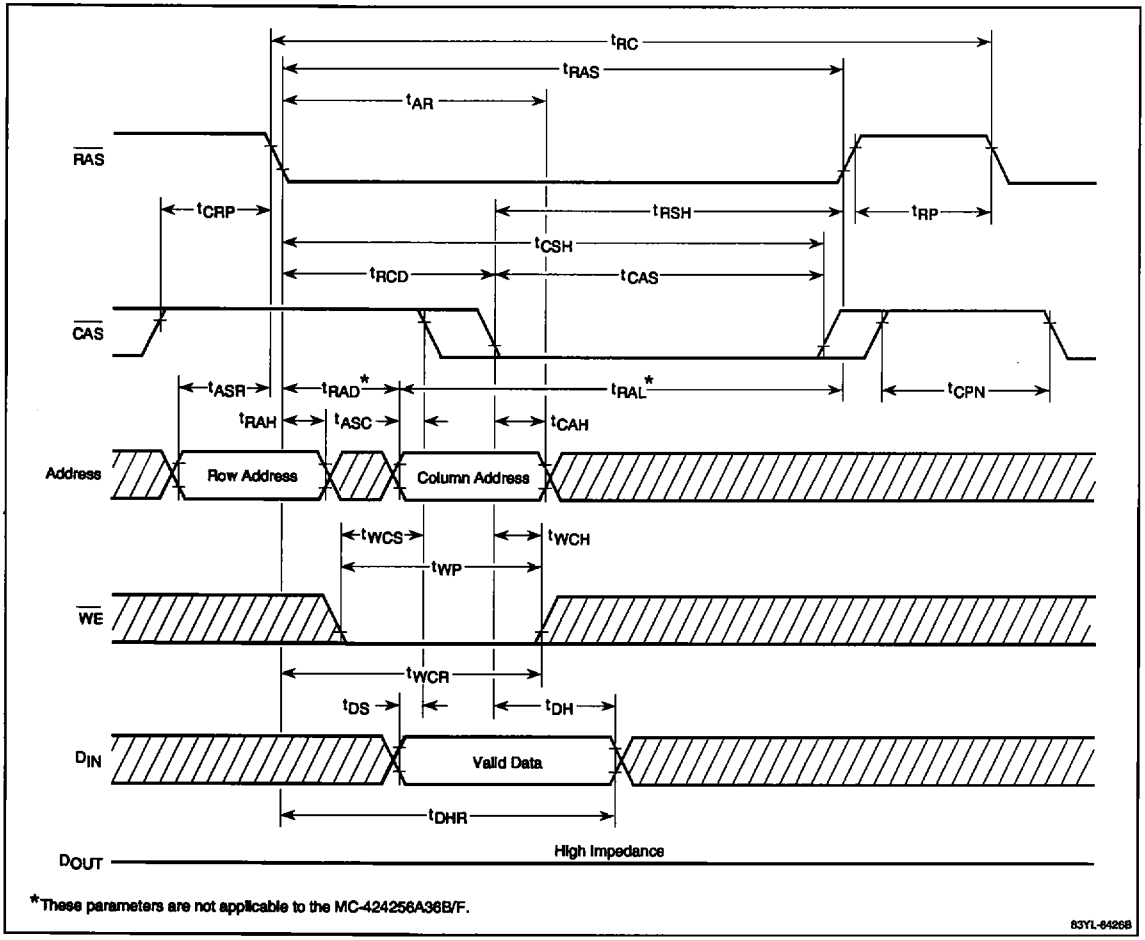
Timing Waveforms (cont)

Early Write Cycle



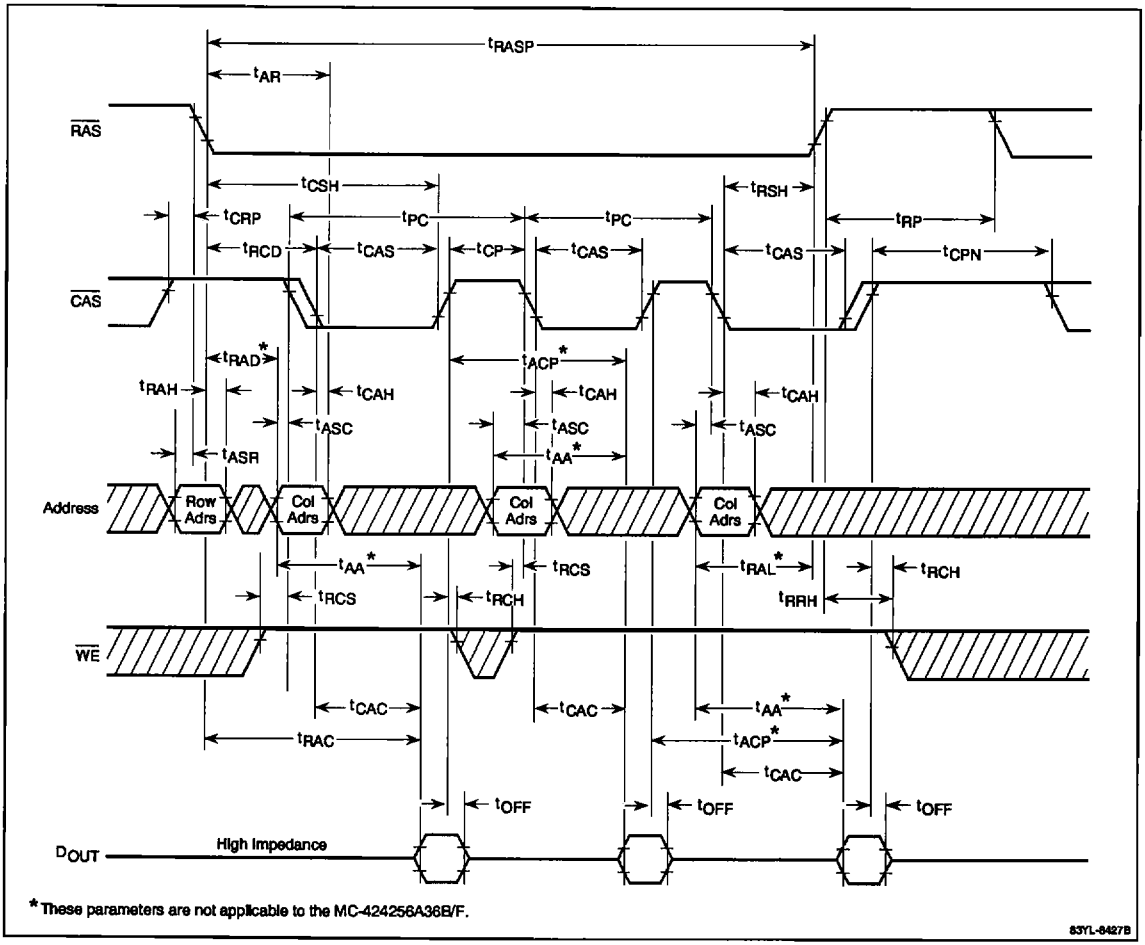
*These parameters are not applicable to the MC-424256A36B/F.

83YL-6426B

9d

Timing Waveforms (cont)

Page/Fast-Page Read Cycle

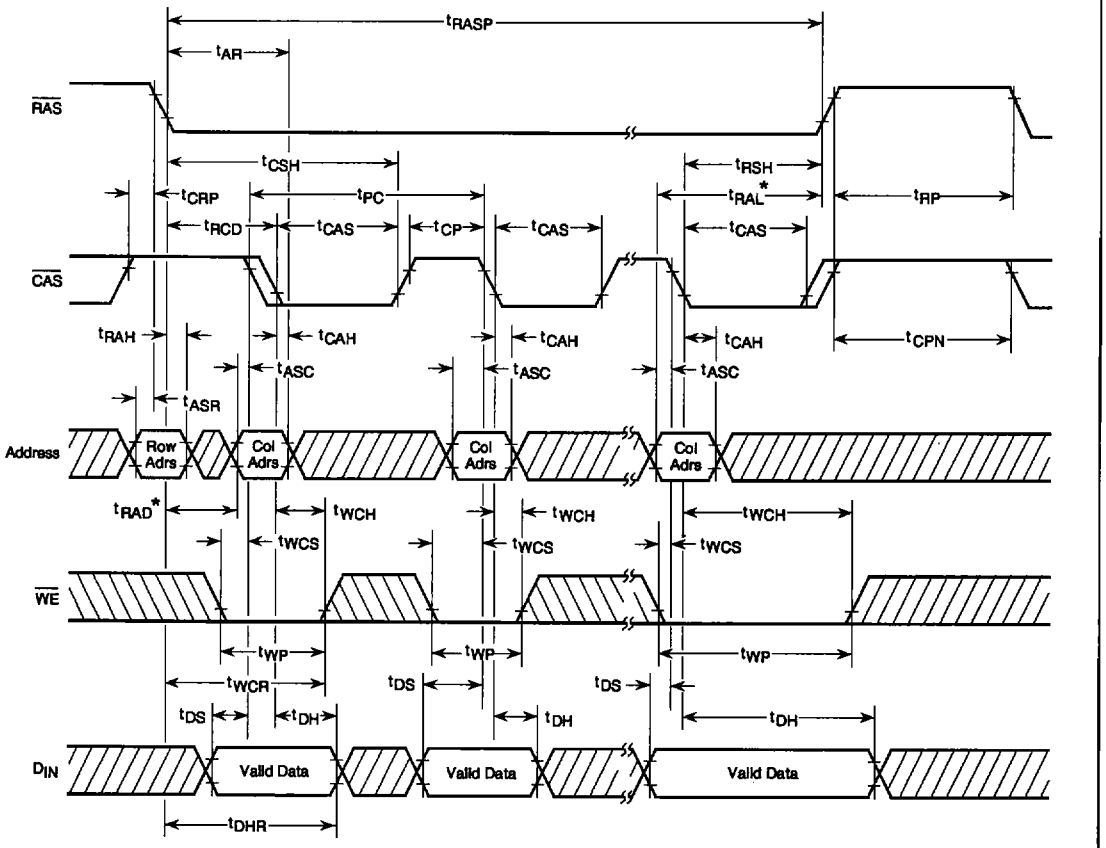


* These parameters are not applicable to the MC-424256A36B/F.

83YL-6427B

Timing Waveforms (cont)

Page/Fast-Page Early Write Cycle



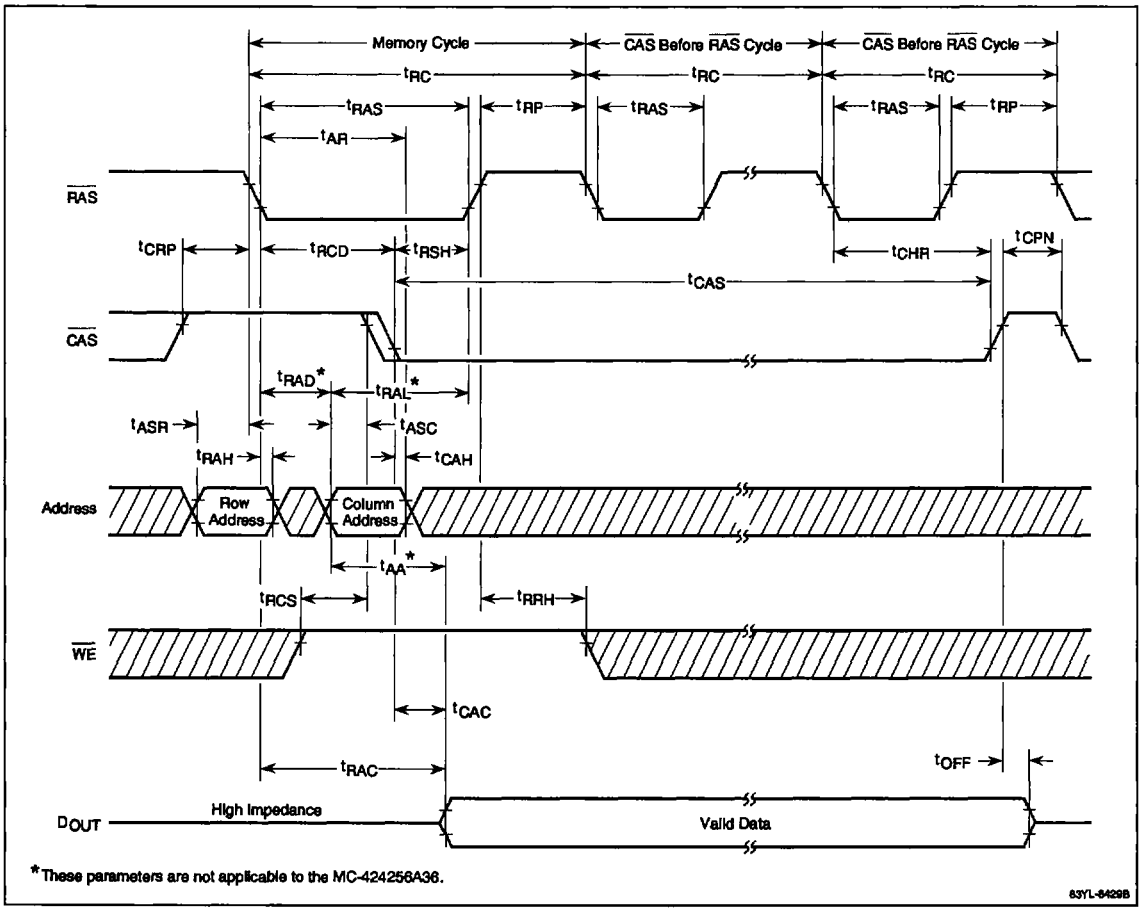
*These parameters are not applicable to the MC-424256A36B/F.

83YL-8428B

9d

Timing Waveforms (cont)

Hidden Refresh Cycle

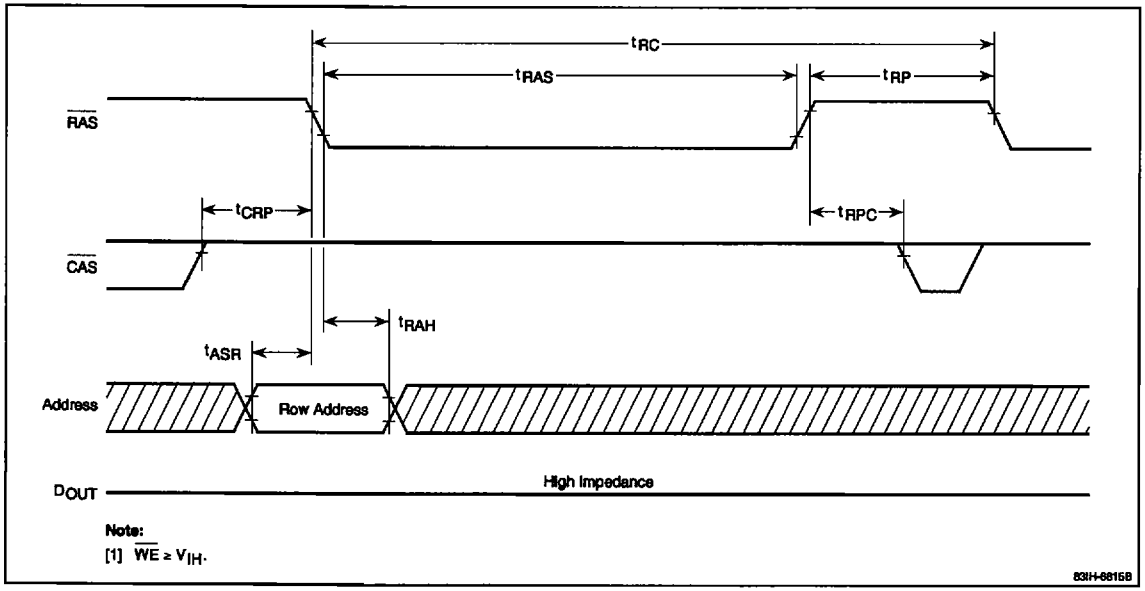


*These parameters are not applicable to the MC-424256A36.

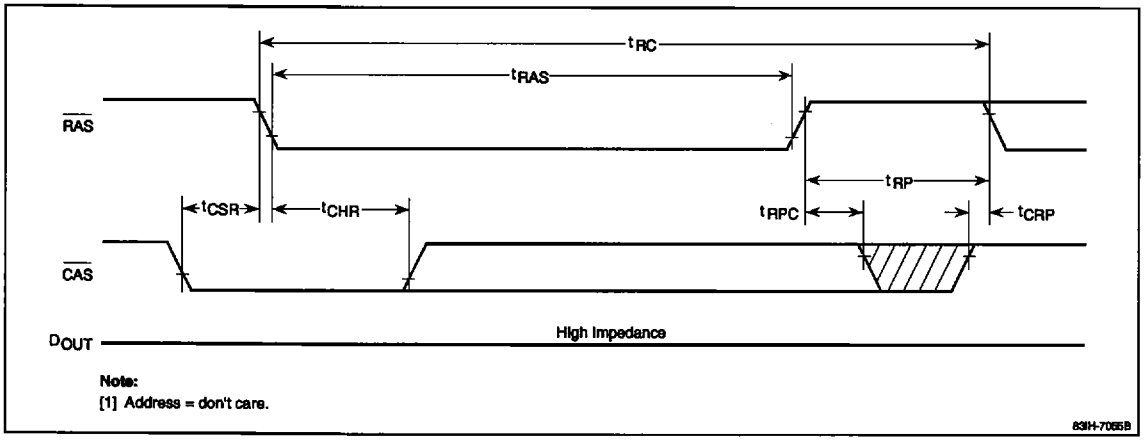
63YL-8429B

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



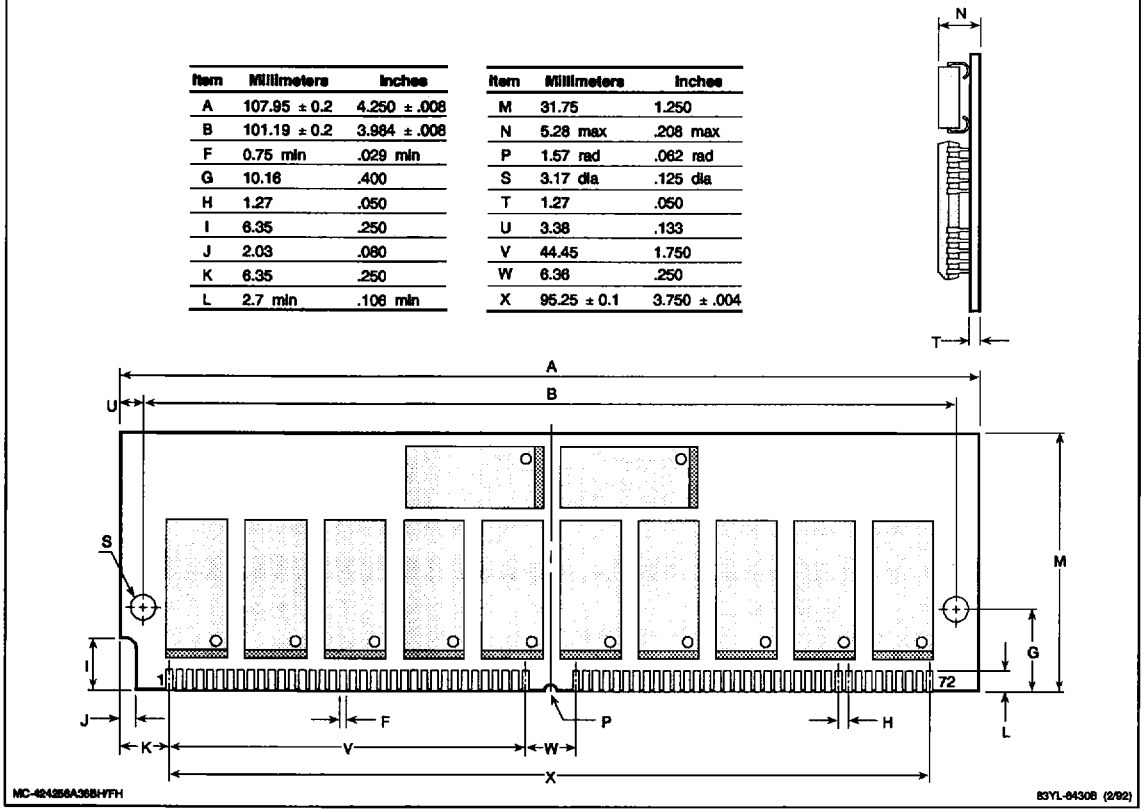
9d

Package Drawings

72-Pin Socket-Mountable SIMM (MC-424256A36BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004

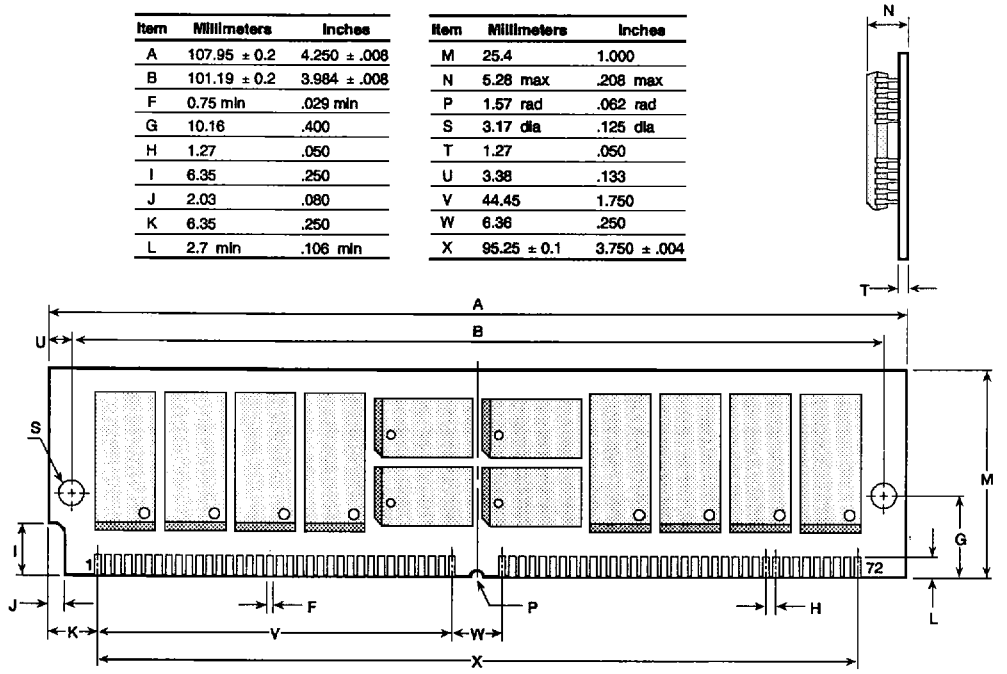


Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42256A36B/F and MC-424256A36B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-42256A36B/F, -424256A36B/F

83YL-8431B (2/92)