

TRIPLE-PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 70ns random, 22ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 350mW active, typical
- 512-cycle refresh within 16.7ms
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERS
- BLOCK WRITE
- BIT MASKED TRANSFERS

OPTIONS

- Timing (DRAM, SAMs [READ cycle / WRITE cycle])

60ns*, 20ns/20ns	-6
70ns, 22ns/20ns	-7
80ns, 25ns/22ns	-8

MARKING

- Packages

Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
- Functionality

QSF output (indicates SAM-half accessed)	MT43C4257A
SSF input (Split SAM special function, stop count)	MT43C4258A

• Part Number Example: MT43C4257ADJ-7

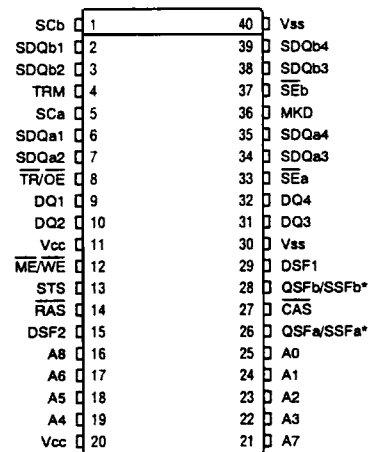
* Consult factory for -6 availability

GENERAL DESCRIPTION

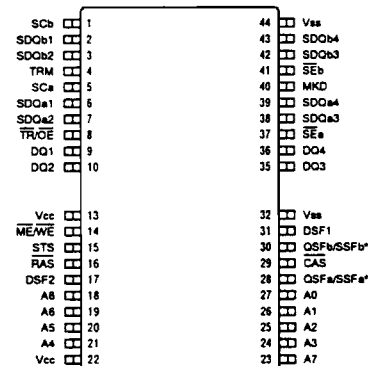
The MT43C4257A/8A are high-speed, triple-port CMOS dynamic random access memories (TPDRAMs) containing 1,048,576 bits. Data may be accessed by a 4-bit-wide DRAM

PIN ASSIGNMENT (Top View)

40-Pin SOJ (SDA-2)



40/44-Pin TSOP (SDD-1)



*MT43C4257A/MT43C4258A

port or by either of two independently clocked 512 x 4-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and either SAM.

TRIPLE-PORT DRAM

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The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048-bit-wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address-decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

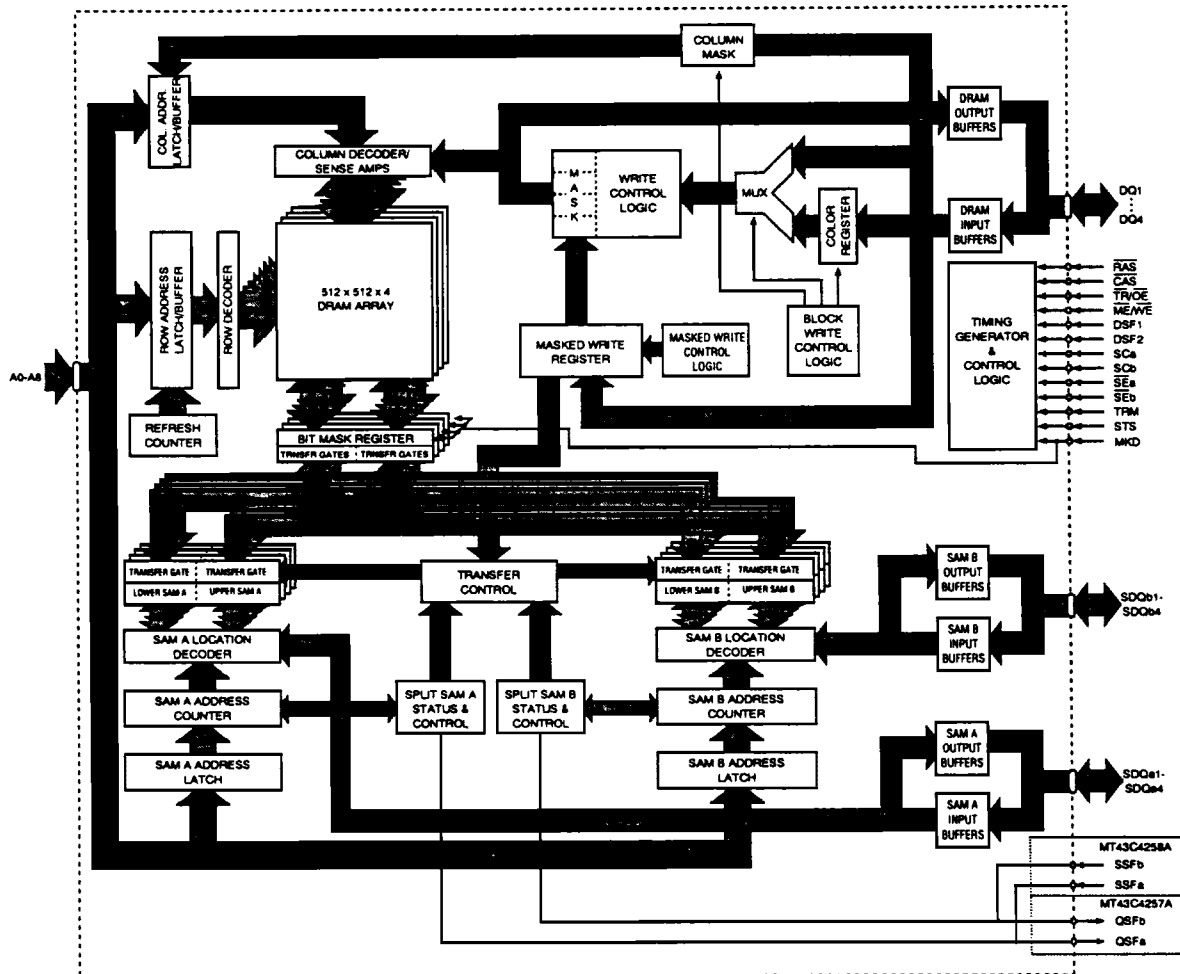
Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit, bit-mask data register may be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257A/8A are optimized for high-performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERS and BLOCK WRITE allow further enhancements to system performance.

TRIPLE-PORT DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5	5	SCa	Input	Serial Clock, SAMA: Clock input to the serial address counter for the SAMA registers and strobe for SAMA control and data inputs.
1	1	SCb	Input	Serial Clock, SAMB: Clock input to the serial address counter for the SAMB registers and strobe for SAMB control and data inputs.
8	8	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of RAS, or Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW); otherwise, the output buffers are in a High-Z state.
12	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
33	37	SEa	Input	Serial Port Enable SAMA: SEa enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEa is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
37	41	SEb	Input	Serial Port Enable, SAMB: SEb enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEb is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
29	31	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
15	17	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
14	16	RAS	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits and strobe the control and data inputs.
27	29	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe control inputs and data inputs.

TRIPLE-PORT DRAM

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by \overline{RAS} and \overline{CAS} to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when \overline{RAS} goes LOW) and the SAM start address (when \overline{CAS} goes LOW).
13	15	STS	Input	SAM Transfer Select: The state of STS at \overline{RAS} time determines which SAM is involved in a transfer (SAMA = LOW, SAMb = HIGH).
36	40	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at \overline{RAS}), then MKD is used as mask data input and is clocked by SCb into the mask data register.
4	4	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
9, 10, 31, 32	9, 10, 35, 36	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
6, 7, 34, 35	6, 7, 38, 39	SDQa1-SDQa4	Input/ Output	Serial Data I/O, SAMA: Input, Output, or High-Z.
2, 3, 38, 39	2, 3, 42, 43	SDQb1-SDQb4	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
26	28	QSFa/SSFa	Output Input	Split SAM Status, SAMA (MT43C4257A): QSFa indicates which half of SAMA is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMA (MT43C4258A): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
28	30	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C4257A): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C4258A): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V \pm 5%
30, 40	32, 44	Vss	Supply	Ground

TRIPLE-PORT DRAM

FUNCTIONAL DESCRIPTION

The MT43C4257A/8A may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, the TR/OE pin will be shown as TR/(OE) in references to transfer operations.

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C4257A/8A TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT43C4257A/8A support CBR, RAS ONLY and HIDDEN types of refresh cycles.

For the CBR REFRESH cycle, the row-addresses are generated and stored in an internal address counter. The user need not supply any address data but must simply perform 512 CBR cycles within the 16.7ms time period.

For RAS ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the RAS ONLY and CBR cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling RAS (while keeping CAS LOW) after a READ or WRITE cycle. This performs CBR REFRESH cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C4257A/8A are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM.

These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 18 address bits used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS, and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

Note: RAS also acts as a "master" chip enable for the TPDRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.

For single-port DRAMS, the OE pin is a "don't care" when RAS goes LOW. For the TPDRAM, TR/(OE) is used when RAS goes LOW to select between DRAM and TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH to LOW transition for all DRAM operations.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transition from HIGH to LOW some time after RAS falls to enable the DRAM output port.

For single-port DRAMS, WE is a "don't care" when RAS goes LOW. For the TPDRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW when CAS goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

TRIPLE-PORT DRAM

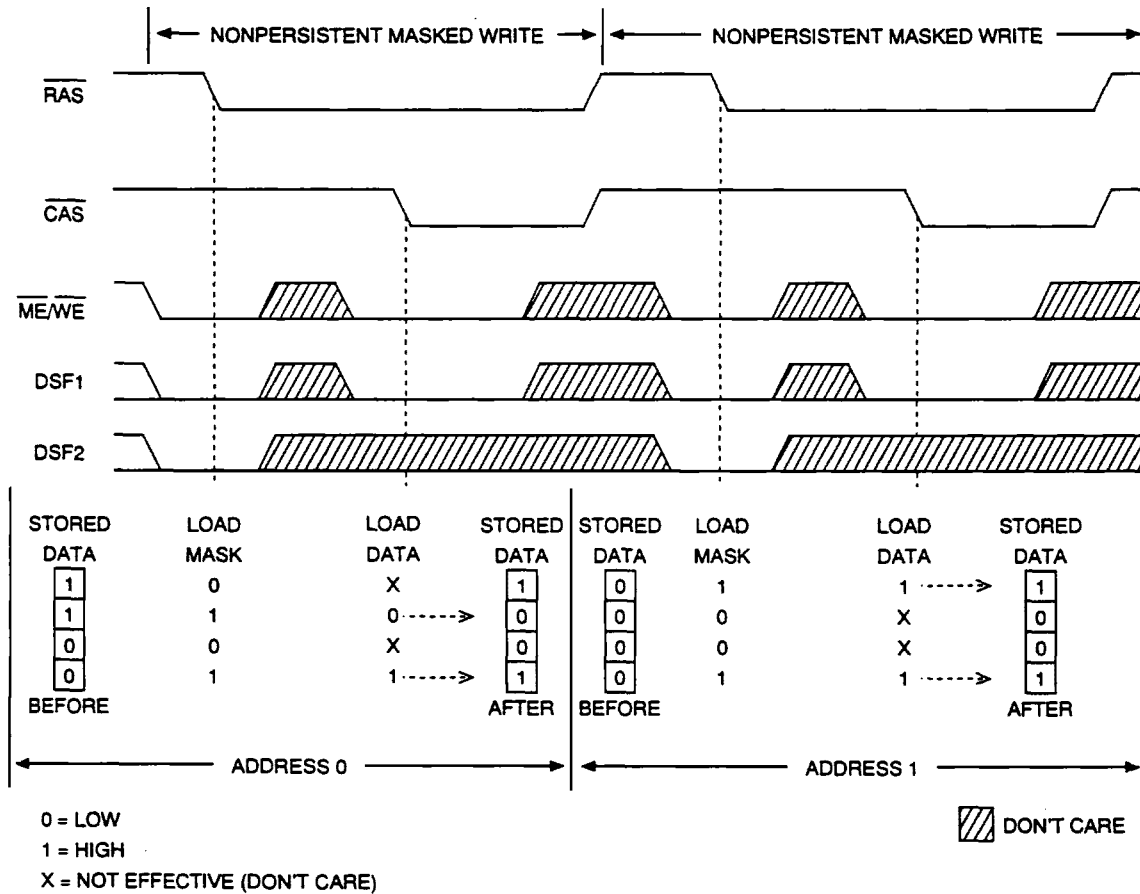


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a 4-bit word. The MT43C4257A/8A support two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/\overline{WE}$, DSF1 and DSF2 are LOW at the \overline{RAS} HIGH-to-LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This

convention is used for all masks on the MT43C4257A/8A. Note that \overline{CAS} is still HIGH. When \overline{CAS} and $\overline{ME}/\overline{WE}$ go LOW, the bits present on the DQ1-DQ4 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of \overline{RAS} . FAST-PAGE-MODE can be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one \overline{RAS} cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

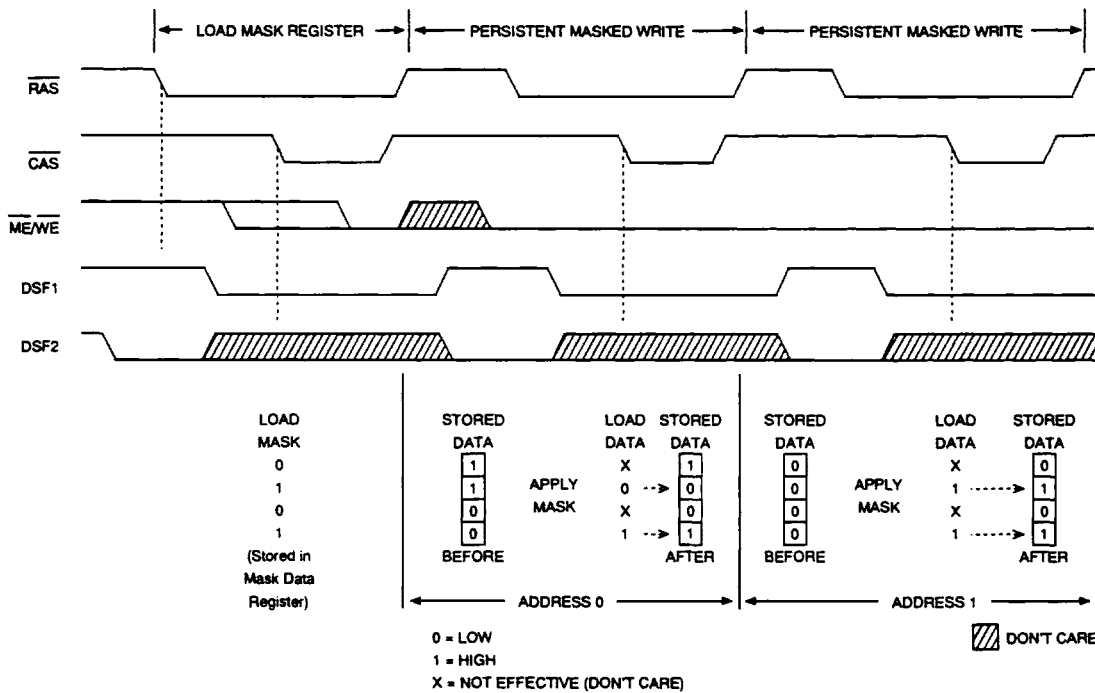


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW, when \overline{RAS} goes LOW. The mask data is loaded into the internal register when \overline{CAS} goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description). PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW, and DSF1 HIGH when \overline{RAS} goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs.

Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when \overline{RAS} falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at \overline{RAS} time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST-PAGE-MODE.

BLOCK WRITE (BW)

The MT43C4257A/8A will perform a BLOCK WRITE cycle if DSF1 is HIGH when \overline{CAS} goes LOW. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 16 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when \overline{CAS} goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" (out of the 128 possible) of four adjacent column locations that will be accessed. When the latter of $\overline{ME}/\overline{WE}$ and \overline{CAS} go LOW, the DQ inputs are latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls (DQs) are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color

TRIPLE-PORT DRAM

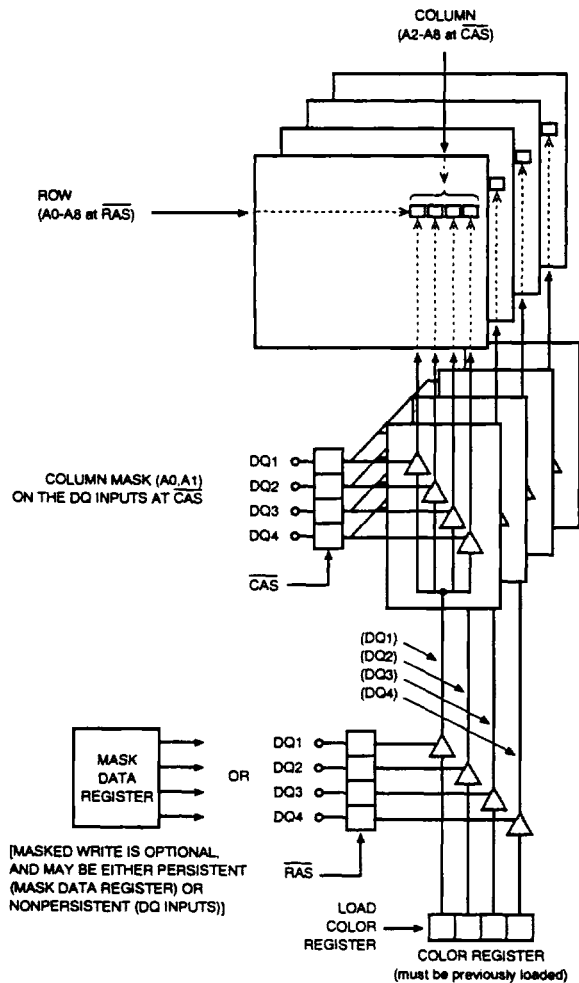


Figure 3
BLOCK WRITE EXAMPLE

register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions may be used during BLOCK WRITE cycles also. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF1 LOW when \overline{RAS} goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF1 pin must be driven HIGH when \overline{CAS} goes LOW to perform

a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when \overline{CAS} goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C4257A / 8A contain two 4-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when \overline{RAS} goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when \overline{RAS} goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when \overline{CAS} goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable WRITES to the four DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when \overline{CAS} goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A WRITE is referenced to the DRAM array and a READ is referenced from the array.

Note: *The three ports of the TPDRAM are independent of, and asynchronous to, one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of \overline{RAS} . The state of STS when \overline{RAS} goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when \overline{RAS} goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping \overline{CAS} . In this case, the previously loaded Tap address will be used.

The MT43C4257A/8A include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a transfer operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERS. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of \overline{RAS} .

NORMAL TRANSFERS

The MT43C4257A/8A support all of the popular transfer cycles available on Micron's 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{ME})/\overline{WE}$ is HIGH, DSF1, DSF2 and $\overline{TR}/(\overline{OE})$ are LOW when \overline{RAS} goes LOW. When \overline{RAS} goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row-address bits indicate the four 512-bit DRAM rows that are to be transferred to the four SAM data registers. The column-address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW

if the lower half, HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAM's I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while \overline{RAS} is low and after the t_{RTH} timing has been met. In order to synchronize the REAL-TIME READ TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not synchronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of \overline{CAS} . The transfer will be completed internally by the device. The first serial clock must meet the t_{RSD} and t_{CSD} delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 9-bit Tap address register is loaded into the address counter. If \overline{SE} for the SAM selected (\overline{SEa} for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. \overline{SE} enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of \overline{RAS} and \overline{CAS} . The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal (non-split) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT can be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when \overline{RAS} goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that

receives the transfer. When $\overline{\text{CAS}}$ falls, address pins A0-A7 determine the Tap address for the SAM-half receiving the transfer; A8 = "don't care." If $\overline{\text{CAS}}$ does not fall, the most recently loaded Tap address for that SAM will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half $\neq 0$. For the MT43C4257A, serial access continues, and when the SAM address counter reaches 255 ("A8" = 1, A0-A7 = 0), the QSF output for that SAM goes HIGH. [QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed]. Then the Tap address for the upper half is automatically loaded. Since the serial access has switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the

upper SAM. $\overline{\text{CAS}}$ is used to load the Tap address. If $\overline{\text{CAS}}$ does not fall, the last Tap address load for the addressed SAM will be reused. If the terminal count of that SAM half is reached before an SRT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

The split SAM operation is slightly different for the MT43C4258A. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (255; lower, 511; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. If SSF is HIGH at SC before an SRT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an SRT, the access will proceed as it does for the MT43C4257A.

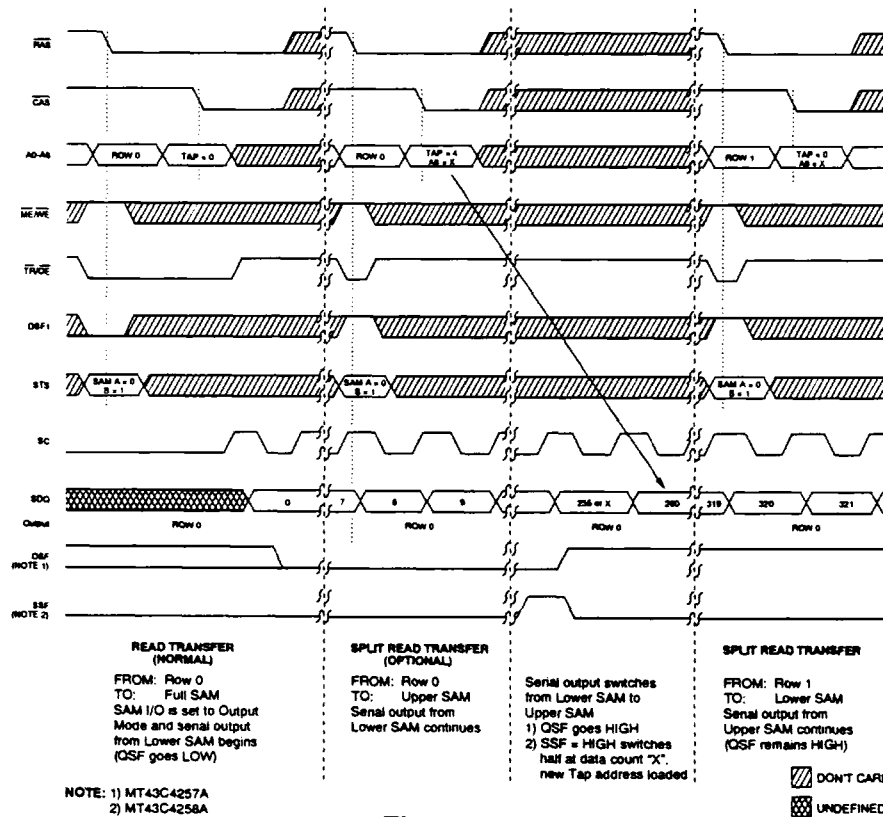


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except \overline{ME} / \overline{WE} and \overline{SE} must be LOW when \overline{RAS} goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when \overline{RAS} goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the \overline{SE} of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the four DQ planes (see Figure 5). The MWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of \overline{RAS} .

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The DQ MASKED SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, an MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately

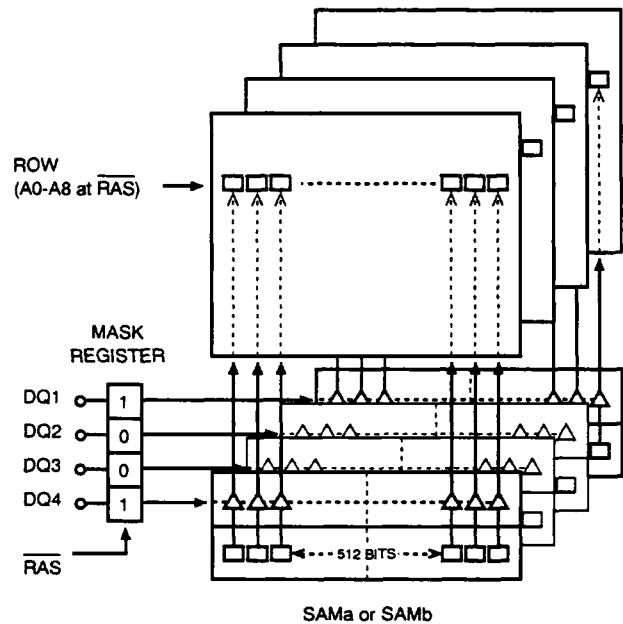


Figure 5
DQ MASKED WRITE TRANSFER

transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all four of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every MSWT cycle at \overline{RAS} time. The mask data acts as an individual write enable for each of the four DRAM DQ planes. For example, DQ1, at \overline{RAS} time, during a MASKED WRITE enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A7) for the other half is loaded when \overline{CAS} falls (A8 is a "don't care"). If \overline{CAS} does not fall, the most recently loaded Tap address for that SAM, A0-A7, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C4257A) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C4258A in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked in. When the final data is input, the SSF input is taken HIGH

at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (255 or 511). If SSF is HIGH at SC before an MSWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C4257A.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, SEa,b and SSFa,b (MT43C4258A). The rising edge of SC increments the serial address counter and provides access to the next SAM location. SE enables or disables the serial input/output buffers.

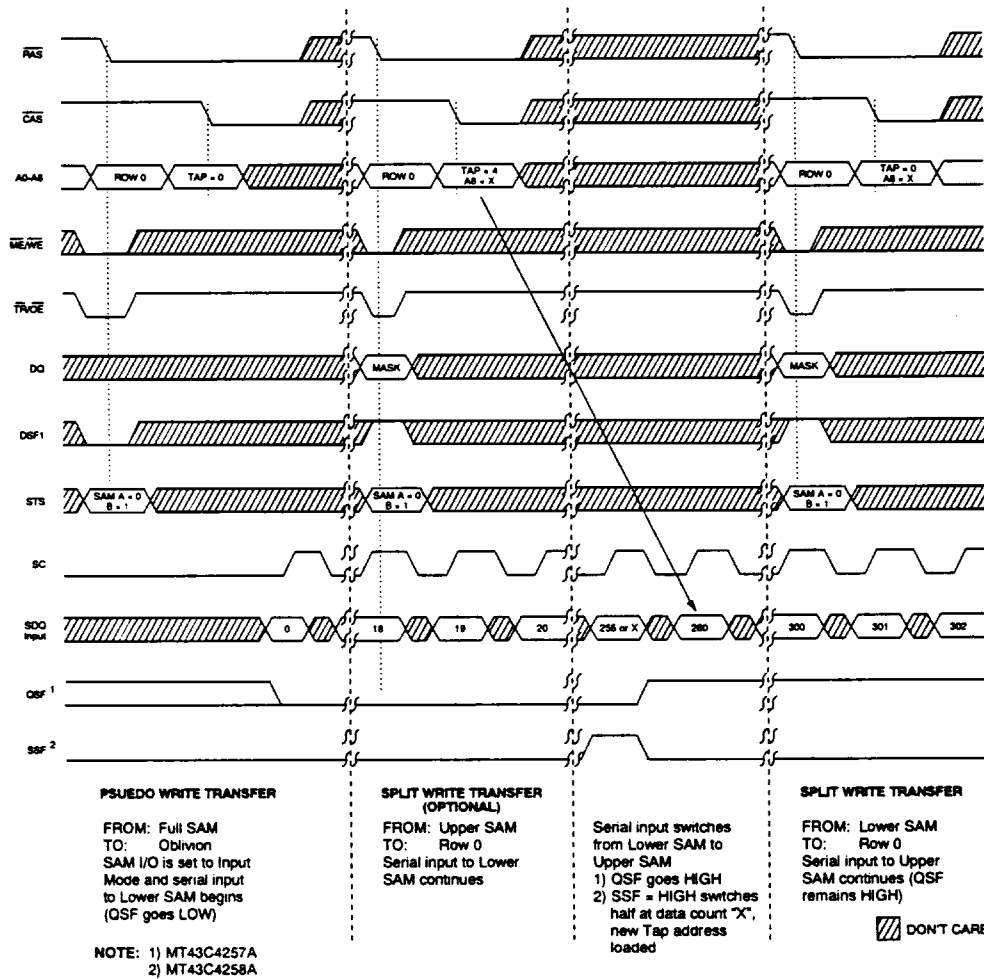


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

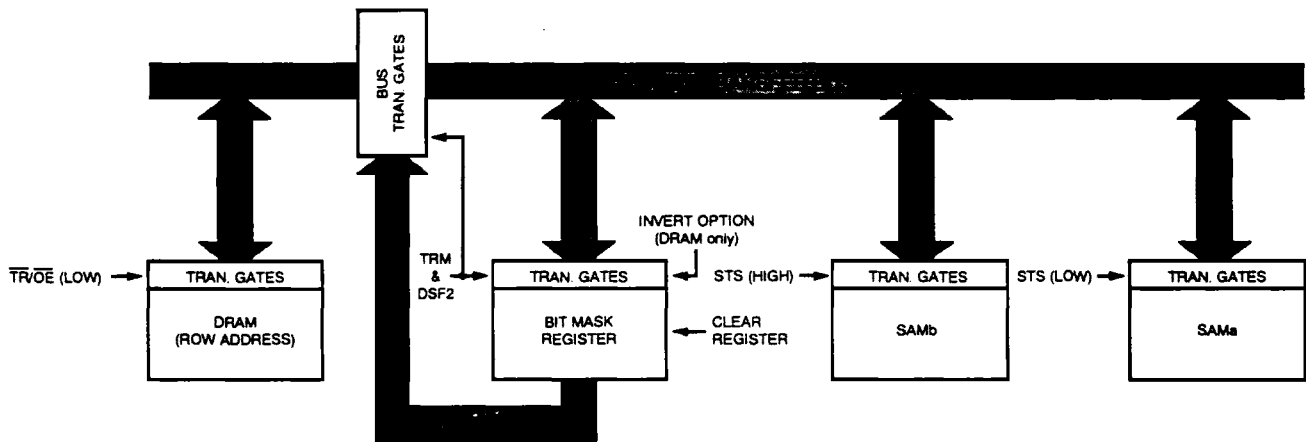


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial Tap address that was loaded in the SAMa,b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. \overline{SE} is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether \overline{SE} is HIGH or LOW. For the MT43C4257A, the address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. The address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

For the MT43C4258A, the address count will wrap as it does for the MT43C4257A, or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. \overline{SE} acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE} = \text{HIGH}$, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the \overline{SE} input. The

operation of SSF (MT43C4258A) is the same as described for serial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERS, the bit mask register must be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONS, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 512 x 4 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERS, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERS may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERS. The timing and control required for any particular BIT MASKED TRANSFER cycle are identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERS between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

TRIPLE-PORT DRAM

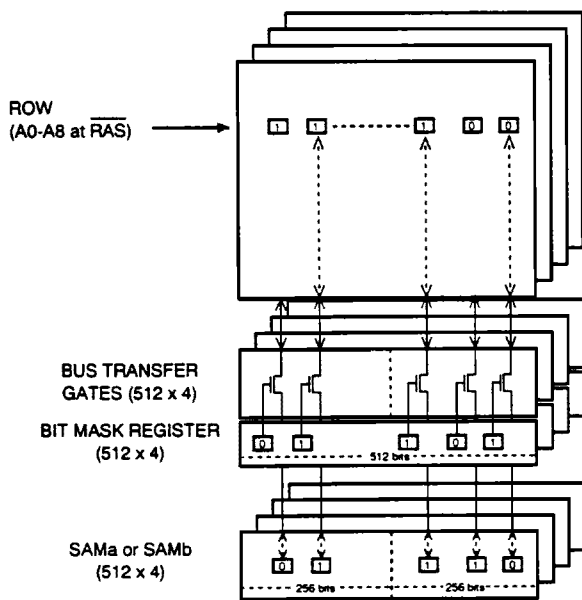


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH to select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when \overline{RAS} falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when \overline{RAS} falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at \overline{RAS} time. If a DQ input is LOW at \overline{RAS} time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 256 SAM bits for that row half will be masked by the corresponding 256 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

DQ MASKED BIT MASKED WRITE TRANSFER (BMWT-DQM)

The BMWT-DQM cycle is nearly identical to the BIT MASKED WRITE TRANSFER, except TRM is LOW and DSF1 is HIGH when \overline{RAS} falls. Two masks are applied during a BMWT-DQM operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at \overline{RAS} time. If a DQ input is LOW at \overline{RAS} time, none of the 512 SAM bits for that DQ plane will be transferred to the DRAM row selected. If a DQ input is HIGH, the 512 SAM bits for that row will be masked by the corresponding 512 mask register bits when written to the selected DRAM row. The remaining control timing is identical to the requirements for a normal WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR contents. Data may be inverted when being transferred between the BMR and DRAM also.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the BMR by using the BMR READ TRANSFER function. When \overline{RAS} falls, TR / (\overline{OE}) is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when \overline{RAS} falls selects whether the serial mask input (SMI) feature is enabled (see the Functional Truth

Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). When \overline{RAS} falls, MKD is LOW to disable SMI, or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the four bit-planes, the data on the MKD pin is written to each bit plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at \overline{RAS} time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. To select a WRITE TRANSFER from the BMR, $\overline{ME}/\overline{WE}$ and DSF2 are LOW and TRM is HIGH when \overline{RAS} falls. The DQ inputs are used to input a DQ bit-plane mask when \overline{RAS} falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at \overline{RAS} time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at \overline{RAS} time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM, instead of the DRAM, is the source of the data. $\overline{ME}/\overline{WE}$ is used to indicate the direction of the transfer, and must be LOW when \overline{RAS} falls for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since

no DRAM access is involved, it is not necessary to provide any particular ROW address at \overline{RAS} time. However, the ROW-address present at \overline{RAS} time will be used as the address for a \overline{RAS} -ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Tap) will be loaded at \overline{CAS} time. This address will be loaded into the serial address counter of the SAM selected by STS at \overline{RAS} time.

Note: Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The $\overline{ME}/\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when \overline{CAS} falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bits LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at \overline{RAS} time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/(\overline{OE})$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are HIGH when \overline{RAS} falls. When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at \overline{RAS} time the serial mask input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when \overline{RAS} falls, during a

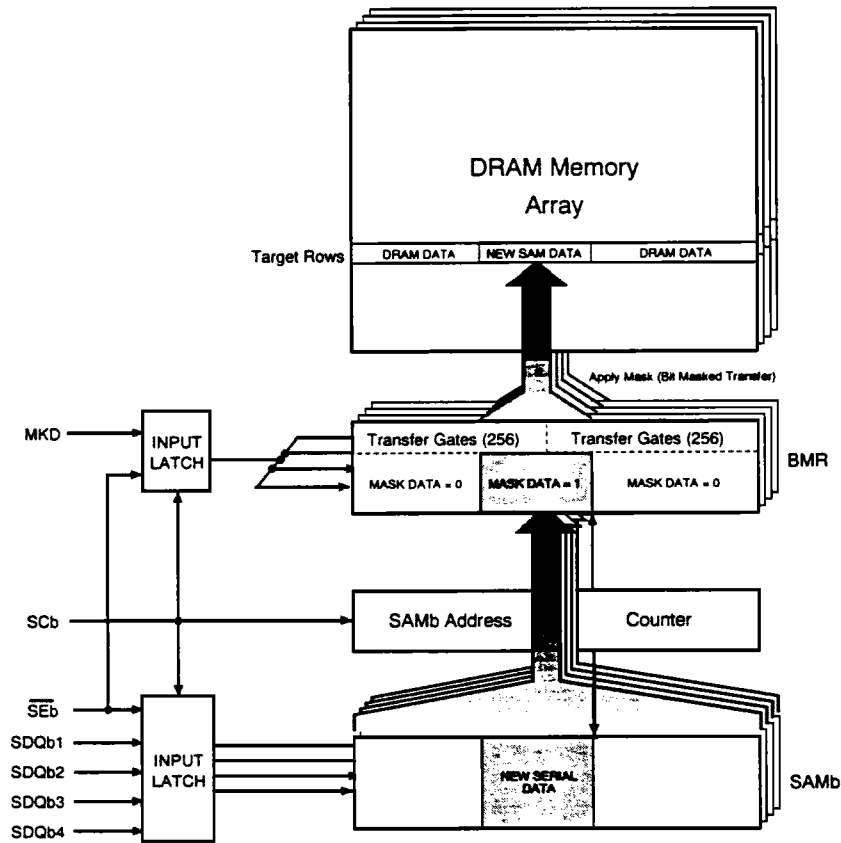


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all four of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR; the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at $\overline{\text{RAS}}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all four planes of the BMR will

be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER or DQ-MASKED BIT-MASKED-WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER or DQ-MASKED BIT-MASKED-WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear only half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via

MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa, or if SMI is disabled.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 16.7ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (MIN), eight RAS cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of (TR)/OE. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will

power-up in the serial input mode (WRITE TRANSFERS) and the SAM I/O pins (SDQs) are in a High-Z state, regardless of the state of SE ab. Also, SPLIT TRANSFER and SMI modes are disabled. The SAMs, as well as the bit mask, color, and DRAM mask registers all contain random data after power-up.

All SDQ and DQ pins are initialized to a High-Z state by the internal power-up detection circuitry. This helps to eliminate bus conflicts, which may occur during power-up sequencing. However, due to the infinite number of ways in which the power supply may be ramped, Micron strongly recommends asserting the OE and SE pins high while applying power to the device. Further, it is recommended that the eight RAS initialization cycles include WRITE TRANSFER commands to both SAMa and SAMb. This sequence will guarantee that both SAMs are in input mode and that the SDQs will be in a High-Z state.

TRIPLE-PORT DRAM

TRUTH TABLE 1

CODE	FUNCTION	RAS FALLING EDGE										CAS FALL	A0-A8 ²		DQ1-DQ4 ³		REGISTERS	
		CAS	TR/OE	WE/WE ⁴	DsF1	DsF2	SEa, SEb	TRM	MKD	STS	DsF1	RAS	CAS	RAS	CAS, WE ⁴	MASK	COLOR	
DRAM OPERATIONS																		
CBR	CAS-BEFORE-RAS REFRESH	0	X	1 ¹¹	X	X	X	X	X	X	X	X	X	X	X	—	—	
ROR	RAS-ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	—	—	
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0 ¹¹	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	—	—	
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0 ¹¹	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	—	
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0 ¹¹	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	—	
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0 ¹¹	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	—	USE	
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0 ¹¹	X	X	X	X	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE	
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0 ¹¹	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE	
REGISTER OPERATIONS																		
LMR	LOAD MASK REGISTER	1	1	1	1	0 ¹¹	X	X	X	X	0	X ⁵	X	X	WRITE MASK	LOAD	—	
LCR	LOAD COLOR REGISTER	1	1	1	1	0 ¹¹	X	X	X	X	1	X ⁵	X	X	COLOR DATA	—	LOAD	
TRANSFER OPERATIONS																		
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—	
SRT ⁹	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—	
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—	
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X ⁵	TAP ⁶	X	X	—	—	
MSWT ⁹	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH DQ MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	DQ MASK	X	—	—	
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	DQ MASK	X	—	—	

TRUTH TABLE 1

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8 ²		DQ1-DQ4 ³		REGISTERS	
		CAS	TR/OE	ME/WE ¹⁰	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS, WE ⁴	MASK	COLOR
BIT MASK REGISTER OPERATIONS																	
BMR-RT	BMR READ TRANSFER (DRAM-BMR TRANSFER)	1	0	1	0	0	X	1	0/1 ⁷	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM-INVERT-BMR TRANSFER)	1	0	1	0	0	X	1	0/1 ⁷	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR-DRAM TRANSFER)	1	0	0	0	0	X	1	0/1 ⁷	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR-INVERT-DRAM TRANSFER)	1	0	0	0	0	X	1	0/1 ⁷	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM-BMR TRANSFER	1	0	0	1	0	X	1	0/1 ⁷	0=SAMa 1=SAMb	X	X ⁵	TAP ⁶	X	X	—	—
BMR-SAM	BMR-SAM TRANSFER	1	0	1	1	0	X	1	0/1 ⁷	0=SAMa 1=SAMb	X	X ⁵	TAP ⁶	X	X	—	—
CLF-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1 ⁷	X	X	X ⁵	X	X	X	—	—
BIT MASKED TRANSFER OPERATIONS																	
BMRT	BIT MASKED READ TRANSFER (BM DRAM-SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—
BMSRT ⁹	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM-SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM-DRAM TRANSFER)	1	0	0	0	1	X	1	X ⁸	0=SAMa 1=SAMb	X	ROW	TAP ⁶	X	X	—	—
BMSWT ⁹	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM-DRAM TRANSFER)	1	0	0	1	1	X	1	X ⁸	0=SAMa 1=SAMb	X	ROW	TAP ⁶	DQ MASK	X	—	—
BMWT-DCM	DQ/BIT MASKED WRITE TRANSFER (BM SAM-DRAM TRANSFER)	1	0	0	1	1	X	0	X ⁸	0=SAMa 1=SAMb	X	ROW	TAP ⁶	DQ MASK	X	—	—

- NOTE:**
- 0 = LOW (V_{IL}); 1 = HIGH (V_{IH}); X = "don't care;" — = "not applicable."
 - These columns show what must be present on the A0-A8 inputs when \overline{RAS} falls and when \overline{CAS} falls.
 - These columns show what must be present on the DQ1-DQ4 inputs when \overline{RAS} falls and when \overline{CAS} falls.
 - With WRITE cycles, the input data is latched at the falling edge of \overline{CAS} or $\overline{ME/WE}$, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of \overline{CAS} or $\overline{TR/OE}$, whichever is later.
 - The ROW that is addressed will be refreshed, but no particular row address is required.
 - Tap address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERS, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A8 is a "don't care" for SPLIT TRANSFERS.
 - The serial mask input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE, DQ MASKED BIT MASKED WRITE TRANSFER or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERS to any SAM and DQ MASKED BIT MASKED WRITE TRANSFERS or BIT MASKED WRITE TRANSFERS from SAMa, the BMR is not cleared automatically.
 - If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
 - SPLIT TRANSFERS do not change SAM I/O direction.
 - SAM I/O direction is a function of the state of $\overline{ME/WE}$ at \overline{RAS} time. If $\overline{ME/WE}$ is LOW, then the selected SAM is an input; if $\overline{ME/WE}$ is HIGH, then the SAM is an output (except for SPLIT TRANSFERS).
 - The MT43C4257A/8A operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they be driven as shown in the Truth Table.

TRIPLE-PORT DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature (plastic) -55°C to +150°C
 Power Dissipation 1.5W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V _{IN} ≤ V _{CC}); all other pins not under test = 0V	I _L	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ V _{OUT} ≤ V _{CC}).	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -2.5mA, SDQs; -5mA all other outputs) Output Low Voltage (I _{OUT} = 2.5mA, SDQs; 5mA all other outputs)	V _{OH} V _{OL}	2.4	0.4	V V	1

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD, \overline{SE} a,b, DSF1,2, STS	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SCa,b SSFa,b	C _{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	C _{I/O}		9	pF	2
Output Capacitance: QSFa,b	C _O		9	pF	2

TSOP THERMAL CONSIDERATIONS (preliminary)

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	θ _{JA}	85	°C/W	
Thermal resistance - Junction to Case	θ _{JC}	15	°C/W	
Maximum Case Temperature	T _C	110	°C	

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6*	-7	-8		
OPERATING CURRENT ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling; $t_{\text{RC}} = t_{\text{RC}} [\text{MIN}]$)	I _{CC1}	95	85	75	mA	3, 4 25
OPERATING CURRENT: PAGE MODE ($\text{RAS} = V_{\text{IL}}$, $\overline{\text{CAS}}$ = Cycling; $t_{\text{PC}} = t_{\text{PC}} [\text{MIN}]$)	I _{CC2}	90	80	70	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$, after 8 $\overline{\text{RAS}}$ cycles [MIN])	I _{CC3}	8	8	8	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{CC}} - 0.2\text{V}$, after 8 $\overline{\text{RAS}}$ cycles [MIN]). All other inputs ≥ V _{CC} - 0.2V or ≤ V _{SS} + 0.2V	I _{CC4}	2	2	2	mA	
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY ($\text{RAS} = \text{Cycling}$; $\text{CAS} = V_{\text{IH}}$)	I _{CC5}	95	85	75	mA	3, 25
REFRESH CURRENT: CBR ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling)	I _{CC6}	95	85	75	mA	3, 5 25
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I _{CC7}	105	95	85	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; $t_{\text{SC}} = t_{\text{SC}} [\text{MIN}]$; $\overline{\text{SEa}}/\overline{\text{SEb}} = V_{\text{IL}}$)	I _{CC8}	35	35	25	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; $t_{\text{SC}} = t_{\text{SC}} [\text{MIN}]$; $\overline{\text{SEb}} = V_{\text{IL}}$)	I _{CC9}	20	20	15	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = V _{IH} or V _{IL} ; $\overline{\text{SEa}}/\overline{\text{SEb}} = V_{\text{IH}}$)	I _{CC10}	0	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = V _{IH} or V _{IL} ; $\overline{\text{SEb}} = V_{\text{IH}}$)	I _{CC11}	0	0	0	mA	

*Consult factory for -6 availability.

TRIPLE-PORT DRAM

TOTAL CURRENT DRAIN

(Notes 3, 4) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5V \pm 5\%$)

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC1-7}) + SAMa CURRENT (I_{CC8} or I_{CC10}) + SAMb CURRENT (I_{CC8} or I_{CC10}) + SMI CURRENT (I_{CC9} or I_{CC11}) (+ 10mA [If DRAM CURRENT = I_{CC3} or I_{CC4}])
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Example 1:

Operating current (-8) with DRAM operating in FAST-PAGE-MODE, SAMa active, SAMb and SMI inactive:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC2}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC10}) + SMI CURRENT (I_{CC11}) [+ 0] = 70 + 25 + 0 + 0 = 95mA (MAX)
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Example 2:

Operating current (-7) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC4}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC8}) + SMI CURRENT (I_{CC9}) [+ 10] = 2 + 35 + 35 + 20 + 10 = 102mA (MAX)
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TRIPLE-PORT DRAM

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±5%)

TRIPLE-PORT DRAM

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t _{RC}	110		130		150		ns	
READ-MODIFY-WRITE cycle time	t _{RWC}	150		170		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	35		40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	t _{PRWC}	85		90		95		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80	ns	14, 17
Access time from $\overline{\text{CAS}}$	t _{CAC}		15		17		20	ns	15
Access time from (TR)/OE	t _{OE}		15		20		20	ns	
Access time from column address	t _{AA}		30		35		40	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	20,000	70	20,000	80	20,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	t _{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	15		20		20		ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	15	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	60		70		80		ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10		10		10		ns	16
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	40	20	50	20	60	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		ns	
Row address setup time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		12		ns	
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	17	40	ns	18
Column address setup time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	10		12		15		ns	
Column address hold time (referenced to $\overline{\text{RAS}}$)	t _{AR}	50		55		60		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		ns	
Read command setup time	t _{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	t _{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{\text{RAS}}$)	t _{RRH}	0		0		0		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	3		3		3		ns	
Output buffer turn-off delay	t _{OFF}	3	20	3	20	3	20	ns	20, 23
Output disable	t _{OD}	3	10	3	10	3	10	ns	20, 23
Output disable hold time from start of WRITE	t _{OEH}	10		10		15		ns	27
Output Enable to $\overline{\text{RAS}}$ delay	t _{ORD}	0		0		0		ns	

*Consult factory for -6 availability.

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{CC} = 5V \pm 5\%$)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time (referenced to \overline{RAS})	t_{WCR}	45		45		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to \overline{RAS} lead time	t_{RWL}	15		20		20		ns	
Write command to \overline{CAS} lead time	t_{CWL}	15		20		20		ns	
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	10		15		15		ns	22
Data-in hold time (referenced to \overline{RAS})	t_{DHR}	45		55		55		ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	85		90		100		ns	21
Column address to \overline{WE} delay time	t_{AWD}	55		55		60		ns	21
\overline{CAS} to \overline{WE} delay time	t_{CWD}	40		40		40		ns	21
Transition time (rise or fall)	t_T	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	t_{REF}		16.7		16.7		16.7	ms	
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	0		0		0		ns	
\overline{CAS} setup time (CBR refresh)	t_{CSR}	10		10		10		ns	5
\overline{CAS} hold time (CBR refresh)	t_{CHR}	15		15		30		ns	5
$\overline{ME}/\overline{WE}$ to \overline{RAS} setup time	t_{WSR}	0		0		0		ns	
$\overline{ME}/\overline{WE}$ to \overline{RAS} hold time	t_{RWH}	10		15		15		ns	
Mask data to \overline{RAS} setup time	t_{MS}	0		0		0		ns	
Mask data to \overline{RAS} hold time	t_{MH}	15		15		15		ns	

*Consult factory for -6 availability.

TRIPLE-PORT DRAM

TRANSFER AND MODE CONTROL TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Notes 6, 7, 8, 9, 10) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{CC} = 5V \pm 5\%$)

TRIPLE-PORT DRAM

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{\text{TR}}/(\overline{\text{OE}})$ LOW to $\overline{\text{RAS}}$ setup time	${}^t\text{TLS}$	0		0		0		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ LOW to $\overline{\text{RAS}}$ hold time	${}^t\text{TLH}$	15	10,000	15	10,000	15	10,000	ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ LOW to $\overline{\text{RAS}}$ hold time (REAL-TIME READ TRANSFER only)	${}^t\text{RTH}$	60	10,000	65	10,000	70	10,000	ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ LOW to $\overline{\text{CAS}}$ hold time (REAL-TIME READ TRANSFER only)	${}^t\text{CTH}$	15		20		20		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ HIGH to SC lead time	${}^t\text{TSL}$	5		5		5		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ HIGH to $\overline{\text{RAS}}$ precharge time	${}^t\text{TRP}$	50		55		60		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ precharge time	${}^t\text{TRW}$	15		20		25		ns	
First SC edge to $\overline{\text{TR}}/(\overline{\text{OE}})$ HIGH delay time	${}^t\text{TSD}$	15		15		15		ns	
$\overline{\text{RAS}}$ to first SC edge delay time	${}^t\text{RSD}$	80		80		80		ns	
$\overline{\text{CAS}}$ to first SC edge delay time	${}^t\text{CSD}$	25		25		25		ns	
Serial output buffer turn-off delay from $\overline{\text{RAS}}$	${}^t\text{SDZ}$	7	35	7	40	10	50	ns	
SC to $\overline{\text{RAS}}$ setup time	${}^t\text{SRS}$	20		25		30		ns	
Serial data input to $\overline{\text{SE}}$ delay time	${}^t\text{SZE}$	0		0		0		ns	
$\overline{\text{RAS}}$ to SD buffer turn on time	${}^t\text{SRO}$	10		10		10		ns	
Serial data input delay from $\overline{\text{RAS}}$	${}^t\text{SDD}$	50		50		60		ns	
Serial data input to $\overline{\text{RAS}}$ delay time	${}^t\text{SZS}$	0		0		0		ns	
Serial-Input-Mode enable ($\overline{\text{SE}}$) to $\overline{\text{RAS}}$ setup time	${}^t\text{ESR}$	0		0		0		ns	
Serial-Input-Mode enable ($\overline{\text{SE}}$) to $\overline{\text{RAS}}$ hold time	${}^t\text{REH}$	15		15		15		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ HIGH to $\overline{\text{RAS}}$ setup time	${}^t\text{YS}$	0		0		0		ns	
$\overline{\text{TR}}/(\overline{\text{OE}})$ HIGH to $\overline{\text{RAS}}$ hold time	${}^t\text{YH}$	15		15		15		ns	
DSF, TRM, STS, MKD to $\overline{\text{RAS}}$ setup time	${}^t\text{FSR}$	0		0		0		ns	
DSF, TRM, STS, MKD to $\overline{\text{RAS}}$ hold time	${}^t\text{RFH}$	15		15		15		ns	
DSF to $\overline{\text{RAS}}$ hold time	${}^t\text{FHR}$	50		55		60		ns	
DSF to $\overline{\text{CAS}}$ setup time	${}^t\text{FSC}$	0		0		0		ns	
DSF to $\overline{\text{CAS}}$ hold time	${}^t\text{CFH}$	15		15		15		ns	
SC to QSF delay time	${}^t\text{SQD}$		30		30		35	ns	28
$\overline{\text{RAS}}$ to QSF delay time	${}^t\text{RQD}$		65		65		65	ns	28
$\overline{\text{CAS}}$ to QSF delay time	${}^t\text{CQD}$		35		35		35	ns	28
$\overline{\text{TR}}/\overline{\text{OE}}$ to QSF delay time	${}^t\text{TQD}$		25		25		25	ns	28
SPLIT TRANSFER setup time	${}^t\text{STS}$	25		25		30		ns	
SPLIT TRANSFER hold time	${}^t\text{STH}$	0		0		0		ns	

*Consult factory for -6 availability.

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time (Read)	t ¹ SCR	20		22		25		ns	
Serial clock cycle time (Write)	t ¹ SCW	20		20		20		ns	
Access time from SC	t ¹ SAC		20		22		25	ns	24, 30
SC precharge time (SC LOW time)	t ¹ SP	7		7		7		ns	
SC pulse width (SC HIGH time)	t ¹ SAS	7		7		7		ns	
Access time from $\overline{\text{SE}}$	t ¹ SEA		12		12		15	ns	24
$\overline{\text{SE}}$ precharge time	t ¹ SEP	7		10		10		ns	
Serial data out hold time after SC HIGH	t ¹ SOH	5		5		5		ns	24, 30
Serial output buffer turn off delay from $\overline{\text{SE}}$	t ¹ SEZ	3	12	3	12	3	12	ns	20, 24
Serial data in setup time	t ¹ SDS	0		0		0		ns	24
Serial data in hold time	t ¹ SDH	10		10		10		ns	24
Serial mask data in setup time	t ¹ MDS	0		0		0		ns	
Serial mask data in hold time	t ¹ MDH	10		10		10		ns	
SERIAL INPUT (Write) Enable setup time	t ¹ SWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	t ¹ SWH	10		10		15		ns	
SERIAL INPUT (Write) disable setup time	t ¹ SWIS	0		0		0		ns	
SERIAL INPUT (Write) disable hold time	t ¹ SWIH	10		10		15		ns	
SSF to SC setup time	t ¹ SFS	0		0		0		ns	29
SSF to SC hold time	t ¹ SFH	10		10		15		ns	29
SSF LOW to SC HIGH delay	t ¹ SFD	5		5		5		ns	29

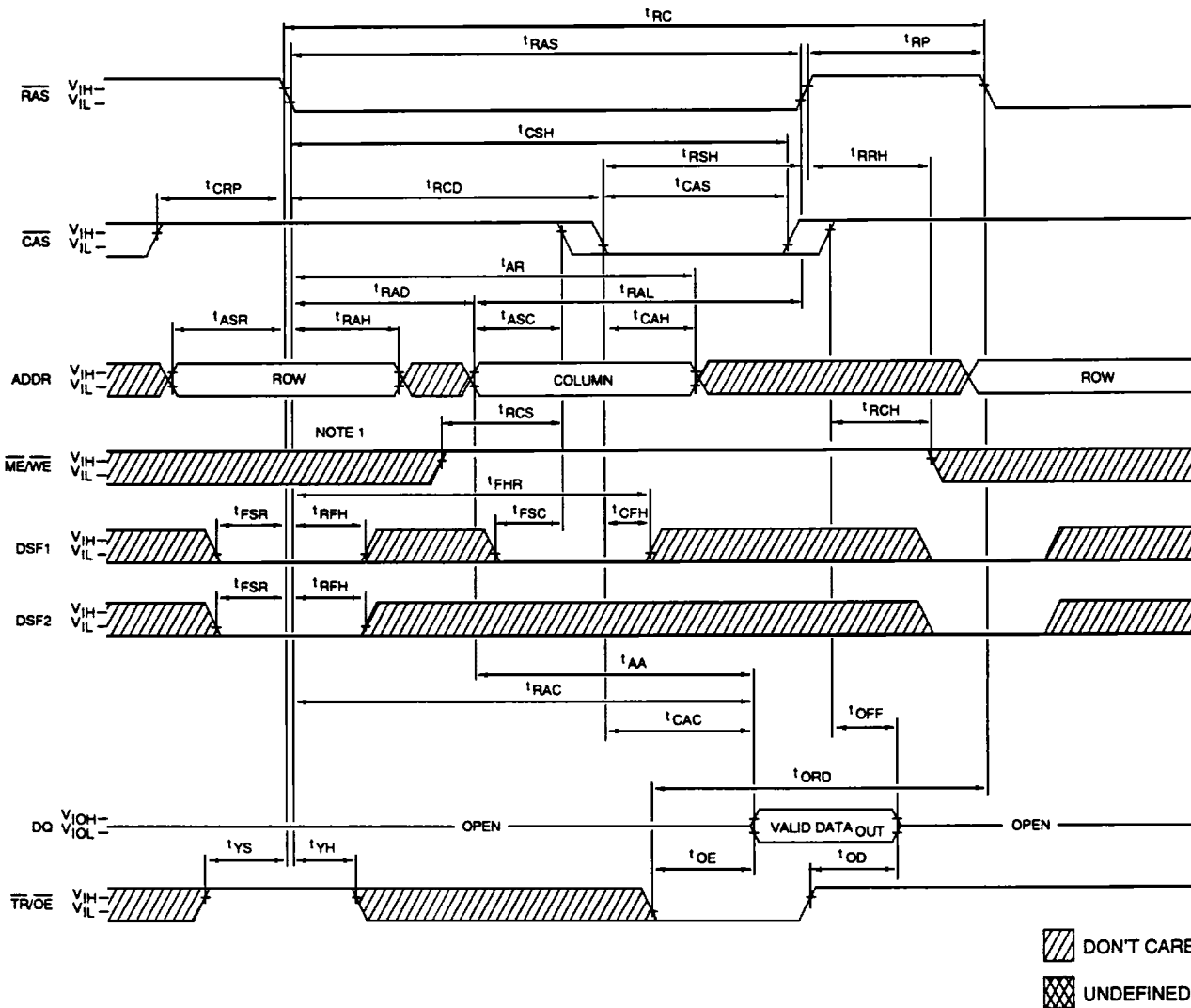
*Consult factory for -6 availability.

TRIPLE-PORT DRAM

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±5%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is assured. The 8 $\overline{\text{RAS}}$ cycle wake-up should be repeated any time the $\overline{\text{REF}}$ refresh requirement is exceeded.
8. AC characteristics assume $t_T = 3$ to 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}} = V_{IH}$, DRAM data outputs (DQ1-DQ4) are High-Z.
12. If $\overline{\text{CAS}} = V_{IL}$, DRAM data outputs (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $t_{RCD} < t_{RCD} \text{ (MAX)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD} \text{ (MAX)}$.
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for t_{CP} .
17. Operation within the $t_{RCD} \text{ (MAX)}$ limit ensures that $t_{RAC} \text{ (MAX)}$ can be met. $t_{RCD} \text{ (MAX)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} \text{ (MAX)}$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD} \text{ (MAX)}$ limit ensures that $t_{RCD} \text{ (MAX)}$ can be met. $t_{RAD} \text{ (MAX)}$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} \text{ (MAX)}$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. t_{OD} , t_{OFF} and t_{SEZ} define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS} \text{ (MIN)}$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{\text{TR}}/\overline{\text{OE}}$. If $t_{WCS} \leq t_{WCS} \text{ (MIN)}$, the cycle is a LATE-WRITE and $\overline{\text{TR}}/\overline{\text{OE}}$ must control the output buffers during the WRITE to avoid data contention. If $t_{RWD} \geq t_{RWD} \text{ (MIN)}$, $t_{AWD} \geq t_{AWD} \text{ (MIN)}$ and $t_{CWD} \geq t_{CWD} \text{ (MIN)}$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if t_{OD} and t_{OEH} are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early WRITE cycles and $\overline{\text{ME}}/\overline{\text{WE}}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{\text{TR}}/\overline{\text{OE}}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{\text{OE}}$ or $\overline{\text{CAS}}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Addresses (A0-A8) change two times or less while $\overline{\text{RAS}} = V_{IL}$.
26. Addresses (A0-A8) change once or less while $\overline{\text{CAS}} = V_{IH}$ and $\overline{\text{RAS}} = V_{IL}$.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken LOW after t_{OEH} is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
28. Applies to the MT43C4257A only.
29. Applies to the MT43C4258A only.
30. t_{SAC} is MAX at 70° C and 4.75V V_{CC}; t_{SOH} is MIN at 0° C and 5.25V V_{CC}. These limits will not occur simultaneously at any given voltage or temperature. $t_{SOH} = t_{SAC}$ - output transition time, this is guaranteed by design.

DRAM READ CYCLE



TRIPLE-PORT DRAM

NOTE: 1. While \overline{WE} is a "don't care" for the READ cycle, if \overline{WE} had been asserted LOW, the contents of the mask register would have been modified. See truth table.

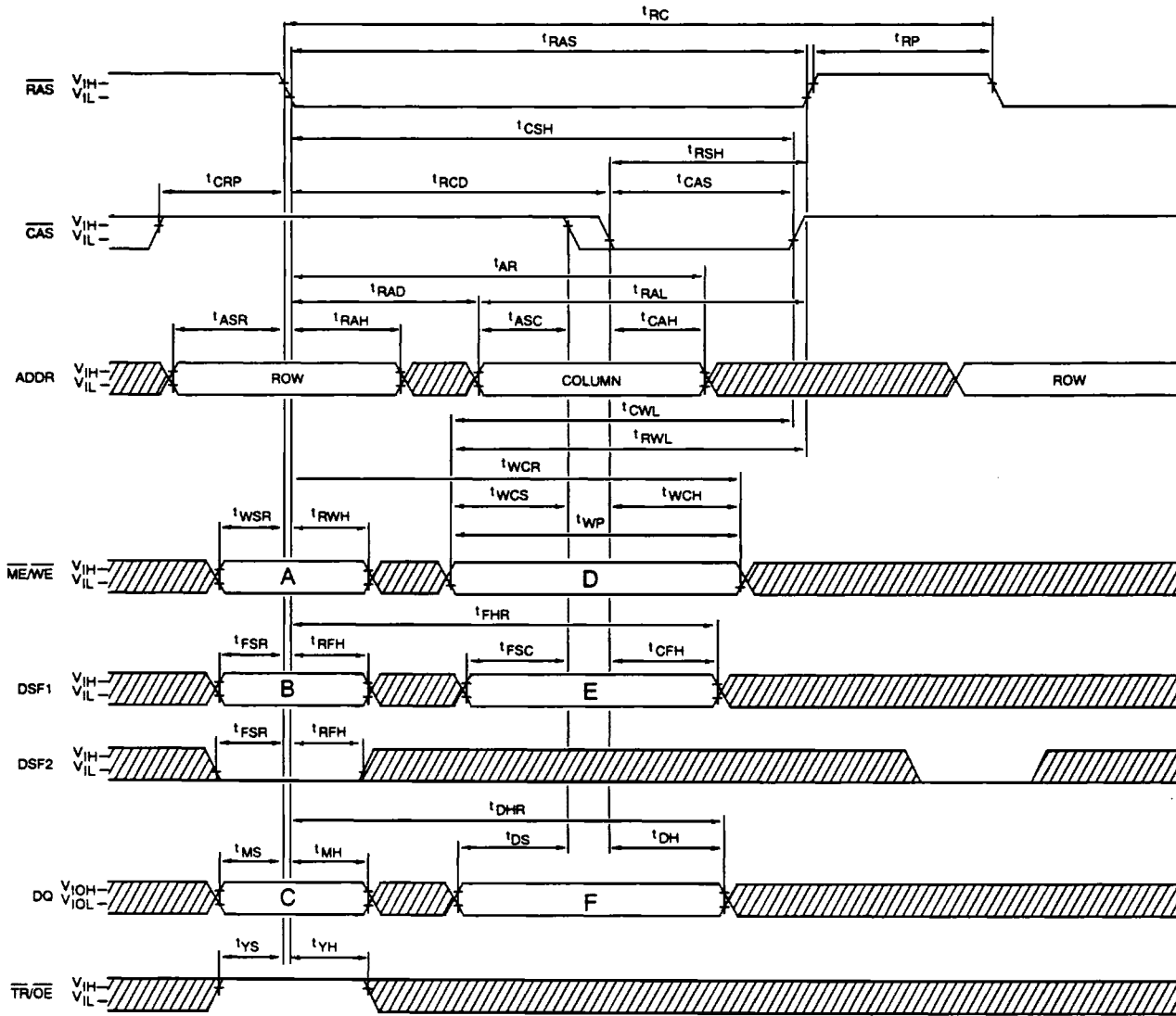
WRITE CYCLE FUNCTION TABLE 1

CODE	FUNCTION	LOGIC STATES ²					
		RAS Falling Edge			CAS Falling Edge		
		A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1 ³	0	DRAM (Masked)
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1 ³	0	DRAM (Masked)
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	X	0/1 ³	1	Column Mask
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1 ³	1	Column Mask
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	0/1 ³	1	Column Mask
LMR	Load Mask Data Register	1	1	X	0/1 ³	0	Write Mask
LCR	Load Color Register	1	1	X	0/1 ³	1	Color Mask

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
 2. TRM, MKD and STS are "don't care" for all WRITE cycles.
 3. If ME/WE is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if ME/WE falls after CAS.

TRIPLE-PORT DRAM

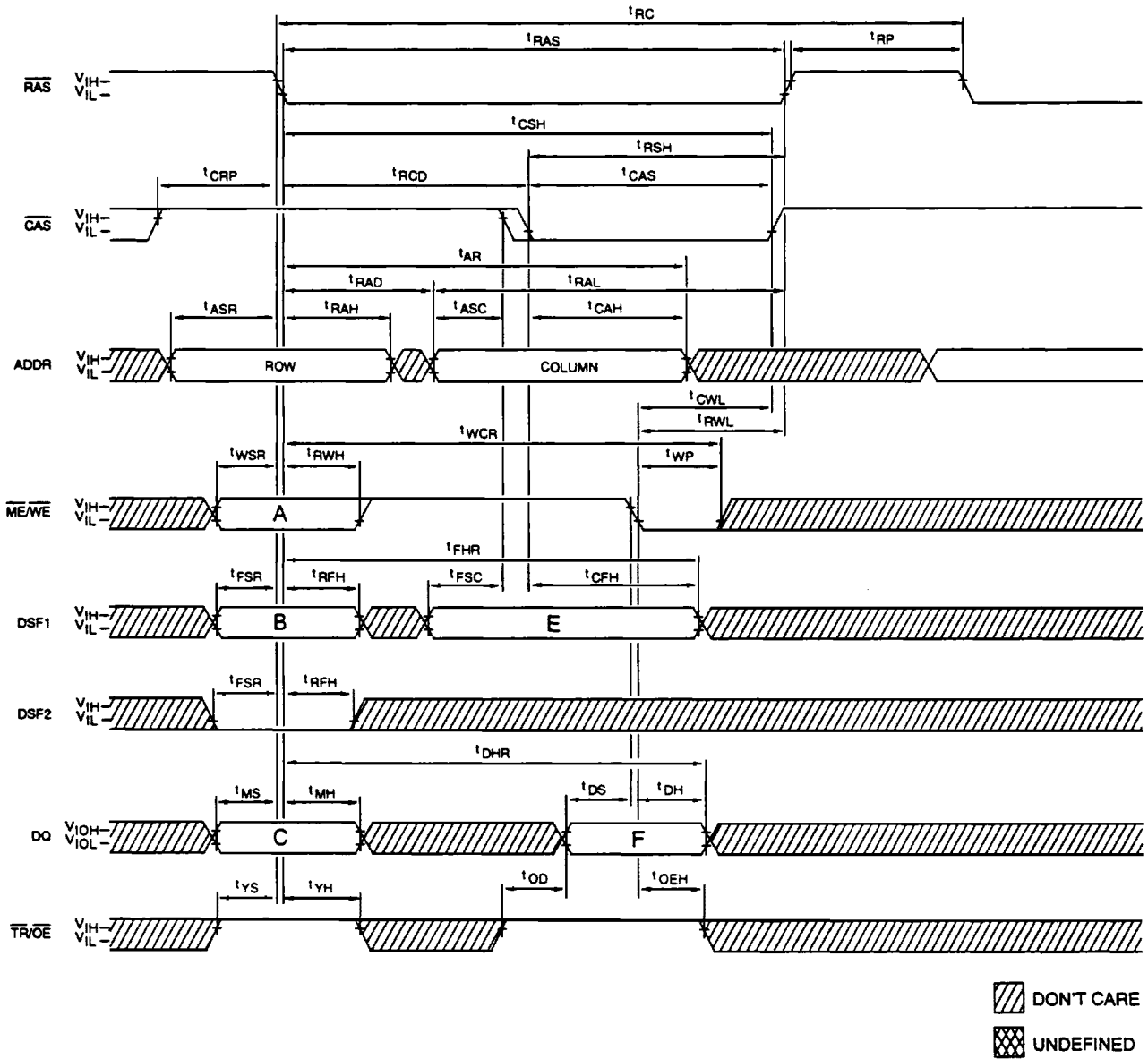
DRAM EARLY-WRITE CYCLE



 DON'T CARE
 UNDEFINED

NOTE: The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

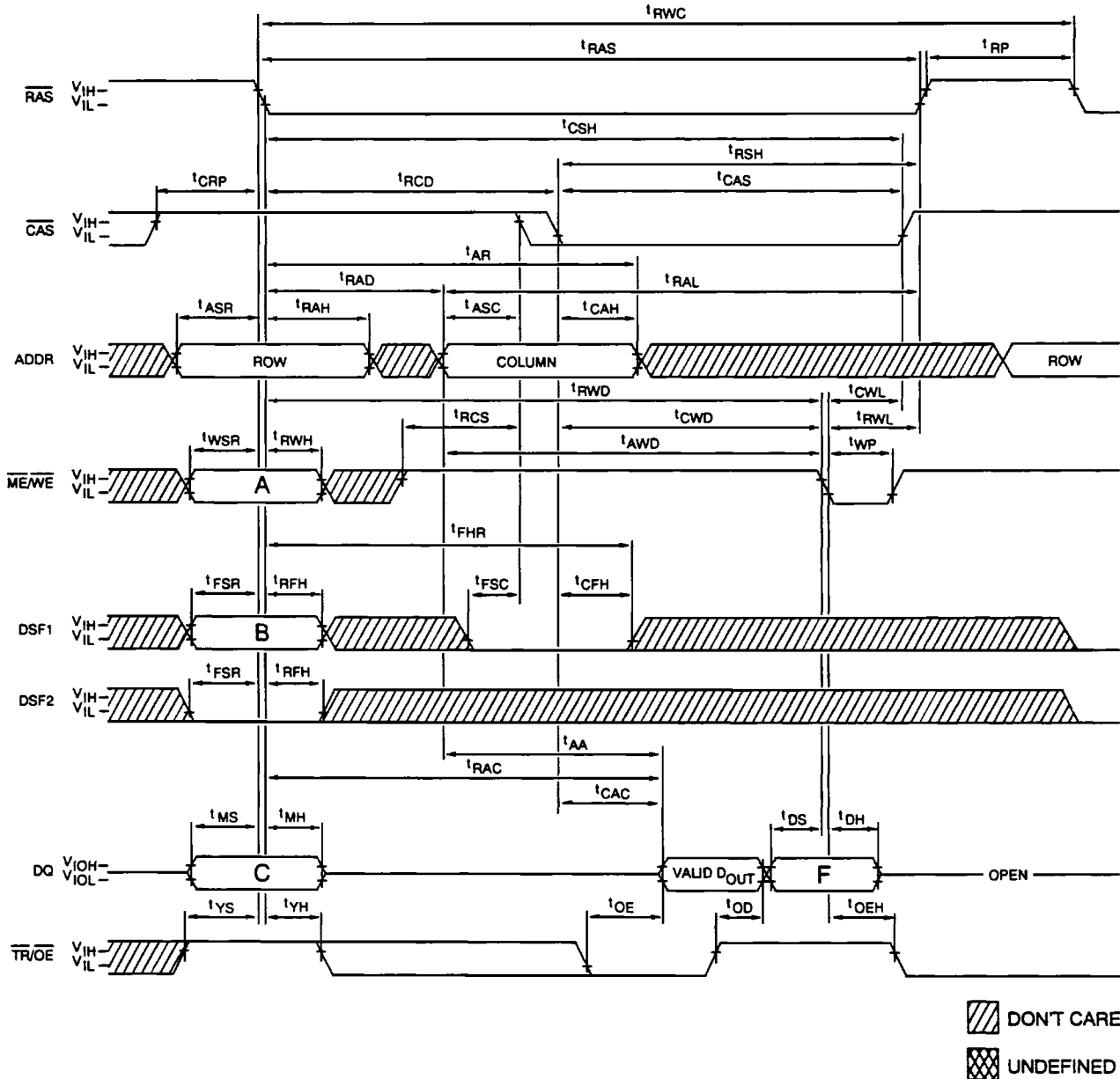
DRAM LATE-WRITE CYCLE 1



TRIPLE-PORT DRAM

NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

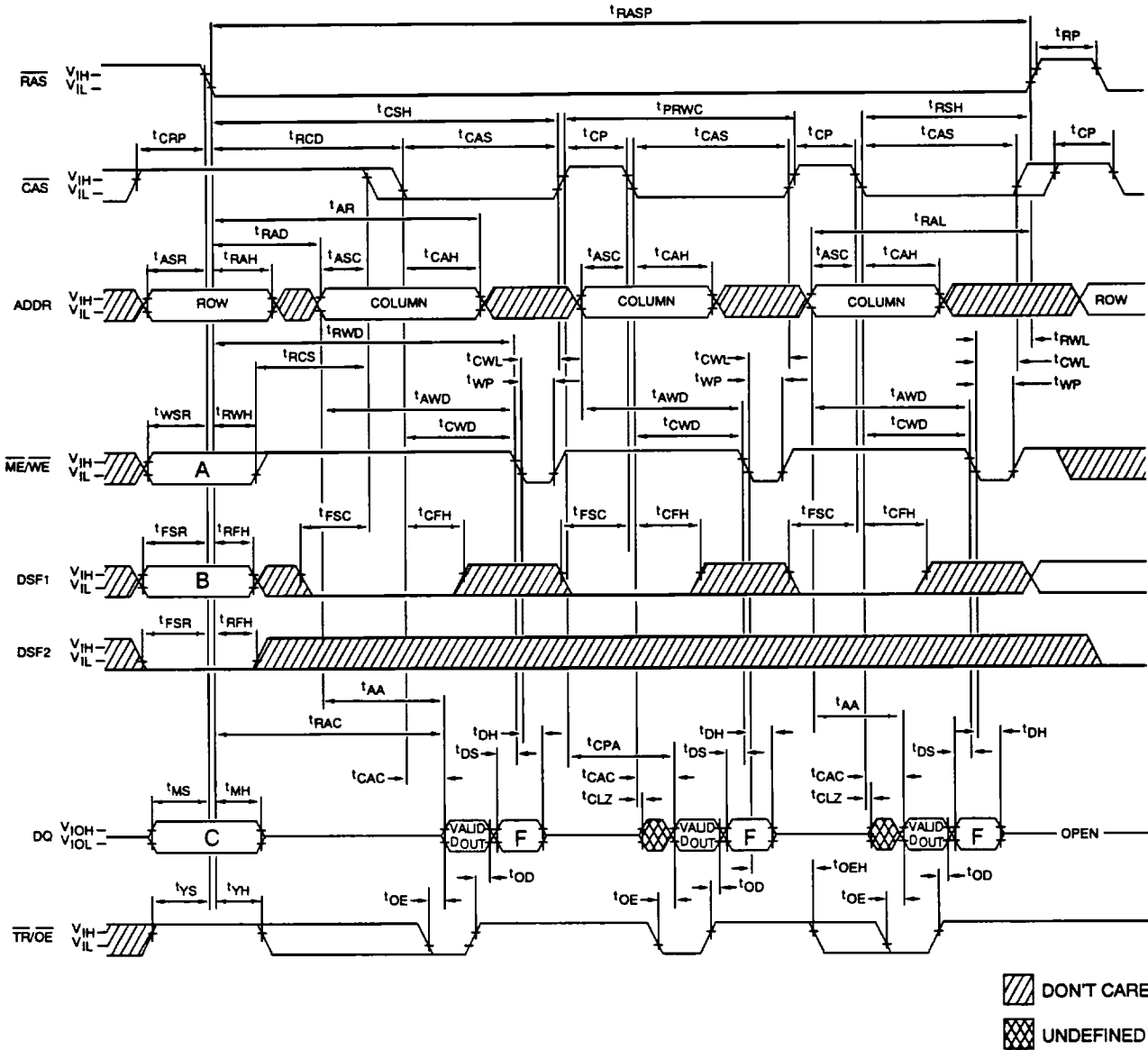
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



TRIPLE-PORT DRAM

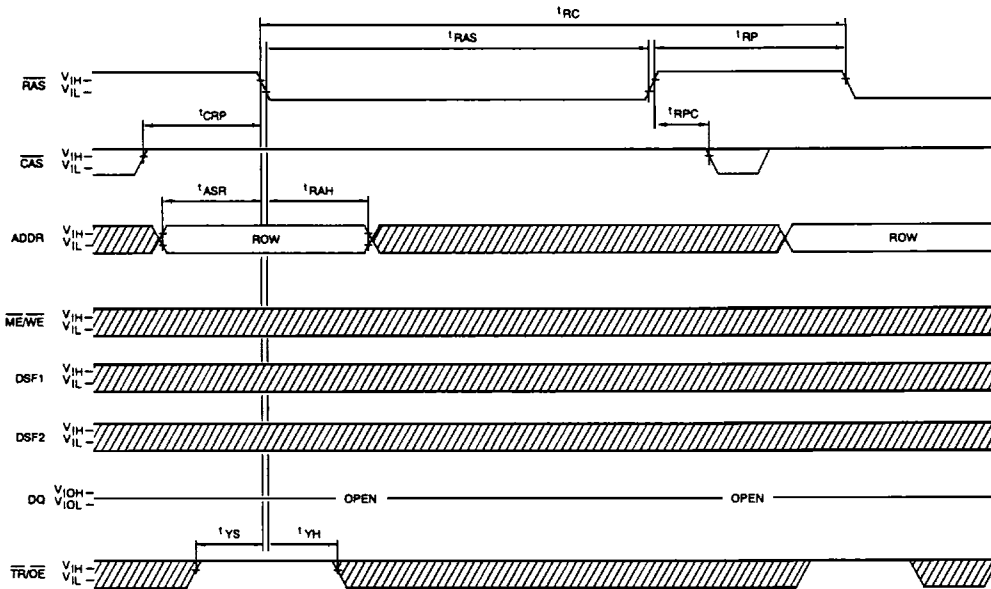
NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

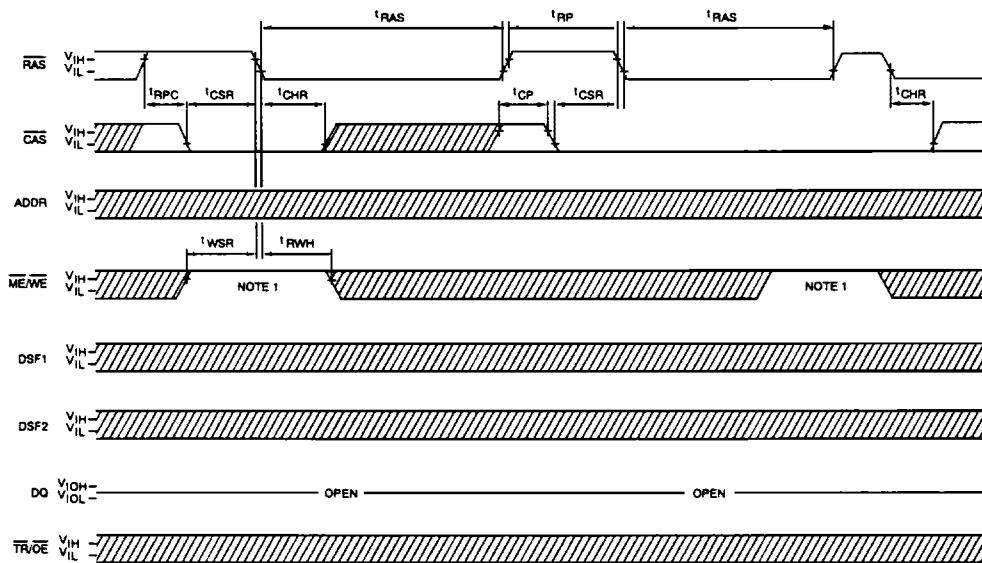


- NOTE:**
1. READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
 2. The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CBR REFRESH CYCLE

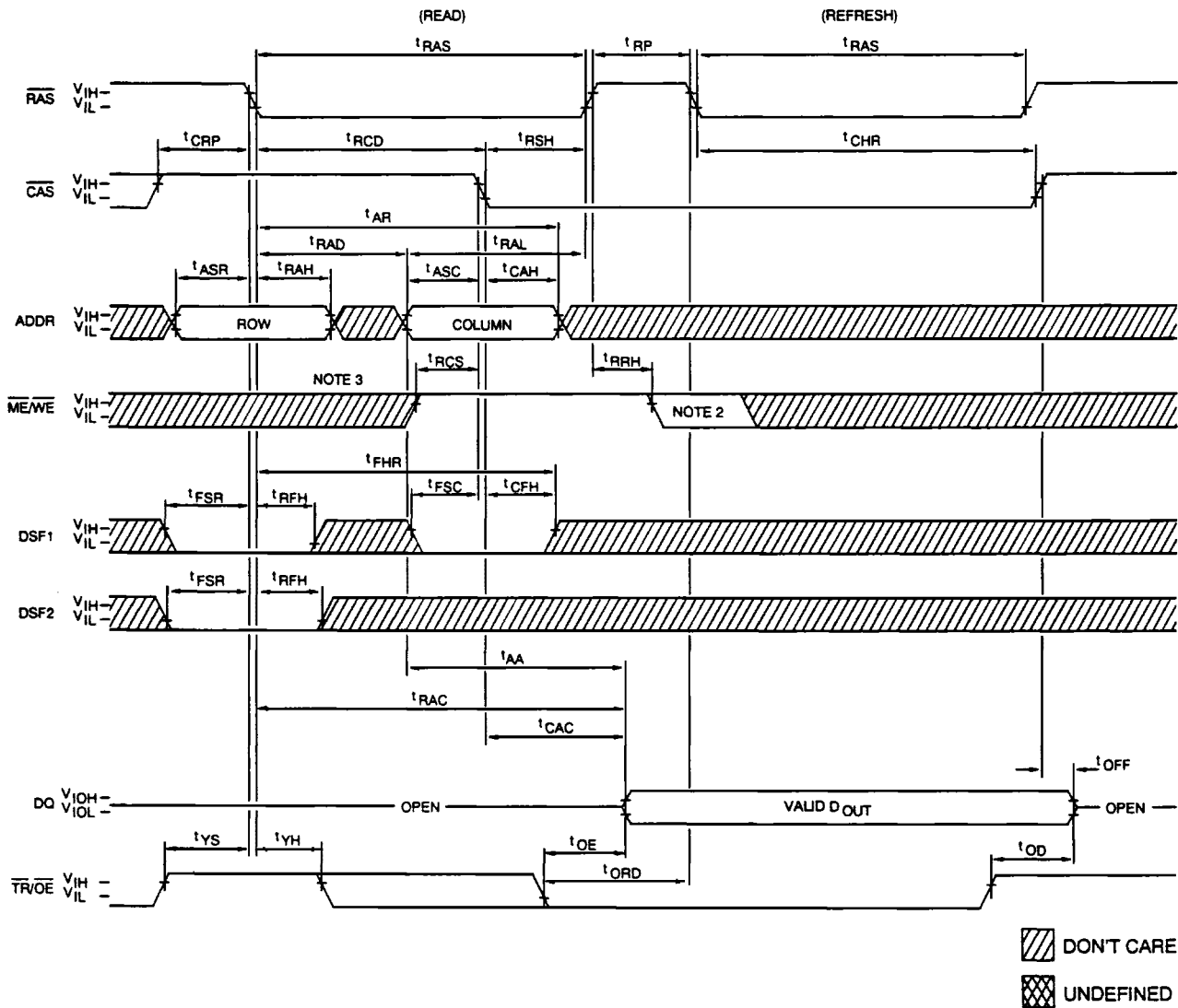


▨ DONT CARE
▩ UNDEFINED

NOTE: 1. The MT43C4257A/8A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

TRIPLE-PORT DRAM

DRAM HIDDEN-REFRESH CYCLE



- NOTE:**
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME/WE} = \text{LOW}$ (when \overline{CAS} goes LOW) and $\overline{TR/OE} = \text{HIGH}$ and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR/OE} = \text{LOW}$ (when \overline{RAS} goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR/OE}$.
 2. The MT43C4257A/8A operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.
 3. While \overline{WE} is a "don't care" for the READ cycle, if \overline{WE} had been asserted LOW, the contents of the mask register would have been modified. See truth table.

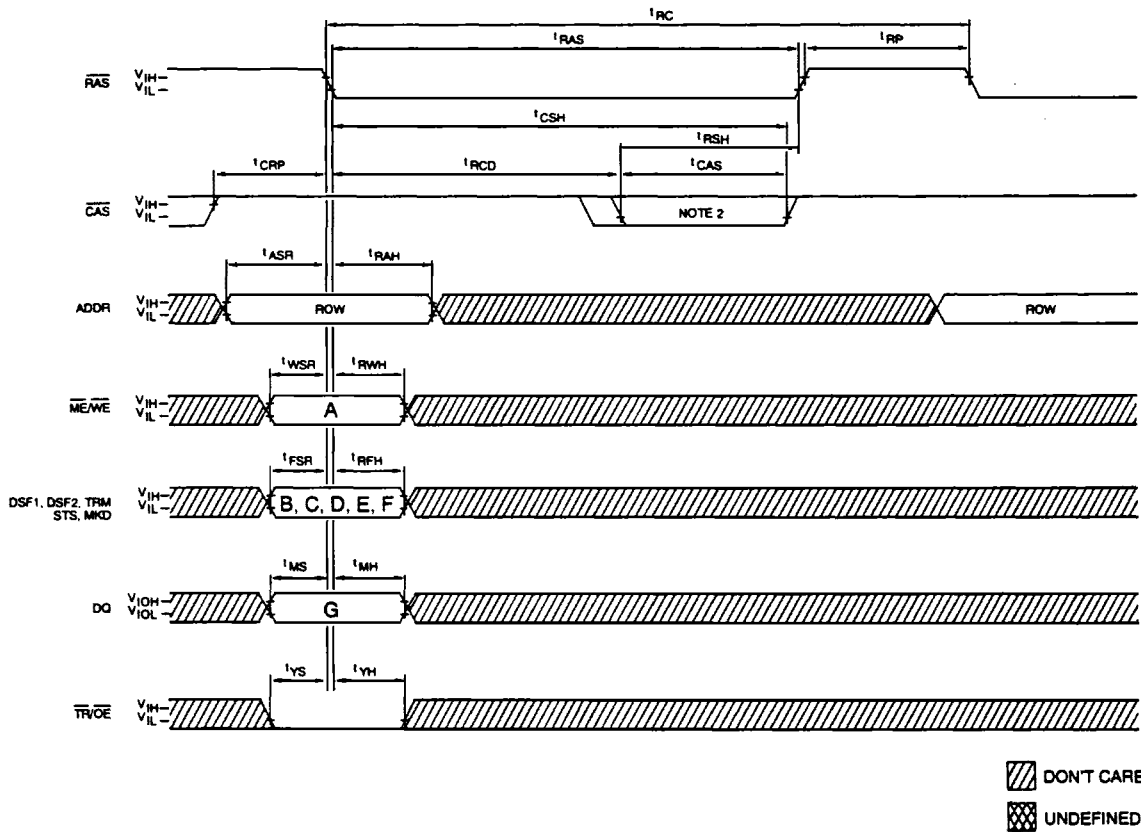
TRIPLE-PORT DRAM

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE 1

CODE	FUNCTION	LOGIC STATES						
		RAS Falling Edge						
		A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/1 ¹	X
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/1 ¹	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/1 ¹	Mask
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/1 ¹	Mask
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	X	0/1 ¹	X

TRIPLE-PORT DRAM

DRAM/BMR TRANSFERS



NOTE: 1. Serial mask input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop \overline{CAS} during a DRAM/BMR TRANSFER.

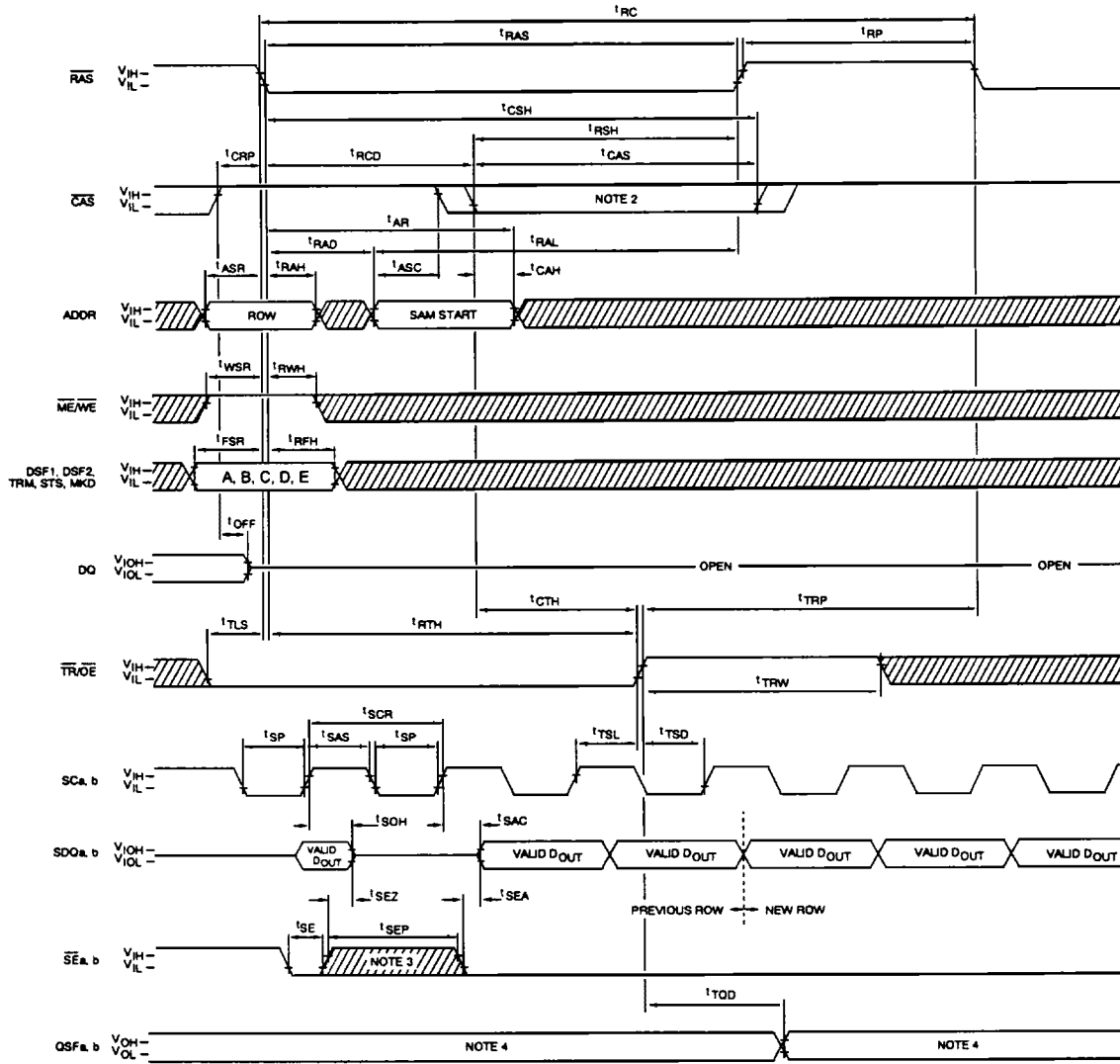
READ TRANSFER CYCLE FUNCTION TABLE ¹

CODE	FUNCTION	LOGIC STATES				
		$\overline{\text{RAS}}$ Falling Edge				
		A DSF1	B DSF2	C TRM	D STS	E MKD
RT	READ TRANSFER	0	0	0	0/1 ²	X
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/1 ²	X
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/1 ²	X
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1	1	0/1 ²	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/1 ²	0/1 ³

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
 2. The state of STS at the falling edge of $\overline{\text{RAS}}$ determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
 3. Serial mask input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

TRIPLE-PORT DRAM

**REAL-TIME READ TRANSFER 1, 5
(DRAM-TO-SAM TRANSFER)**
(When part was previously in the SERIAL OUTPUT mode)

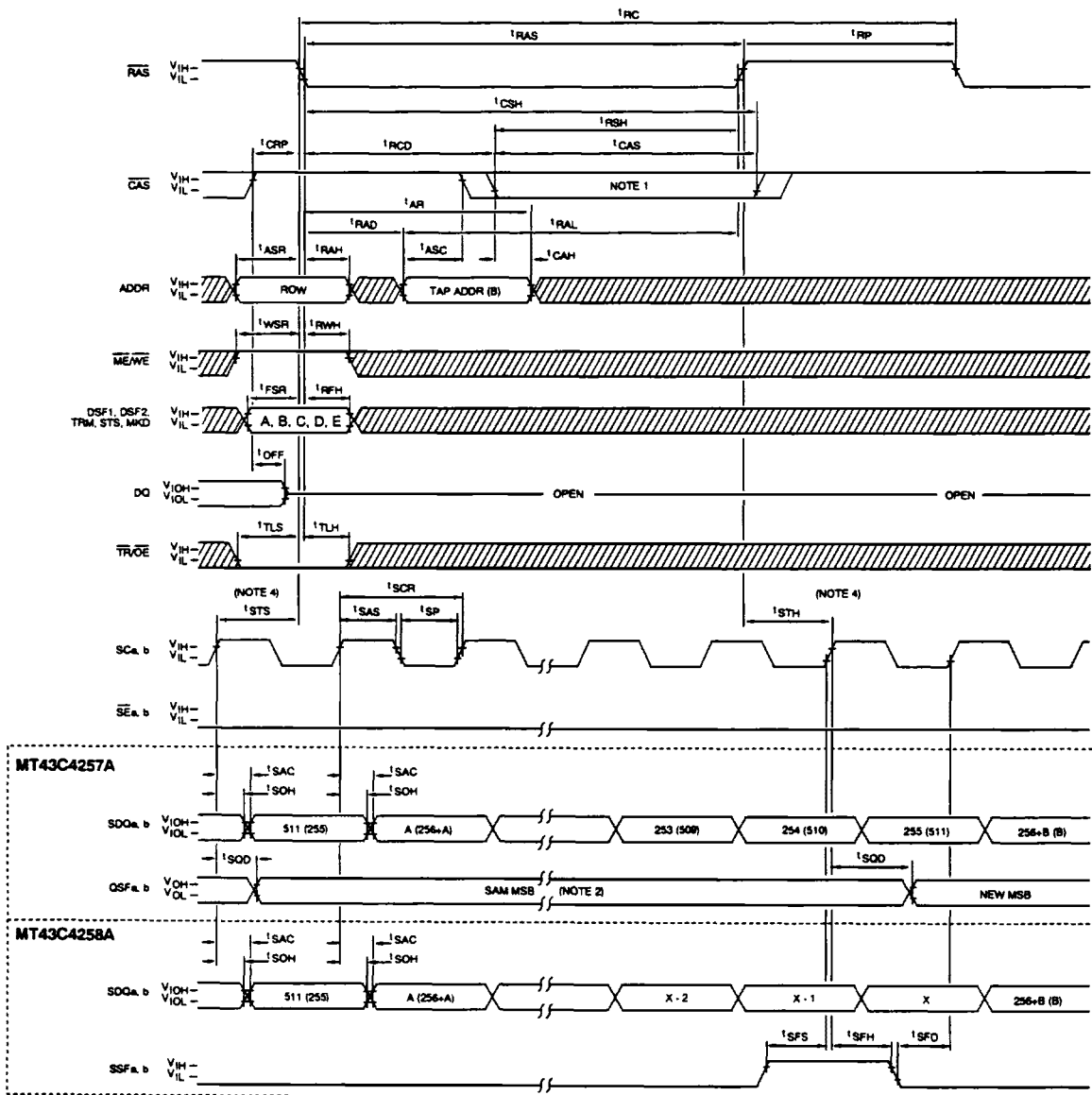


▨ DON'T CARE
▩ UNDEFINED

- NOTE:**
1. SSFa, b = "don't care" (MT43C4258A).
 2. \overline{CAS} is used to load the Tap address. If \overline{CAS} does not fall, the most recently loaded Tap address will be reused. t_{CTH} only applies if \overline{CAS} falls.
 3. The \overline{SE} pulse is shown to illustrate the serial output enable and disable timing. It is not required.
 4. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed. QSF will reflect the value of the newly loaded tap address prior to the first serial access following a full transfer operation.
 5. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

TRIPLE-PORT DRAM

**SPLIT READ TRANSFER³
(SPLIT DRAM-TO-SAM TRANSFER)**



TRIPLE-PORT DRAM

- NOTE:**
1. \overline{CAS} is used to load the Tap address. If \overline{CAS} does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
 2. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed.
 3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
 4. 'STS refers to the last serial clock cycle of the previous SAM half. 'STH refers to the last serial clock cycle of the present SAM half. 'STS represents the earliest time a serial transfer may be performed, while 'STH represents the latest time a serial transfer may be performed. These specifications ensure that transfers are not performed while the SAM counter is near a split-SAM boundary.

DON'T CARE
 UNDEFINED

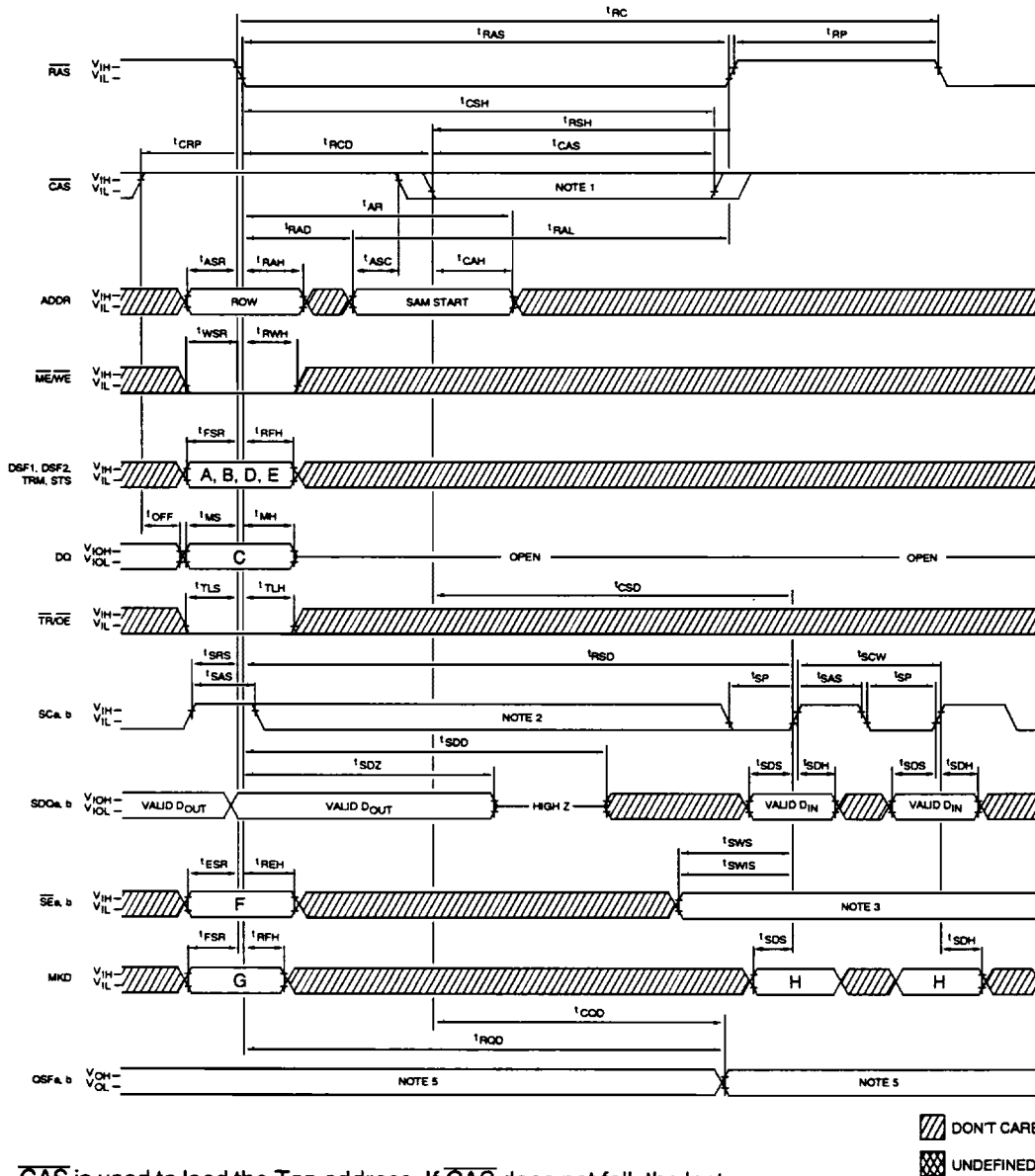
WRITE TRANSFER CYCLE FUNCTION TABLE ¹

CODE	FUNCTION	LOGIC STATES							
		RAS Falling Edge							SC
		A DSF1	B DSF2	C DQ	D TRM	E STS	F SE	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	X	0	0/1 ²	0	X	-
PWT	PSEUDO WRITE TRANSFER	0	0	X	0	0/1 ²	1	X	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/1 ²	X	X	-
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/1 ²	X	X	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	X	1	0/1 ²	X	X	0/1 ⁴
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/1 ²	X	X	0/1 ⁴
SAM-BMR	(SAM→BMR) TRANSFER	1	0	X	1	0/1 ²	X	0/1 ³	-
BMWT-DQM	DQ/BIT MASKED WRITE TRANSFER (SAM→DRAM)	1	1	Mask	0	0/1 ²	X	X	0/1 ⁴

- NOTE:**
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
 2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
 3. Serial mask input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
 4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERS to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

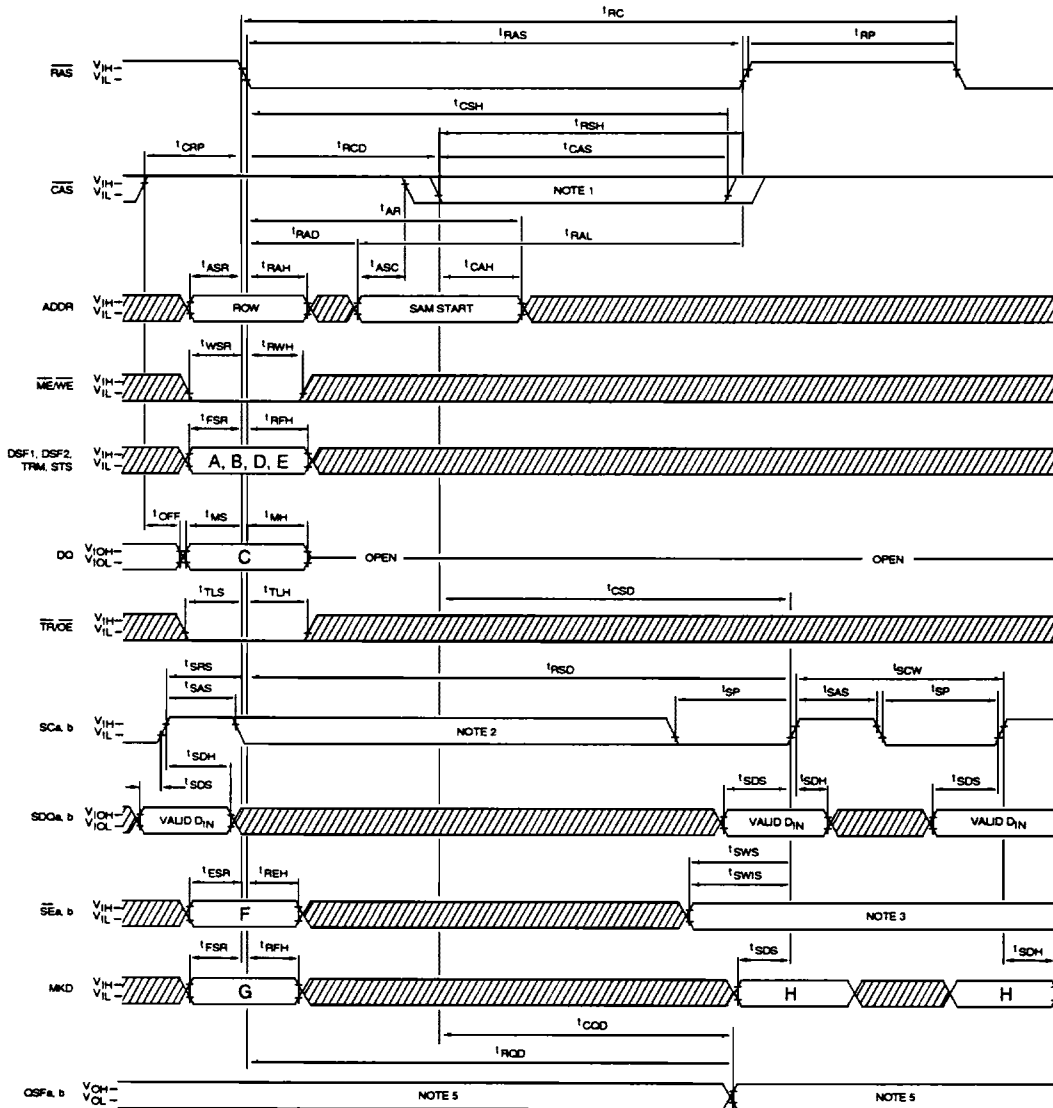
TRIPLE-PORT DRAM

WRITE TRANSFER 4
(When part was previously in the SERIAL OUTPUT mode)



- NOTE:**
1. \overline{CAS} is used to load the Tap address. If \overline{CAS} does not fall, the last Tap address loaded for the addressed SAM will be reused.
 2. There must be no rising edges on the SC input during this time period.
 3. \overline{SE} must be LOW to input new serial data, but the serial address register is incremented by SC regardless of \overline{SE} .
 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
 5. QSF = 0 when the lower SAM (bits 0–255) is being accessed. QSF = 1 when the upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258A). QSF will reflect the value of the newly loaded tap address prior to the first serial access following a full transfer operation.

WRITE TRANSFER 4
(When part was previously in the SERIAL INPUT mode)

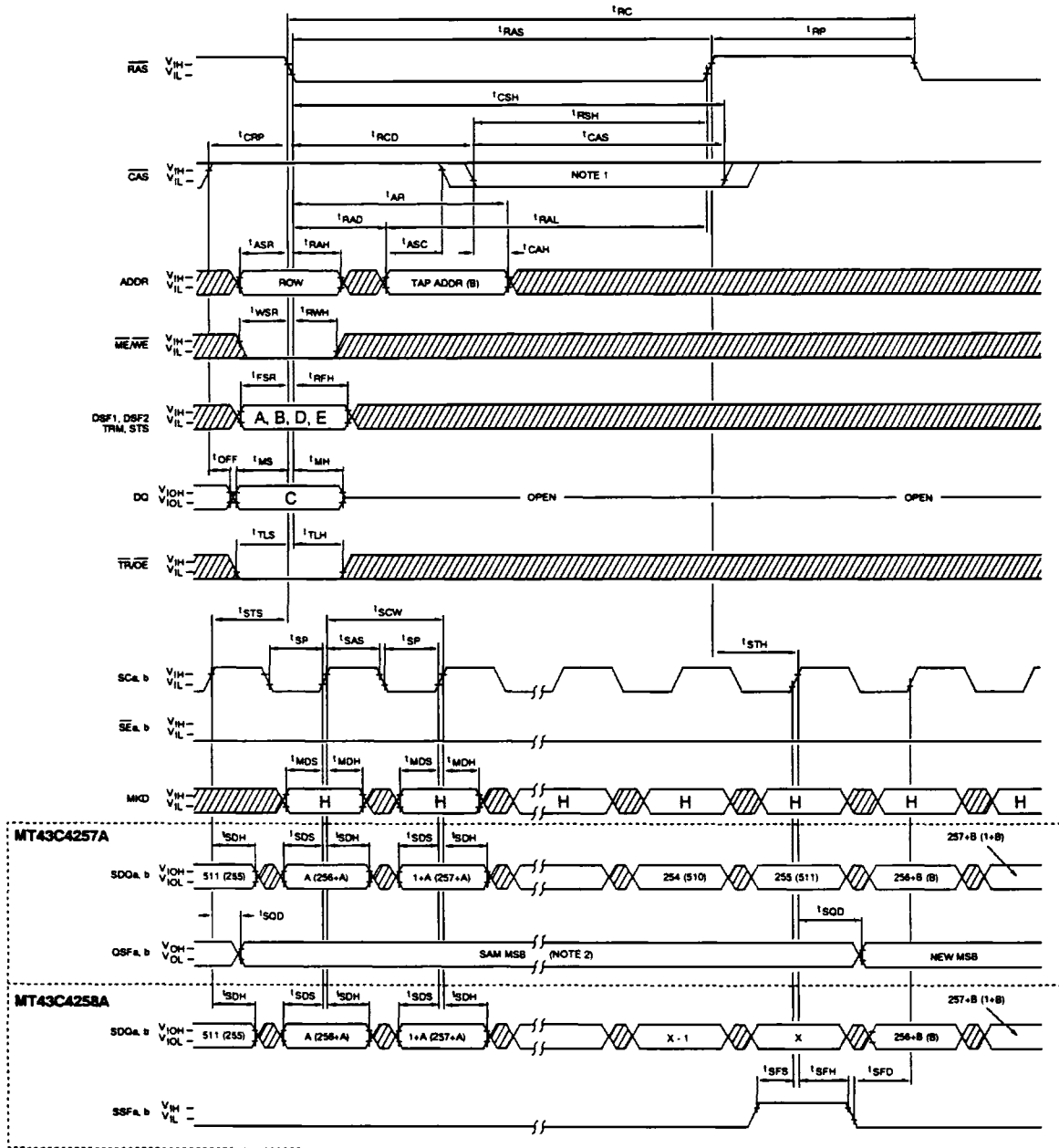


▨ DON'T CARE
▩ UNDEFINED

- NOTE:**
1. \overline{CAS} is used to load the Tap address. If \overline{CAS} does not fall, the last Tap address loaded for the addressed SAM will be reused.
 2. There must be no rising edges on the SC input during this time period.
 3. \overline{SE} must be LOW to input new serial data, but the serial address register is incremented by SC regardless of \overline{SE} .
 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
 5. QSF = 0 when the lower SAM (bits 0–255) is being accessed.
QSF = 1 when the upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258A). QSF will reflect the value of the newly loaded tap address prior to the first serial access following a full transfer operation.

TRIPLE-PORT DRAM

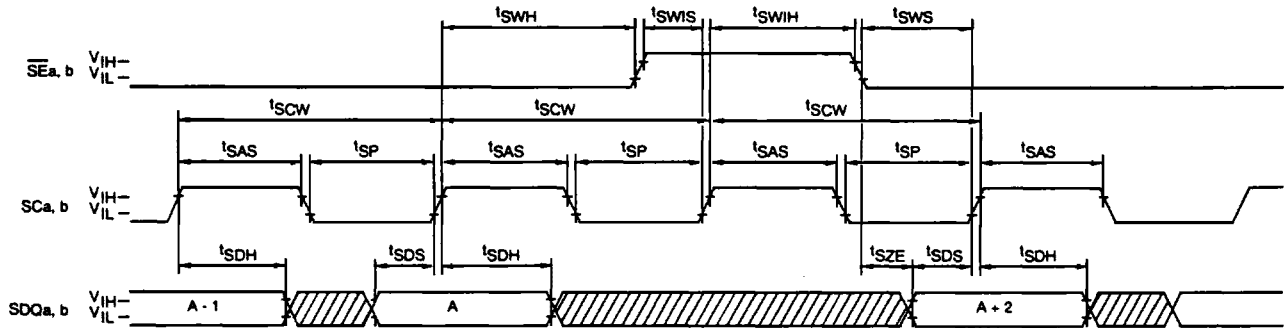
SPLIT WRITE TRANSFER ³
(SPLIT SAM-TO-DRAM TRANSFER)



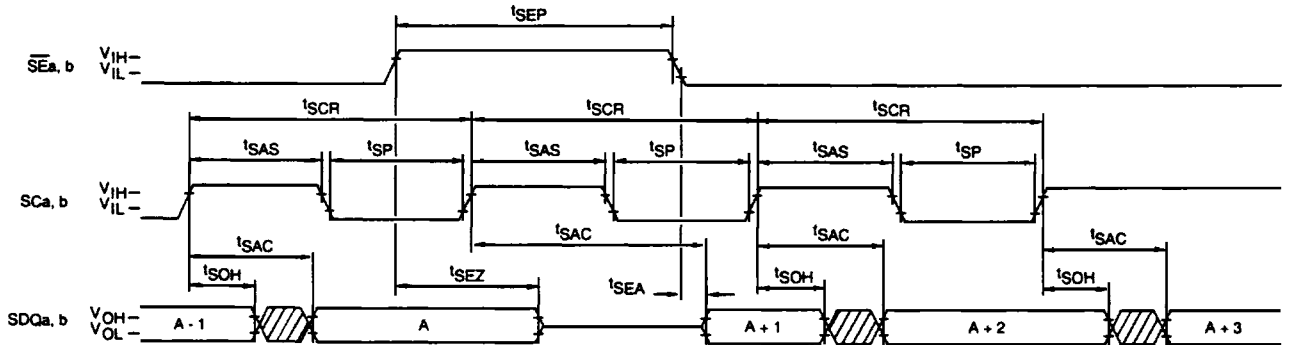
TRIPLE-PORT DRAM

- NOTE:**
1. $\overline{\text{CAS}}$ is used to load the Tap address. If $\overline{\text{CAS}}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
 2. $\text{QSF} = 0$ when the lower SAM (bits 0–255) is being accessed.
 $\text{QSF} = 1$ when the upper SAM (bits 256–511) is being accessed.
 3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



 DON'T CARE
 UNDEFINED

TRIPLE-PORT DRAM

NOTE: 1. \overline{SEa} , SCa and $SDQa$ are used when accessing \overline{SEb} ; \overline{SEb} , SCb and $SDQb$ are used when access in \overline{SEa} .