VSC8538

Octal 10/100/1000BASE-T PHY with Integrated 1.25 Gbps SerDes

Datasheet

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.0

Revision 4.0 of this datasheet was published in June 2006. The following is a summary of the changes implemented in the datasheet.

- In the DC characteristics for VDDIO at 3.3 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –42 µA minimum and 42 µA maximum.
- In the DC characteristics for VDDIO at 2.5 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –32 µA minimum and 32 µA maximum.
- In the DC characteristics for VDDIO at 1.8 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –23 µA minimum and 23 µA maximum.
- In the DC characteristics for VDDIO at 1.8 V, for the output high and low voltage parameters, new conditions were added to correlate with the output high and low current drive strength. The output high current drive strength parameter was updated from 1.0 mA to 4.0 mA maximum. The output low current drive strength parameter was updated from –1.0 mA to –4.0 mA. For more information, see Table 60, page 76.
- In the DC characteristics for VDD33 at 3.30 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –42 µA minimum and 42 µA maximum.
- For the MAC DC output characteristics, the output differential voltage was updated from 350 mV minimum, 1200 mV typical, and 1400 mV maximum to 700 mV minimum, 1000 mV typical, and 1200 mV maximum. The output rise and fall time was updated from 300 ps maximum to 200 ps maximum, and the typical value 120 ps was added. Random and deterministic jitter specifications (including footnotes) were removed and replaced with the total jitter specification. The total receive jitter tolerance parameter was added. For more information about these characteristics, see Table 62, page 77.
- In the DC characteristics for LED pins, a qualifier in the introductory paragraph was removed stating that these specifications are valid only when a voltage range of 1.3 V to 2.3 V is applied to the LED pins. For the output high and low voltage parameters, new conditions were added to correlate with the output high and low current drive strength. The output high current drive strength parameter was updated from 4.0 mA to 8.0 mA maximum. The output low current drive strength parameter was updated from –4.0 mA to –8.0 mA minimum. For more information, see Table 64, page 78.

- In the DC characteristics for JTAG pins, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –42 µA minimum and 42 µA maximum.
- For the current consumption specifications, the power consumption parameter was renamed from “worst case” to “full traffic conditions” to be technically accurate. The power consumption maximum was updated from TBD to 5.91 W. Also, in the introductory text, a reference to 64-bit was corrected to 64-byte. For more information about current consumption, see Table 66, page 79.
- For the AC clock output characteristics, the total jitter values were changed from TBD to 217 ps typical and 491 ps maximum.
- In the stress ratings, the power supply voltage parameter was removed because it was redundant. For the DC input voltage on the VDD12 and VDD12A supply pins, the maximum was updated from 1.5 V to 1.4 V. The electrostatic discharge voltage was specified as meeting a Class 2 rating. For more information about the Class 2 rating, see Table 75, page 85.
- For the serial management interface (SMI) pins, it was clarified that EECLK and EEDAT are referenced to VDD33, not VDDIO.

Revision 2.1

Revision 2.1 of this datasheet was published in March 2006. The following is a summary of the changes implemented in the datasheet:

Introduction and Overview

- The VSC8538device now supports the 100BASE-FX communication speed.
- In the high-level block diagram, representation of the XTAL pin was corrected from “XTAL 1/2” to “XTAL1” and “XTAL2.”

Functional Descriptions

- The figures for the SerDes MAC interface and SGMII MAC interface were clarified to show that the TDP and TDN pins are capacitors in series within the VSC8538 device.
- In the Cat5 Media Interface figure, the pinout order for the RJ45 was corrected.
- The “SerDes MAC-to-SerDes MAC Modes” section was removed because it does not apply to the VSC8538 device.
- New information was added about how to manually force the device to use MDI/MDI-X.
- For better document organization, the power-over-Ethernet (PoE) information now has its own heading.
- In the far-end loopback diagram, the loopback arrow for the PHY port was redrawn closer to the MAC to more accurately portray the data path.
- In the discussion of GPIO pins, the total number was corrected from eight to 16. You cannot configure the SIGDET pins as GPIO pins, as was previously mentioned.

- For the JTAG IDCODE binary values, the device version number was corrected from 0000 to 0001.

Configuration (Registers)

- In the mode status register (address 1), the descriptions for bits 14:13 were corrected from 100BASE-X to 100BASE-TX.
- In the identifier 2 register (address 3), which enables device identification, the default for bits 9:4 was modified from 0010000 to 101000. The default for bits 3:0 was modified from 0000 to 0001.
- The address for the CRC good counter register was corrected from 31E (0x1F) to 18E (0x12).
- In the ActiPHY™ control register (address 20E), bit 15, formerly reserved, is now used to disable the carrier extension.
- Information about the CMODE pins was expanded and corrected.

Electrical Specifications

- In the DC characteristics for pins referenced to VDDIO at 1.8 V, the output low current drive strength parameter changed from maximum 4.5 mA to 1.0 mA. The output high current drive strength parameter changed from minimum –4.5 mA to –1.0 mA.
- In the DC characteristics for the MAC output pins, the values for the output common mode voltage parameter were converted from volts to millivolts. The maximum for this parameter was modified from 600 mV to 610 mV. References to the SER_DOP and SER_DIP pins were removed (these pins are not available in VSC8538).
- In the DC characteristics for the MAC input pins, the minimum value for the peak-to-peak input differential voltage parameter was modified from 100 mV to 120 mV. References to the SER_DOP and SER_DIP pins were removed (these pins are not available in VSC8538).
- In the DC characteristics for LED[3:0]_*n* pins, the output low current drive strength parameter changed from maximum 8.0 mA to 4.0 mA. The output high current drive strength parameter changed from minimum –8.0 mA to –4.0 mA.
- For the current consumption specifications, information was removed explaining how to calculate the current consumption when using ActiPHY. Information about running eight ports in SerDes/SGMII to 1000BASE-X mode was also removed. This information is not required.
- For the reference clock input specifications using the 25 MHz crystal clock input option, the maximum crystal equivalent series resistance was corrected from 300 Ω to 30 Ω.
- The device reset specifications were thoroughly updated to match the device.

Pin Descriptions

- For better organization, the GPIO pins are now listed in their own section; they were grouped with the SerDes MAC interface pins in the prior revision.

- In the list of JTAG pins, in the description for the NTRST (T3) pin, ground was incorrectly referred to as VSSIO; it is now corrected to VSS.
- In the description for the miscellaneous pins REF_FILT_A and REF_FILT_B, the external connection for these pins was corrected from a 2 kΩ resistor to 1 µF capacitor.

Package Information and Errata

- The body thickness dimensions were corrected in the package drawing and description.
- New errata were added, and all prior errata were removed because they no longer apply to this revision.

Revision 2.0

Revision 2.0 of this datasheet was published in September 2005. This was the first publication of the document.

1 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC8538 Octal 10/100/1000BASE-T PHY with Integrated 1.25 Gbps SerDes.

In addition to the datasheet, Vitesse maintains an extensive part-specific library of support and collateral materials that you may find useful in developing your own product. Depending upon the Vitesse device, this library may include:

- Software Development Kits with sample commands and scripts
- Reference designs showing the Vitesse device built in to applications in ways intended to exploit its relative strengths
- Presentations highlighting the operational features and specifications of the device to assist in developing your own product road map
- Input/Output Buffer Information specification (IBIS) models to help you create and support the interfaces available on the particular Vitesse product
- Application notes that provide detailed descriptions of the use of the particular Vitesse product to solve real-world problems
- White papers published by industry experts that provide ancillary and background information useful in developing products that take full advantage of Vitesse product designs and capabilities
- User guides that describe specific techniques for interfacing to the particular Vitesse products

Visit and register as a user on the Vitesse Web site to keep abreast of the latest innovations from research and development teams and the most current product and application documentation. The address of the Vitesse Web site is www.vitesse.com.

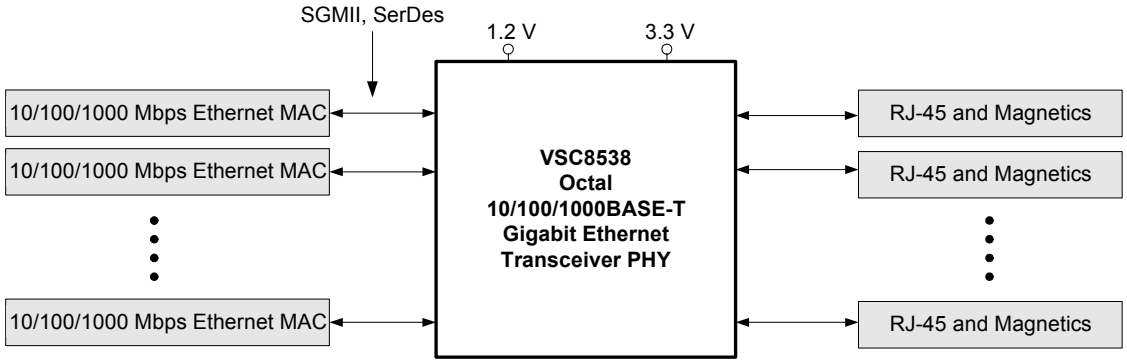
2 Product Overview

The VSC8538 device is a low-power, octal Gigabit Ethernet transceiver with an integrated 1.25 Gbps SerDes interface. It is designed for use in applications such as multiport switches and routers, where its compact ball grid array (BGA) packaging, low electromagnetic interference (EMI) line driver, and integrated line side termination resistors conserve both power and PC board space. Using the VSC8538 device in your design makes it possible to lower the component count of your PC board, sub-assembly, or device without sacrificing chip-centric capabilities or utility; which in turn can make it less expensive to produce and more cost-effective to deploy.

Vitesse's mixed signal and digital signal processing (DSP) architecture—a key operational feature of the VSC8538 device—assures robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 140 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environment and system electronic noise. This device also supports 100BASE-FX to connect to fiber modules, such as GBICs and SFPs.

The following illustration shows a high-level, generic view of a VSC8538 application.

Figure 1. Typical Application



2.1 Features and Benefits

This section lists key aspects of the VSC8538 device functionality and design that distinguish it from similar products.

Table 1. Features and Benefits

Feature	Benefit
650 mW per port power consumption (when configured for 1000BASE-T operation)	Lowers system cost by eliminating the need for extra heat-dissipating and power-processing components; simplifies system design
27 mm x 27 mm, 444-pin BGA packaging	Facilitates single row, high port density switch designs
Patented, low EMI line driver with integrated line side termination resistors	Eliminates the need for as many as 384 passive components in 48-port switch applications

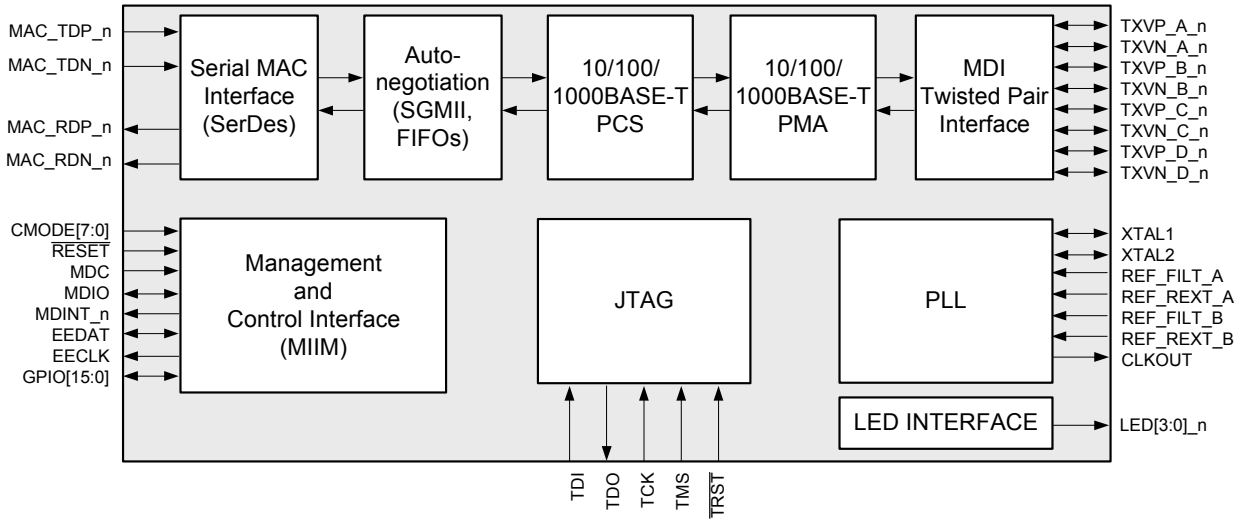
Table 1. Features and Benefits *(continued)*

Feature	Benefit
Compliance with IEEE standard 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T, 1000BASE-X, 100BASE-FX)	Ensures seamless deployment in devices throughout existing copper networks while maintaining excellent tolerance to ambient electronic noise and any substandard cabling
Support for frame sizes greater than 16 kilobytes at all device throughput settings, programmable synchronization FIFO buffers	Provides for maximum Jumbo frame sizes on custom SANs and LANs
Four integrated and programmable LED direct drivers per port, on-chip filtering and support for bi-color LEDs	Eliminates the need for external components, lowers EMI generation, lowers design cost
Multiple built-in testing facilities, including near end, far end, and connector loopback; Ethernet packet generator with CRC error counter	Lowers system or device development and deployment costs; decreases time-to-market
Serial LED interface option	Enables design flexibility
Support for the CISCO specification for serial gigabit media-independent interface version 1.7 (SGMII (v1.7), for 1000BASE-X MACs, for IEEE standard 1149.1-1999 JTAG boundary scan, and for IEEE standard 1149.6 AC-JTAG scan.	Saves manufacturing and quality assurance costs
VeriPHY™ cable diagnostics	Enables system managers to simplify deployment and improve Gigabit Ethernet network performance

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8538 device.

Figure 2. High-level Block Diagram



3 Functional Descriptions

This section provides detailed information about how the VSC8538 device works, what configurations and operational features are available, and how to test its function. It includes descriptions of the various device interfaces and how to set them up.

With the information in this section, you can better determine which device setup parameters you must access to configure the VSC8538 device to work in your application. There are three ways to configure the VSC8538 device. You can access and set its internal memory registers, you can use a combination of the device CMODE pins and its registers, or you can configure and connect an external EEPROM to execute a configuration sequence upon system startup.

For information about VSC8538 device registers, see "Registers," page 39.

For information about the device CMODE pins, see "CMODE," page 68.

For information about using an EEPROM with the VSC8538 device, see "EEPROM," page 71.

3.1 Operating Modes

With respect to its function in your design, the VSC8538 device acts as the interface between a media access controller (MAC) and Category 5 (Cat5) media or 100BASE-FX fiber media.

Depending upon the speed of data throughput required in your application, the MAC may be either a SerDes or an SGMII device.

The operating mode you choose when setting up the VSC8538 device is a function of which type of MAC is to be connected and which data throughput speed is required. The following table shows the relationship between the VSC8538 device operating mode and the data throughput speed between the Vitesse device and the MAC that is connected to it.

Table 2. Operating Mode versus Speed

VSC8538 Mode	Supported Speed
SerDes MAC-to-Cat5 Link Partner	1000BASE-T only
SGMII MAC-to-Cat5 Link Partner	10BASE-T, 100BASE-T, or 1000BASE-T
SGMII MAC-to-100BASE-FX Link Partner(1)	100BASE-FX

1. Support for this communication speed is facilitated by using the connections on the Cat5 copper pins. For more information about this mode, see "SGMII MAC-to-100BASE-FX Mode," page 21.

3.1.1 SerDes MAC-to-Cat5 Mode MAC Interface

When connected to a SerDes MAC, the VSC8538 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported. So to

configure the device to operate in this mode, select the 1000BASE-T only setting in the registers, using the CMODE pin, or in the external EEPROM startup sequence.

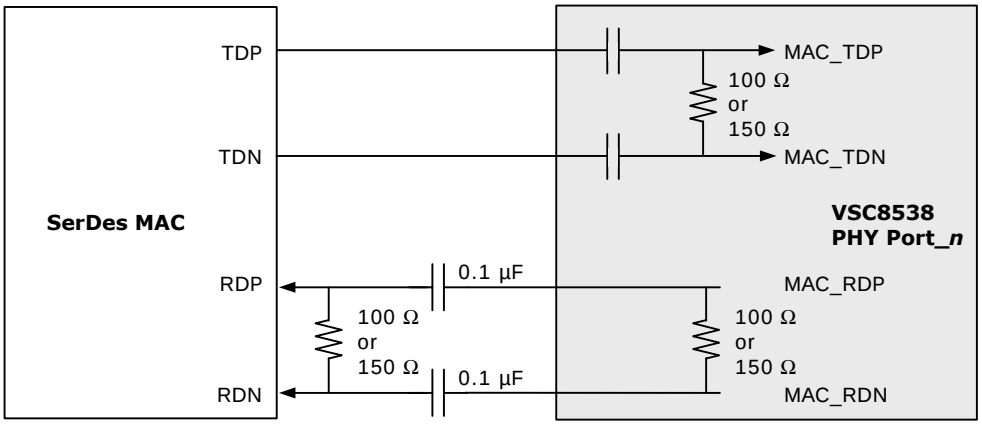
For information about using the device registers to configure the VSC8538 device to operate in SerDes MAC-to-Cat5 mode, see "Mode Control," page 42.

For information about the device CMODE pins, see "CMODE," page 68.

For information about using an EEPROM with the VSC8538 device, see "EEPROM," page 71.

The following illustration shows a typical connection of the VSC8538 device to a SerDes MAC.

Figure 3. SerDes MAC Interface



3.1.2 SGMII MAC-to-Cat5 Mode MAC Interface

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8538 device can be connected to an SGMII-compatible MAC.

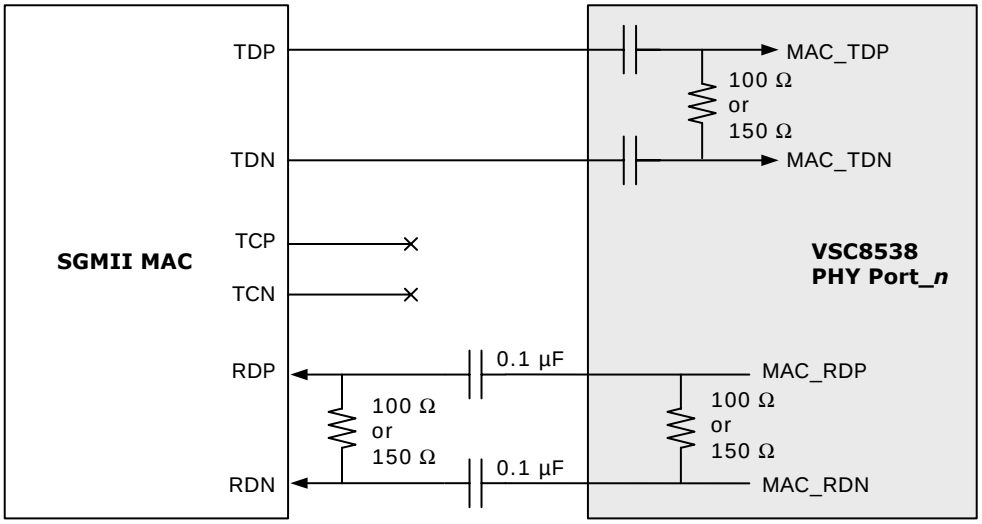
For information about using the device registers to configure the VSC8538 device to operate in SerDes MAC-to-Cat5 Mode, see "Mode Control," page 42.

For information about the device CMODE pins, see "CMODE," page 68.

For information about using an EEPROM with the VSC8538 device, see "EEPROM," page 71.

The following illustration shows a typical connection of the VSC8538 device to an SGMII-compatible MAC.

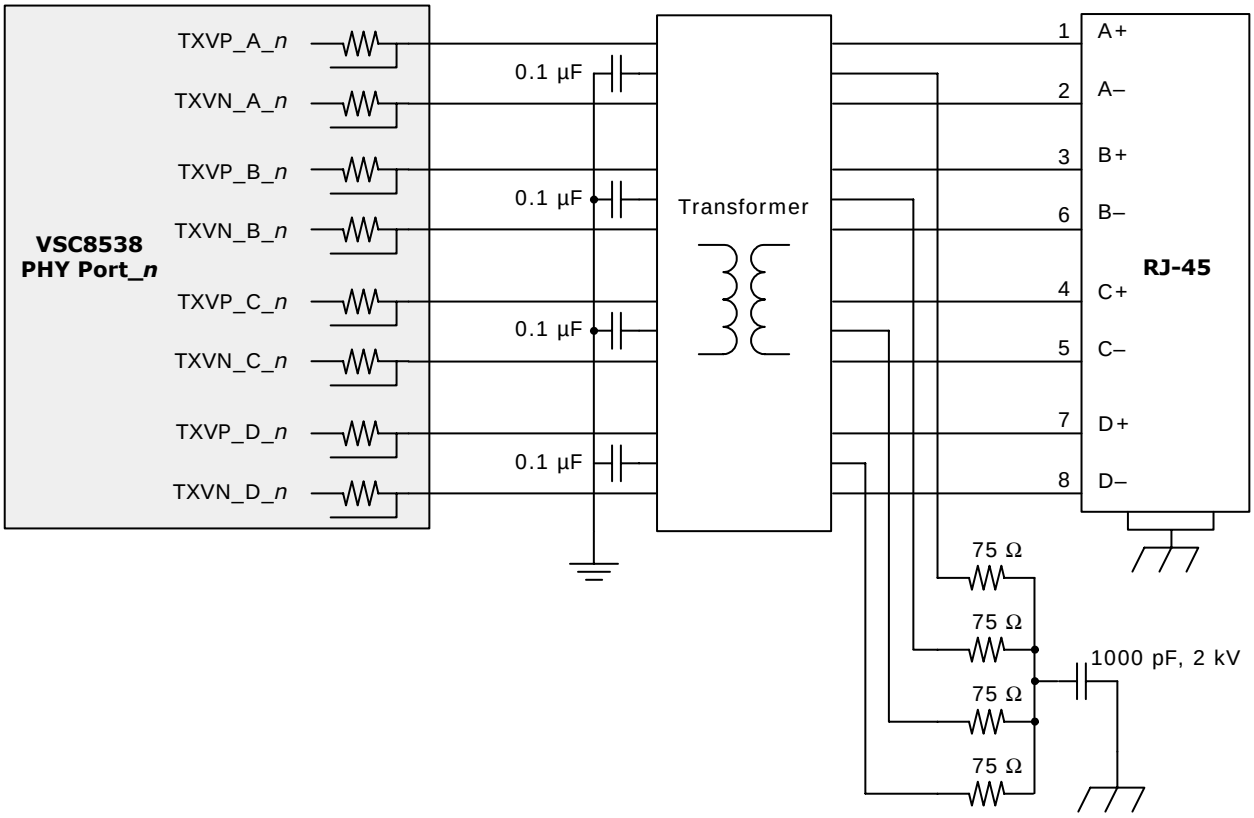
Figure 4. SGMII MAC Interface



3.1.3 All Modes Cat5 Media Interface

The VSC8538 device twisted pair interface is compliant with the IEEE standard 802.3-2000. Unlike many other gigabit PHYs, the VSC8538 device uses fully integrated, passive components (required to connect the PHY's Cat5 interface to an external 1:1 transformer). The following illustration shows the connections.

Figure 5. Cat5 Media Interface



3.2 SGMII MAC-to-100BASE-FX Mode

The VSC8538 can support the 100BASE-FX communication speed to connect to fiber modules, such as GBICs and SFPs. This capability is facilitated by using the connections on the Cat5 copper pins.

This feature is enabled using register 18G. In this mode, the SIGDET pin is not used. Also relevant in this mode are the Link100 LED and the Link LED, as well as the device auto-negotiation advertisement register (address 4).

3.3 Cat5 Auto-Negotiation

The VSC8538 device supports twisted pair auto-negotiation as defined by clause 28 of the IEEE standard 802.3-2000.

The auto-negotiation process consists of the evaluation of the advertised capabilities of the PHY and its link partner to determine the best possible operating mode; throughput speed, duplex configuration, and master or slave operating modes in the case of 1000BASE-T setups. Auto-negotiation also allows a connected MAC to communicate with its link partner MAC through the VSC8538 device using optional “next pages,” setting attributes that may not otherwise be defined by the IEEE standard.

In installations where the Cat5 link partner does not support auto-negotiation, the VSC8538 automatically switches to use parallel detection to select the appropriate link speed.

Clearing VSC8538 device register 0, bit 12 disables clause 28 twisted-pair auto-negotiation. If auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode. For more information about configuring auto-negotiation, see "IEEE Standard and Main Registers," page 41.

3.4 Manual MDI/MDI-X Setting

As an alternative to Auto MDI/MDI-X detection, you can force the PHY to be MDI or MDI-X by using the following scripts.

Format:

```
Phywrite ( register(dec), data(hex) )

Phywritemask ( register(dec), data(hex), mask(hex) )
```

To force MDI:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0010, 0x0018 )

Phywrite ( 31, 0x0000 )
```

To force MDI-X:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0018, 0x0018 )

Phywrite ( 31, 0x0000 )
```

To resume MDI/MDI-X setting based on register 18, bits 7 and 5:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0000, 0x0018 )

Phywrite ( 31, 0x0000 )
```

3.5 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8538 device includes a robust automatic, media-dependent and crossed media-dependent detection feature, Auto MDI/MDI-X, in all of its three available speeds (10BASE-T, 100BASE-T, and 1000BASE-T). The function is fully compliant with clause 40 of the IEEE standard 802.3-2002.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both Auto MDI/MDI-X detection and Polarity Correction are enabled in the device by default. You can change the default settings using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

The VSC8538 device's automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table.

Table 3. Supported MDI Pair Combinations

RJ-45 Pin Pairings				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

Note The VSC8538 device can be configured to perform Auto MDI/MDI-X even when its Auto-negotiation feature is disabled (setting register 0.12 to 0) and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0.

3.6 Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8538 device provides an automatic link speed "downshift" option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T.

This is useful in setting up in networks using older cable installations that may include only pairs A and B and not pairs C and D.

You can configure and monitor link speed downshifting using register bits 20E.4:1. For more information, see "Extended PHY Control Set 1," page 52.

3.7 Transformer-less Ethernet

The Cat5 media interface supports 10/100/1000BT Ethernet for backplane applications such as those specified by the PICMG™ 2.16 and ATCA™ 3.0 specifications for eight-pin channels. With proper AC coupling, the typical Cat5 transformer can be removed and replaced with capacitors. For more information, see *Transformer-less Ethernet Concept and Applications*. This application note is available on the Vitesse Web site at www.vitesse.com.

3.8 Ethernet In-line Powered Devices

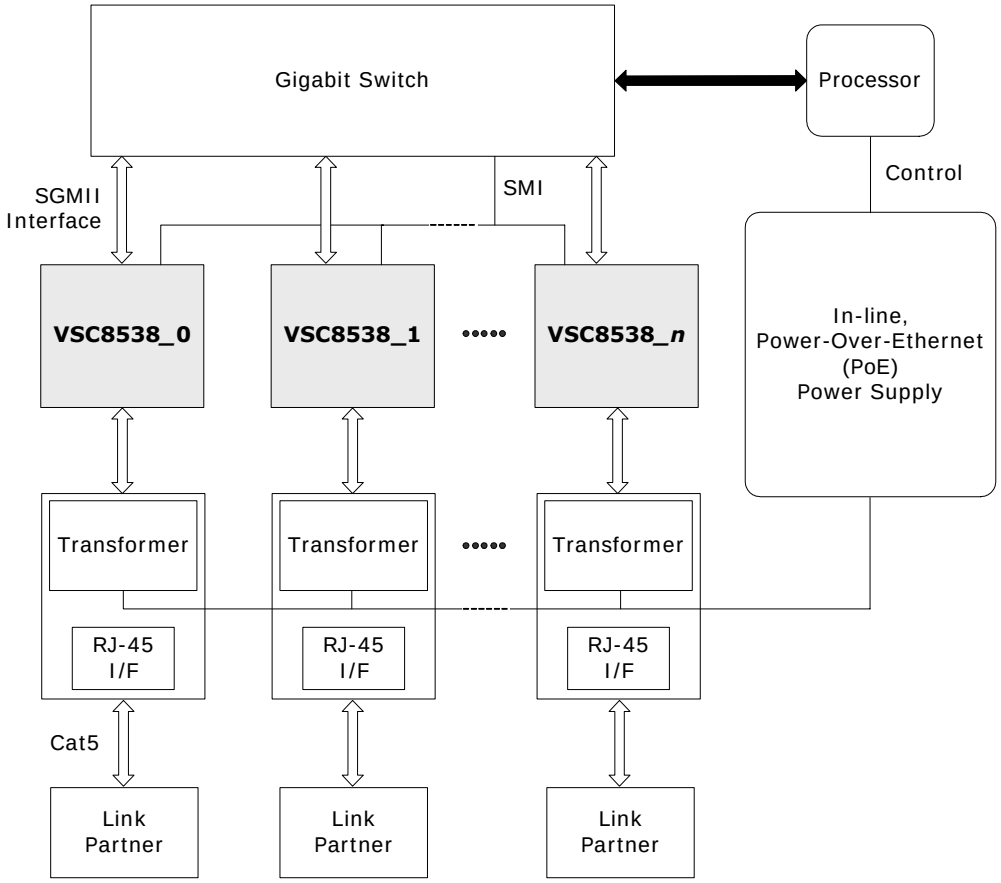
The VSC8538 device can detect legacy in-line powered devices in Ethernet network applications. Its in-line powered detection capability can be part of a system that allows for IP-phone and other devices such as wireless access points to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a Private Branch Exchange (PBX) office switch over the telephone cabling. This can eliminate the need for an IP-phone to have an external power supply. It also enables the inline

powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or some other uninterruptible power source).

For more information about legacy in-line powered device detection, visit the Cisco Web site at www.cisco.com.

The following illustration shows an example of this type of application.

Figure 6. In-line Powered Ethernet Switch Diagram



The following procedure describes the process that an Ethernet switch must perform in order to process in-line power requests made by a link partner (LP) that is, in turn, capable of receiving in-line power.

1. Enable the in-line powered device detection mode on each VSC8538 PHY using its serial management interface. Set register bit 23E.10 to 1.

2. Ensure that the VSC8538 device Auto-Negotiation Enable bit (register 0.12) is also set to 1. In the application, the device sends a special Fast Link Pulse (FLP) signal to the LP. Reading register bit 23E.9:8 will return 00 during the search for devices that require PoE.

3. The VSC8538 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE will loopback the FLP pulses when it is in a

powered-down state. This is reported when VSC8538 device register bit 23E.9:8 reads back 01. It can also be verified as an in-line power detection interrupt by reading VSC8538 device register bit 26.9, which should be a 1, and which will subsequently be cleared and the interrupt de-asserted after the read.

If an LP device does not loop back the FLP after a specific time, VSC8538 device register bit 23E.9:8 automatically resets to 10.

4. If the VSC8538 PHY reports that the LP needs PoE, the Ethernet switch must enable in-line power on this port, externally of the PHY.

5. The PHY automatically disables in-line powered device detection if the VSC8538 device register bit 23E.9:8 automatically resets to 10, and then automatically changes to its normal auto-negotiation process. A link is then auto-negotiated and established when the link status bit is set (register bit 1.2 is set to 1).

6. In the event of a link failure (indicated when VSC8538 device register bit 1.2 reads 0), the in-line power should be disabled to the in-line powered device external to the PHY. The VSC8538 PHY disables its normal auto-negotiation process and re-enables its in-line powered device detection mode.

3.9 802.3af PoE Support

The VSC8538 device is also compatible with switch designs that are intended for use in systems that supply power to Data Terminal Equipment (DTE) by means of the MDI or twisted pair cable, as described in clause 33 of the IEEE standard 802.3af.

3.10 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY™ power management mode for each PHY. This mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN™ capability. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY “wakes up” at a programmable interval and attempts to “wake-up” the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY™ power management mode in the VSC8538 device is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

There are three operating states possible when ActiPHY™ mode is enabled:

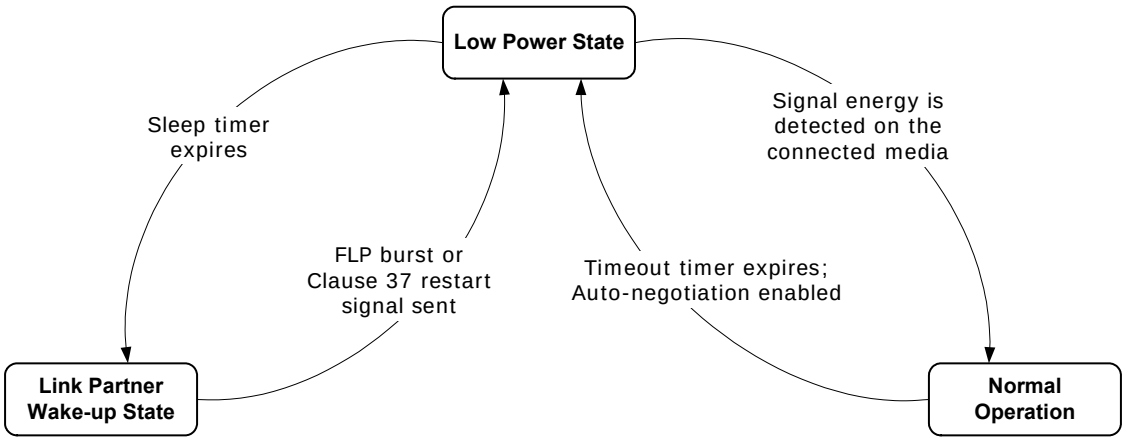
- Low power state
- LP wake-up state
- Normal operating state (link up state)

The VSC8538 device switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the link status time-out timer has expired. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described. If auto-negotiation is disabled and the link is forced to 10BT or 100BTX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 7. ActiPHY State Diagram



3.10.1 Low Power State

In the low power state, all major digital blocks are powered down. However the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT_n)
- CLKOUT

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-Negotiation capable link partner
- Another PHY in Enhanced ActiPHY LP Wake-up state

In the absence of signal energy on the media pins, the PHY transitions from the low power state to the LP wake-up state periodically based on the programmable sleep timer (register bits 20E.14:13). The actual sleep time duration is randomized from –80 milliseconds (ms) to +60 ms in order to avoid two linked PHYs in ActiPHY Mode entering a lock-up state during operation.

3.10.2 Link Partner Wake-up State

In this state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E.12:11.

In this state, the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT_*n*)
- CLKOUT

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.10.3 Normal Operating State

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

3.11 Serial Management Interface

The VSC8538 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32, 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible by means of device register 31.

For more information, see "Extended Page Registers," page 59.

The SMI is a synchronous serial interface with bidirectional data on the MDIO pin being clocked on the rising edge of the MDC pin. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending upon the total load on MDIO. An external, 2 kΩ pull-up resistor is required on the MDIO pin.

3.11.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The following illustrations show the SMI frame format for the read operation and write operation.

Figure 8. SMI Read Frame

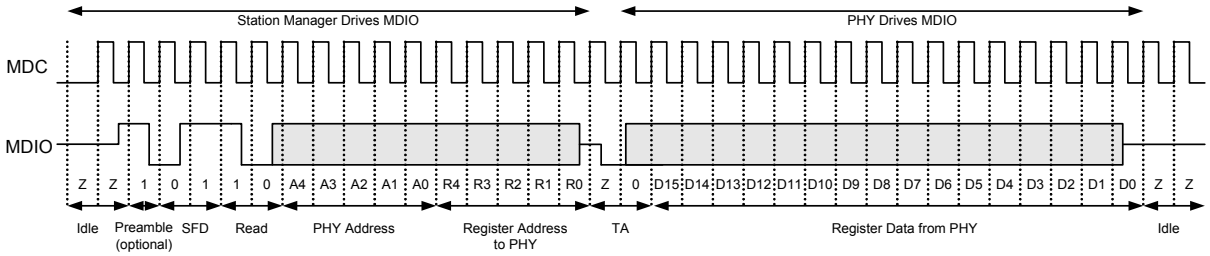
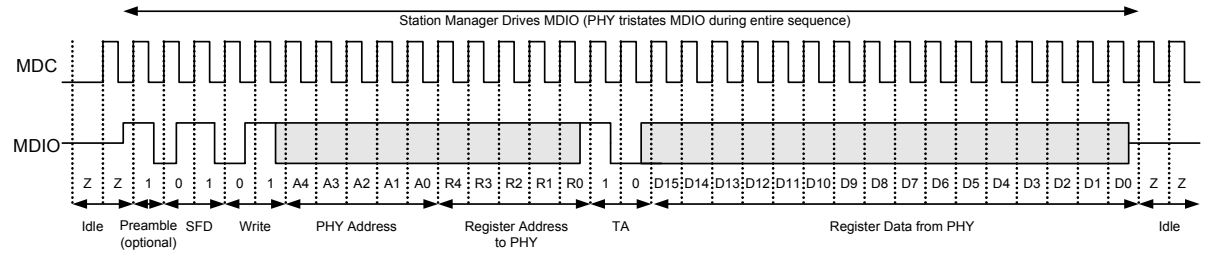


Figure 9. SMI Write Frame



The following provides additional information about the terms used in Figure 8 and Figure 9.

Idle During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.

Preamble By default, preambles are not expected or required. The preamble is a string of 1s. If it exists, the preamble must be at least one bit, but otherwise may be of an arbitrary length.

Start of Frame (SFD) A pattern of 01 indicates the start of frame. If not 01, all following bits are ignored until the next preamble pattern is detected.

Read or Write Opcode A pattern of 10 indicates a read. A 01 pattern indicates a write. If these bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.

PHY Address The particular VSC8538 responds to a message frame only when the received PHY address matches its physical address. The physical address is five bits long (4:0). Bits 4:3 are set by the CMODE pins. Bits 2:0 represent the PHY of the device being addressed.

Register Address The next five bits are the register address.

Turn-around The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turn-around (TA) bits. During read operations, the VSC8538 device drives the second TA bit, a logical 0.

Data The 16-bits read from or written to the device are considered the data or data stream. When data is being read from a PHY, it is valid at the output from one rising

edge of MDC to the next rising edge of MDC. When data is being written to the PHY, it must be valid around the rising edge of MDC.

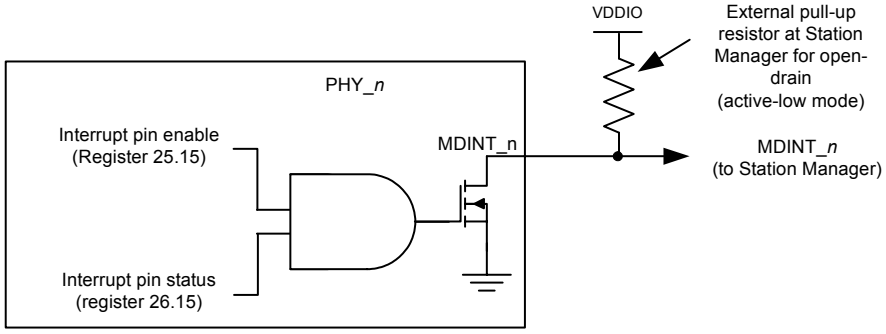
Idle The sequence is repeated.

3.11.2 SMI Interrupts

The SMI also includes an output interrupt signal, MDINT_*n*, for signaling the Station Manager when certain events occur in the PHY. A separate MDINT_*n* pin is included for each VSC8538 device PHY.

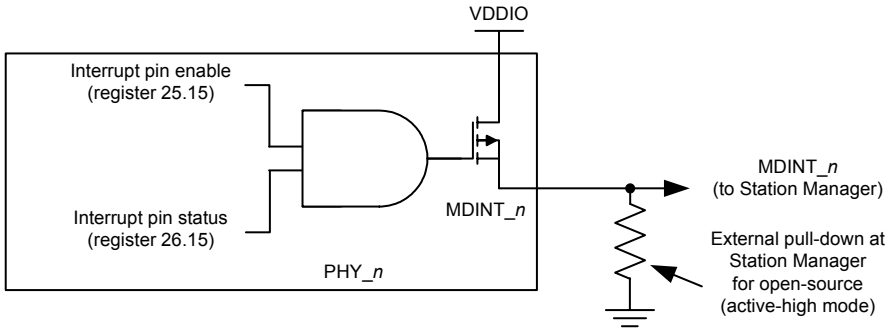
Each MDINT_*n* pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 10. MDINT_*n* Configured as an Open-Drain (Active-low) Pin



Alternatively, each MDINT_*n* pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

Figure 11. MDINT_*n* Configured as an Open-source (Active-high) Pin



If only one interrupt pin is required, each MDINT_*n* pin can be tied together to a single pull-up or pull-down resistor in a wired-OR configuration.

When a PHY generates an interrupt, the MDINT_*n* pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII Register 25.15) is set.

3.12 LED Interface

The VSC8538 device drives up to four LEDs directly for each PHY port. All LED outputs are active-low and are driven with 3.3 V from the VDD33 power supply. The pins, mainly used to sink current of the cathode side of an LED when active, can also source supply the anode portion of LEDs when not in the active state. This allows for two LED pins to be used to drive a multi-status, bi-colored LED.

3.12.1 LED Modes

Each LED pin can be configured to display different status information. Set the LED mode either by using register 29 or with the CMODE pin setting. For additional operating flexibility, LED output functions can be set on a per-port basis. The following table summarizes LED functions.

Table 4. LED Mode and Function Summary

Mode(1)	Function Name	LED State(2) and Description
0	Link/Activity(3)	1 = No link in any speed on any media interface. 0 = Valid link at any speed on any media interface. Blink or Pulse-stretch = Valid link at any speed on any media interface and with activity present.
1	Link1000/Activity	1 = No link in 1000BASE-T. 0 = Valid 1000BASE-T link. Blink or Pulse-stretch = Valid 1000BASE-T link with activity present.
2	Link100/Activity	1 = No link in 100BASE-TX. 0 = Valid 100BASE-TX link. Blink or Pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/Activity	1 = No link in 10BASE-T. 0 = Valid 10BASE-T link. Blink or Pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1 = No link in 100BASE-TX or 1000BASE-T. 0 = Valid 100BASE-TX or 1000BASE-T link. Blink or Pulse-stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1 = No link in 10BASE-T or 1000BASE-T. 0 = Valid 10BASE-T or 1000BASET-T link. Blink or Pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/Activity	1 = No link in 10BASE-T or 100BASE-TX. 0 = Valid 10BASE-T or 100BASE-TX link. Blink or Pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present.
7	Reserved	
8	Duplex/Collision	1 = Link established in half-duplex mode, or no link established. 0 = Link established in full-duplex mode. Blink or Pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1 = No collision detected. Blink or Pulse-stretch = Collision detected.
10	Activity	1 = No activity present. Blink or Pulse-stretch = Activity present (becomes TX activity present if register bit 30.14 is set to 1).

Table 4. LED Mode and Function Summary *(continued)*

Mode[1]	Function Name	LED State[2] and Description
11	Reserved	
12	Auto-Negotiation Fault	1 = No auto-negotiation fault present. 0 = Auto-Negotiation fault occurred.
13	Serial Mode	Serial Stream = See Serial LED Mode Section. Only relevant on PHY port 0 and reserved in others.
14	Force LED Off	1 = De-asserts the LED.
15	Force LED On	0 = Asserts the LED.

1. Equivalent to the setting used in register 29 to configure each LED pin.
2. For LED states: 1 = pin held high (de-asserted), 0 = pin held low (asserted), and blink/pulse-stretch dependent on LED behavior setting in register 30.
3. Link/Activity can be configured to only display copper link and disable fiber link status by setting register bits 30.15 to 1.

3.12.2 LED Behavior

Several LED behaviors can be programmed into the VSC8538 device. Use the settings in register 30 to program LED behavior, which includes the following.

LED Combine Allows for an LED to display status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED will assert when linked to a 1000BASE-T partner and will also blink or pulse-stretch when activity is transmitted either by the PHY or received by the Link Partner. The combine feature when disabled only allows status of the primary function selected. In this example, only Link1000 will assert the LED and secondary mode, activity, will not display if the combine feature is disabled.

LED Blink or Pulse-Stretch This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. For activity or collision to be visually seen, these two modes are provided. Blink is a 50% duty cycle oscillation of asserting and deasserting an LED pin. Pulse-stretch will guarantee an LED will be asserted and deasserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

Rate of LED Blink or Pulse-Stretch This controls the LED blink rate or pulse-stretch length when Blink/Pulse-Stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, this can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

LED Pulsing Enable To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

3.12.3 Serial LED Mode

Optionally, the VSC8538 device can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to Serial

LED Mode. When the mode is enabled on PHY0, the device LED[0] pin becomes the serial data pin and the LED[1] pin becomes serial clock pin. All other LED pins can still be configured normally. The Serial LED Mode clocks out the 96 LED status bits on the rising edge of the serial clock.

The LED behavior settings (in device register 30) can also be used in Serial LED Mode. The controls are used on a per-PHY basis, where the LED Combine and LED Blink or Pulse-Stretch setting of LED0_*n* for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY.

The serial bitstream outputs, 1 through 96, of each LED signal are shown in the following table beginning with PHY port 0 and ending with PHY port 7. The individual signals can be clocked out in the order shown.

Table 5. LED Serial Stream Order

PHY0	PHY1	PHY2	PHY3	PHY4	PHY5	PHY6	PHY7
Bit 1. Link/Activity	Bit 13. Link/Activity	Bit 25. Link/Activity	Bit 37. Link/Activity	Bit 49. Link/Activity	Bit 61. Link/Activity	Bit 73. Link/Activity	Bit 85. Link/Activity
Bit 2. Link1000/ Activity	Bit 14. Link1000/ Activity	Bit 26. Link1000/ Activity	Bit 38. Link1000/ Activity	Bit 50. Link1000/ Activity	Bit 62. Link1000/ Activity	Bit 74. Link1000/ Activity	Bit 86. Link1000/ Activity
Bit 3. Link100/ Activity	Bit 15. Link100/ Activity	Bit 27. Link100/ Activity	Bit 39. Link100/ Activity	Bit 51. Link100/ Activity	Bit 63. Link100/ Activity	Bit 75. Link100/ Activity	Bit 87. Link100/ Activity
Bit 4. Link10/ Activity	Bit 16. Link10/ Activity	Bit 28. Link10/ Activity	Bit 40. Link10/ Activity	Bit 52. Link10/ Activity	Bit 64. Link10/ Activity	Bit 76. Link10/ Activity	Bit 88. Link10/ Activity
Bit 5. Reserved	Bit 17. Reserved	Bit 29. Reserved	Bit 41. Reserved	Bit 53. Reserved	Bit 65. Reserved	Bit 77. Reserved	Bit 89. Reserved
Bit 6. Duplex/ Collision	Bit 18. Duplex/ Collision	Bit 30. Duplex/ Collision	Bit 42. Duplex/ Collision	Bit 54. Duplex/ Collision	Bit 66. Duplex/ Collision	Bit 78. Duplex/ Collision	Bit 90. Duplex/ Collision
Bit 7. Collision	Bit 19. Collision	Bit 31. Collision	Bit 43. Collision	Bit 55. Collision	Bit 67. Collision	Bit 79. Collision	Bit 91. Collision
Bit 8. Activity	Bit 20. Activity	Bit 32. Activity	Bit 44. Activity	Bit 56. Activity	Bit 68. Activity	Bit 80. Activity	Bit 92. Activity
Bit 9. Reserved	Bit 21. Reserved	Bit 33. Reserved	Bit 45. Reserved	Bit 57. Reserved	Bit 69. Reserved	Bit 81. Reserved	Bit 93. Reserved
Bit 10. TX Activity	Bit 22. TX Activity	Bit 34. TX Activity	Bit 46. TX Activity	Bit 58. TX Activity	Bit 70. TX Activity	Bit 82. TX Activity	Bit 94. TX Activity
Bit 11. RX Activity	Bit 23. RX Activity	Bit 35. RX Activity	Bit 47. RX Activity	Bit 59. RX Activity	Bit 71. RX Activity	Bit 83. RX Activity	Bit 95. RX Activity
Bit 12. Auto-Negotiation Fault	Bit 24. Auto-Negotiation Fault	Bit 36. Auto-Negotiation Fault	Bit 48. Auto-Negotiation Fault	Bit 60. Auto-Negotiation Fault	Bit 72. Auto-Negotiation Fault	Bit 84. Auto-Negotiation Fault	Bit 96. Auto-Negotiation Fault

3.13 GPIO Pins

The VSC8538 provides up to 16 dedicated general-purpose input/output (GPIO) pins.

All device GPIO pins and their behavior are controlled by means of registers. For more information, see "General-Purpose I/O Registers," page 66.

3.14 Testing Features

The VSC8538 device includes several testing features designed to make it easier to perform system-level debugging and in-system production testing. This section describes the available features.

3.14.1 Ethernet Packet Generator (EPG)

The device EPG can be used at each of the 10/100/1000BASE-T speed settings to isolate problems between the MAC and the VSC8538 device, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Note The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8538 device is connected to a live network.

To enable the VSC8538 device EPG feature, set the device register bit 29E.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. The PHY receive output pins to the MAC are still active when the EPG is enabled, however. If it is necessary to disable the MAC receive pins as well, set register bit 0.10 to 1.

When the device register bit 29E.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E and 30E. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If register bit 29E.13 is set to 0, register bit 29E.14 is cleared automatically after 30,000,000 packets have been transmitted.

3.14.2 CRC Counters

Two separate cyclical redundancy checking (CRC) counters are available on all PHYs in the VSC8538 device. There is a 14-bit good CRC counter available in register bits 18E.13:0 and a separate 8-bit counter available in register bits 23E.7:0.

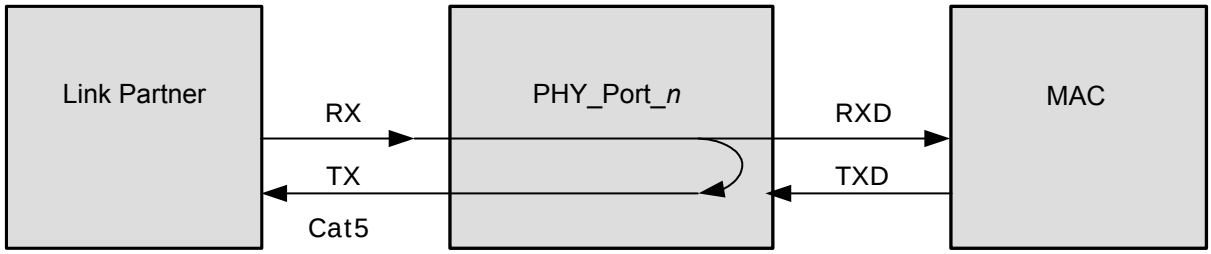
The device CRC counters operate in 10/100/1000BASE-T testing as follows:

- Upon receiving a packet on the media interface, register bit 18E.15 is set and cleared after being read. The packet then is counted by either the good CRC counter or the bad CRC counter. Both CRC counters are also automatically cleared when read.
- The good CRC counter's highest value is 10,000 packets. After it reaches this value, the counter clears and continues to count additional packets beyond that value. The bad CRC counter saturates when it reaches its maximum counter limit of 255 packets.

3.14.3 Far-end Loopback

The Far-end Loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

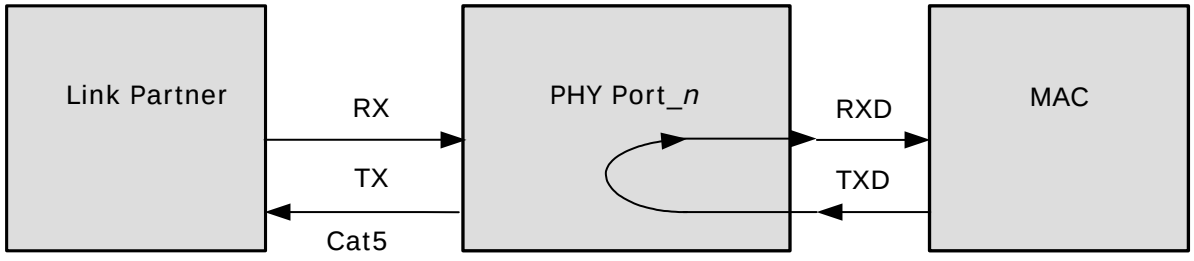
Figure 12. Far-end Loopback Diagram



3.14.4 Near-end Loopback

When the Near-end Loopback testing feature is enabled (by setting the device register bit 0.14 to 1), data on the transmit data pins (TXD) is looped back onto the device received data pins (RXD) as illustrated in the following illustration. When using this testing feature, no data is transmitted over the network.

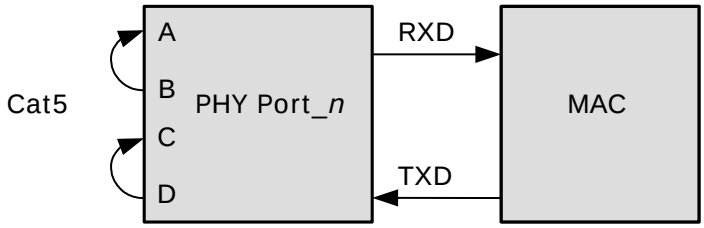
Figure 13. Near-end Loopback Diagram



3.14.5 Connector Loopback

The Connector Loopback testing feature allows for the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D as shown in the following illustration. The Connector Loopback feature functions at all available interface speeds.

Figure 14. Connector Loopback Diagram



When using the Connector Loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, only the following additional writes are required. Execute the additional writes in this, the following order:

1. Enable the 1000BASE-T Connector Loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

3.14.6 VeriPHY Cable Diagnostics

The VSC8538 device includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY® suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on the Cat5 twisted pair cabling.

Note If a link is established on the twisted pair interface in 1000BASE-T mode, VeriPHY can run without disruption of the link or disruption of any data transfer. However, if a link is established in 100BASE-TX or 10BASE-T, VeriPHY will cause the link to drop while the diagnostics are running. After the diagnostics are finished, the link will be re-established.

The following diagnostic functions are part of the VeriPHY suite:

- Detection of coupling between cable pairs
- Detection of cable pair termination
- Determination of cable length

Coupling Between Cable Pairs Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause error conditions such as anomalous coupling between cable pairs. These conditions can all prevent the device from establishing a link in any speed.

Cable Pair Termination Proper termination of Cat5 cable requires 100 Ω differential impedance between the positive and negative cable terminals. The IEEE standard 802.3 allows for a termination of as high as 115 Ω or as low as 85 Ω. If the termination falls outside of this range, it will be reported by the VeriPHY diagnostics as an anomalous termination. The diagnostics can also determine the presence of an open or shorted cable pair.

Cable Length When the Cat5 cable in an installation is properly terminated, VeriPHY reports the approximate cable length in meters.

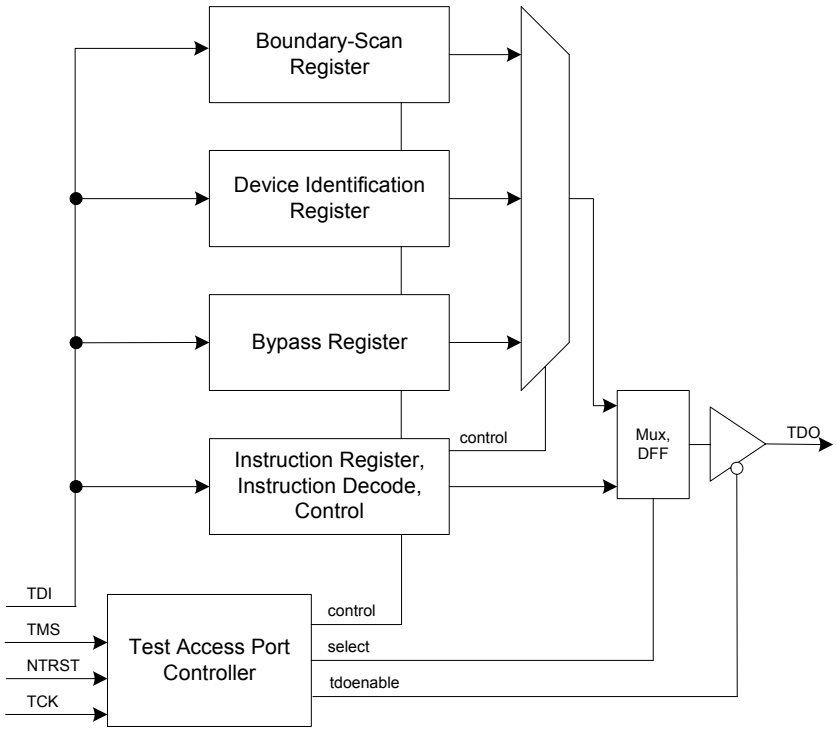
3.14.7 IEEE 1149.1 JTAG Boundary Scan

The VSC8538 device supports the Test Access Port and Boundary Scan Architecture described in the IEEE standard 1149.1. The device includes an IEEE 1149.1-compliant test interface, often referred to as a "JTAG TAP Interface."

The JTAG boundary scan logic on the VSC8538 device, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal NTRST.

The following illustration shows the TAP and Boundary Scan architecture.

Figure 15. Test Access Port and Boundary Scan Architecture Diagram



After a TAP reset, the Device Identification register is serially connected between TDI and TDO by default. The TAP Instruction register is loaded either from a shift register (when a new instruction is shifted in) or, if there is no new instruction in the shift

register, a default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

3.14.8 JTAG Instruction Codes

The VSC8538 device supports the following instruction codes:

EXTEST Allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.

SAMPLE/PRELOAD Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following table provides information about the meaning of IDCODE binary values stored in the device JTAG registers.

Table 6. JTAG Device Identification Register Description

Description	Device Version Number	Model Number	Manufacturing Identity	LSB
Bit field	31 through 28	27 through 12	11 through 1	0
Binary value	0001	1000 0101 0011 1000	001 1001 1000	1

CLAMP Allows the state of the signals driven from the component pins to be determined from the Boundary Scan register while the Bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.

HIGHZ Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

BYPASS The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

The following table provides more information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8538.

Table 7. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	IEEE 1149.1 Specification	IEEE 1149.6 Specification(1)
EXTEST	0000	Boundary-Scan	244	Mandatory	
SAMPLE/PRELOAD	0001	Boundary-Scan	244	Mandatory	
IDCODE	0110	Device Identification	32	Optional	
CLAMP	0010	Bypass Register	1	Optional	
HIGHZ	0011	Bypass Register	1	Optional	
BYPASS	1111	Bypass Register	1	Mandatory	
EXTEST_PULSE	0100	Boundary-Scan Register	244		Mandatory
EXTEST_TRAIN	0101	Boundary-Scan Register	244		Mandatory
RESERVED	0111, 1000 through 1110				

1. For more information about the specifications in IEEE standard 1149.6, visit the IEEE Web site at www.IEEE.org.

3.14.9 Boundary Scan Register Cell Order

All inputs and outputs are observed in the Boundary Scan register cells. All outputs are additionally driven by the contents of Boundary Scan register cells. Bidirectional pins have all three related Boundary Scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Vitesse Web site at www.vitesse.com.

3.15 IEEE 1149.6 AC-JTAG Boundary Scan Interface

The IEEE 1149.6 AC-JTAG solution integrated on all SerDes ports of the VSC8538 device extends the capability of IEEE 1149.1 Boundary Scan to mixed-signal pins. This interface is backward-compatible to the IEEE 1149.1 standard.

4 Configuration

The VSC8538 device can be configured using three different methods:

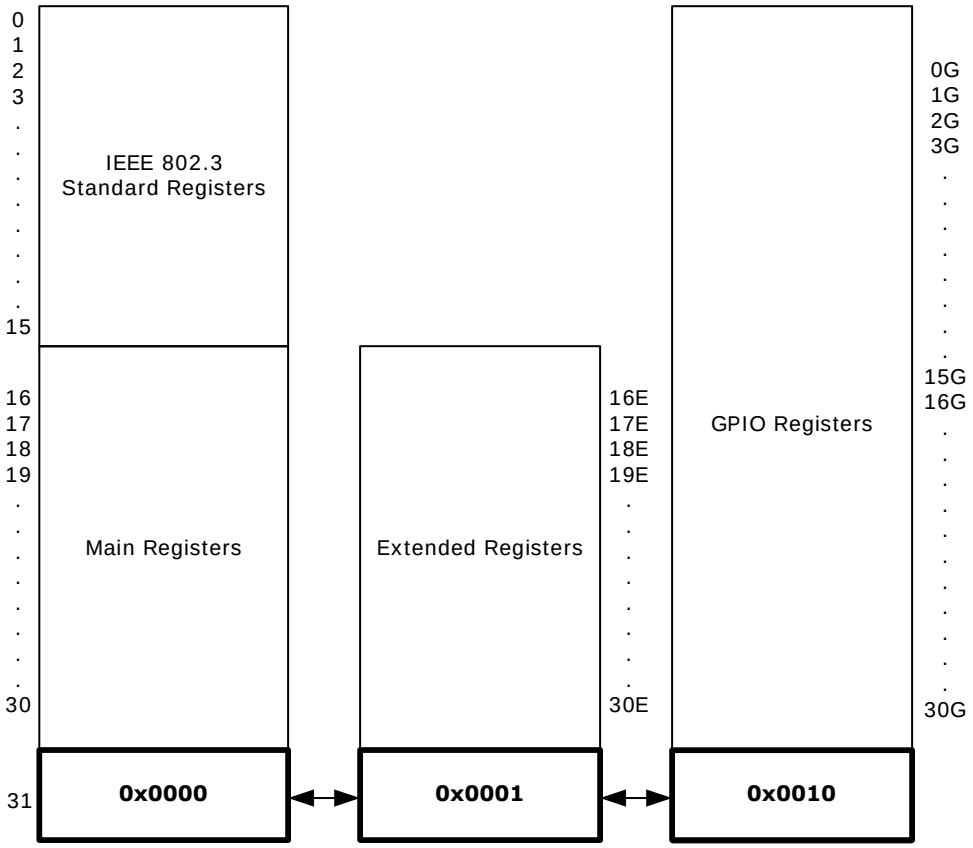
- Setting internal memory registers by means of the management interface
- Setting a combination of CMODE pins and registers
- Loading a configuration into an external EEPROM and connecting that device so that it writes configuration information upon system startup

4.1 Registers

This section provides information about how to configure the VSC8538 device using its internal memory registers and the management interface. For information about configuring the device using the CMODE pins, see “CMODE,” page 68. For information about setting up an external EEPROM to perform startup configuration, see “EEPROM,” page 71.

The VSC8538 device uses three types of registers: the IEEE standard and main device registers with addresses from 0 to 31, the extended registers with addresses from 16E through 30E, and the general-purpose input and output (GPIO) registers with addresses from 0G to 30G. The following illustration shows the relationship between the device registers and their address spaces.

Figure 16. Register Space Diagram



4.1.1 Reserved Registers

For main registers 16 through 31, extended registers 16E through 30E, and GPIO registers 0G through 30G, any bits marked as “Reserved” should be processed as read only and their states as undefined.

4.1.2 Reserved Bits

In writing to registers with reserved bits, use a “read-modify-then-write” technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.2 IEEE Standard and Main Registers

In the VSC8538 device, the standard registers' page space consists of the IEEE standard registers and the Vitesse standard registers. The following table lists the names of the registers associated with the addresses as dictated by the IEEE standard.

Table 8. IEEE 802.3 Standard Registers

Register Address	Register Name
0	Mode control
1	Mode status
2	PHY identifier 1
3	PHY identifier 2
4	Auto-Negotiation advertisement
5	Auto-Negotiation link partner ability
6	Auto-Negotiation expansion
7	Auto-Negotiation next-page transmit
8	Auto-Negotiation link partner next-page receive
9	1000BASE-T control
10	1000BASE-T status
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	1000BASE-T status extension 1

The following table lists the names of the registers in the device Main Page space. These registers are accessible only when register address 31 is set to 0x0000.

Table 9. Main Registers

Register Address	Register Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2
18	Bypass control
19	Reserved
20	Reserved
21	Reserved
22	Extended control and status
23	Extended PHY control 1
24	Extended PHY control 2
25	Interrupt mask
26	Interrupt status
27	MAC interface auto-negotiation control and status
28	Auxiliary control and status
29	LED mode select
30	LED behavior

Table 9. Main Registers *(continued)*

Register Address	Register Name
31	Extended register page access

4.2.1 Mode Control

The device register at memory address 0 controls several aspects of VSC8538 functionality. The following table shows the available bit settings in this register and what they control.

Table 10. Mode Control, Address 0 (0x00)

Bit	Name	Mode	Description	Default
15	Software reset	R/W	This is a self-clearing bit that restores all serial management interface (SMI) registers to their default state, except for sticky and super sticky bits. 1 = Reset asserted. 0 = Reset de-asserted. You must wait 4 µs after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1 = Loopback enabled. 0 = Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bit 8 of this register).	0
6, 13	Forced speed selection	R/W	MSB = bit 6, LSB = bit 13. 00 = 10 Mbps. 01 = 100 Mbps. 10 = 1000 Mbps. 11 = Reserved.	10
12	Auto-Negotiation enable	R/W	1 = Auto-Negotiation enabled. 0 = Auto-Negotiation disabled.	1
11	Power-down	R/W	1 = Power-down enabled.	0
10	Isolate	R/W	1 = Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart auto-negotiation	R/W	This is a self-clearing bit. 1 = Restart auto-negotiation on media interface.	0
8	duplex	R/W	1 = Full-duplex. 0 = Half-duplex.	0
7	Collision test enable	R/W	1 = Collision test enabled.	0
6	MSB for speed selection	R/W	See bit 13 above.	1
5:0	Reserved			000000

4.2.2 Mode Status

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

Table 11. Mode Status, Address 1 (0x01)

Bit	Name	Mode	Description	Default
15	100BASE-T4 capability	RO	1 = 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1 = 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1 = 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1 = 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1 = 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1 = 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1 = 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1 = Extended status information present in register 15.	1
7	Reserved	RO		0
6	Preamble suppression capability	RO	1 = MF preamble may be suppressed. 0 = MF always required.	1
5	Auto-Negotiation complete	RO	1 = Auto-Negotiation complete.	0
4	Remote fault	RO	This bit latches high. 1 = Far-end fault detected.	0
3	Auto-Negotiation capability	RO	1 = Auto-Negotiation capable.	1
2	Link status	RO	This bit latches low. 1 = Link is up.	0
1	Jabber detect	RO	This bit latches high. 1 = Jabber condition detected.	0
0	Extended capability	RO	1 = Extended register capable.	1

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8538 device are used to provide information associated with aspects of the device identification. The following tables list the readouts you can expect.

Table 12. Identifier 1, Address 2 (0x02)

Bit	Name	Mode	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0x0007

Table 13. Identifier 2, Address 3 (0x03)

Bit	Name	Mode	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	0x0001
9:4	Vitesse model number	RO	VSC8538	101000
3:0	Device revision number	RO		0001

4.2.4 Auto-Negotiation Advertisement

The bits in address 4 in the main registers space control the VSC8538 device ability to notify other devices of the status of its auto-negotiation feature. The following table shows the available settings and readouts.

Table 14. Device Auto-Negotiation Advertisement, Address 4 (0x04)

Bit	Name	Mode	Description	Default
15	Next page transmission request	R/W	1 = Request enabled	0
14	Reserved	RO		0
13	Transmit remote fault	R/W	1 = Enabled	0
12	Reserved technologies	R/W		0
11	Advertise asymmetric pause	R/W	1 = Advertises asymmetric pause	CMODE
10	Advertise symmetric pause	R/W	1 = Advertises symmetric pause	CMODE
9	Advertise 100BASE-T4	R/W	1 = Advertises 100BASE-T4	0
8	Advertise 100BASE-TX FDX	R/W	1 = Advertise 100BASE-TX FDX	CMODE
7	Advertise 100BASE-TX HDX	R/W	1 = Advertises 100BASE-TX HDX	CMODE
6	Advertise 10BASE-T FDX	R/W	1 = Advertises 10BASE-T FDX	CMODE
5	Advertise 10BASE-T HDX	R/W	1 = Advertises 10BASE-T HDX	CMODE
4:0	Advertise selector	R/W		00001

4.2.5 Link Partner Auto-Negotiation Capability

The bits in main register 5 enable you to determine if the Cat5 link partner (LP) used with the VSC8538 device is compatible with the auto-negotiation functionality.

Table 15. Auto-Negotiation Link Partner Ability, Address 5 (0x05)

Bit	Name	Mode	Description	Default
15	LP next page transmission request	RO	1 = Requested	0
14	LP acknowledge	RO	1 = Acknowledge	0
13	LP remote fault	RO	1 = Remote fault	0
12	Reserved	RO		0
11	LP advertise asymmetric pause	RO	1 = Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1 = Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1 = Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1 = Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1 = Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1 = Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1 = Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

4.2.6 Auto-Negotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP auto-negotiation functioning. The following table shows the available settings and readouts.

Table 16. Auto-Negotiation Expansion, Address 6 (0x06)

Bit	Name	Mode	Description	Default
15:5	Reserved	RO		00000000000
4	Parallel detection fault	RO	This bit latches high. 1 = Parallel detection fault.	0
3	LP next page capable	RO	1 = LP is next page capable.	0
2	Local PHY next page capable	RO	1 = Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1 = New page has been received.	0

Table 16. Auto-Negotiation Expansion, Address 6 (0x06) *(continued)*

Bit	Name	Mode	Description	Default
0	LP is auto-negotiation capable	RO	1 = LP is capable of auto-negotiation.	0

4.2.7 Transmit Auto-Negotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an auto-negotiation sequence. The following table shows the settings available.

Table 17. Auto-Negotiation Next Page Transmit, Address 7 (0x07)

Bit	Name	Mode	Description	Default
15	Next page	R/W	1 = More pages follow	0
14	Reserved	RO		0
13	Message page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Complies with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	Message/ unformatted code	R/W		00000000001

4.2.8 Auto-Negotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP auto-negotiation. The following table shows the possible readouts.

Table 18. Auto-Negotiation LP Next Page Receive, Address 8 (0x08)

Bit	Name	Mode	Description	Default
15	LP next page	RO	1 = More pages follow	0
14	Acknowledge	RO	1 = LP acknowledge	0
13	LP message page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge 2	RO	1 = LP complies with request	0
11	LP toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	LP message/ unformatted code	RO		00000000000

4.2.9 1000BASE-T Control

The VSC8538 device's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 19. 1000BASE-T Control, Address 9 (0x09)

Bit	Name	Mode	Description	Default
15:13	Transmitter test mode	R/W	000 = Normal. 001 = Mode 1: Transmit waveform test. 010 = Mode 2: Transmit jitter test as master. 011 = Mode 3: Transmit jitter test as slave. 100 = Mode 4: Transmitter distortion test. 101 to 111 = Reserved: Operation not defined.	000
12	Master/slave manual configuration	R/W	1 = Master/slave manual configuration enabled.	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1 = Configure PHY as master during negotiation. 0 = Configure PHY as slave during negotiation.	0
10	Port type	R/W	1 = Multi-port device. 0 = Single-port device.	1
9	1000BASE-T FDX capability	R/W	1 = PHY is 1000BASE-T FDX capable.	CMODE
8	1000BASE-T HDX capability	R/W	1 = PHY is 1000BASE-T HDX capable.	CMODE
7:0	Reserved	R/W		0x00

Note Transmitter Test Mode (bits 15:13) operates in the manner described in IEEE standard 802.3, section 40.6.1.1.2. If using any of the Transmitter Test Modes, the Auto-Media Sense functionality must be disabled. For more information, see "Extended PHY Control Set 1," page 52.

4.2.10 1000BASE-T Status

The bits in register 10 of the main register space allow you to read the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 20. 1000BASE-T Status, Address 10 (0x0A)

Bit	Name	Mode	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0
14	Master/slave configuration resolution	RO	1 = Local PHY configuration resolved to master. 0 = Local PHY configuration resolved to slave.	1
13	Local receiver status	RO	1 = Local receiver okay.	0

Table 20. 1000BASE-T Status, Address 10 (0x0A) *(continued)*

Bit	Name	Mode	Description	Default
12	Remote receiver status	RO	1 = Remote receiver OK.	0
11	LP 1000BASE-T FDX capability	RO	1 = LP 1000BASE-T FDX capable.	0
10	LP 1000BASE-T HDX capability	RO	1 = LP 1000BASE-T HDX capable.	0
9:8	Reserved	RO		00
7:0	Idle error count	RO	This is a self-clearing bit.	0x00

4.2.11 Main Registers Reserved Addresses

In the VSC8538 device main registers page space, registers 11 through 15 (0x0B through 0x0E) are reserved.

4.2.12 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 21. 1000BASE-T Status Extension 1, Address 15 (0x0F)

Bit	Name	Mode	Description	Default
15	1000BASE-X FDX capability	RO	1 = PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1 = PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1 = PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1 = PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO		0x000

4.2.13 100BASE-TX Status Extension

Register 16 in the main registers page space of the VSC8538 device provides additional information about the status of the device's 100BASE-TX operation.

Table 22. 100BASE-TX Status Extension, Address 16 (0x10)

Bit	Name	Mode	Description	Default
15	100BASE-TX Descrambler	RO	1 = Descrambler locked.	0
14	100BASE-TX lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0

Table 22. 100BASE-TX Status Extension, Address 16 (0x10) *(continued)*

Bit	Name	Mode	Description	Default
13	100BASE-TX disconnect state	RO	This is a self-clearing bit. 1 = PHY 100BASE-TX link disconnect detected.	0
12	100BASE-TX current link status	RO	1 = PHY 100BASE-TX link active.	0
11	100BASE-TX receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	100BASE-TX transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0
9	100BASE-TX SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	100BASE-TX ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7:0	Reserved	RO		

4.2.14 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 22, page 48. The following table shows the settings available.

Table 23. 1000BASE-T Status Extension 2, Address 17 (0x11)

Bit	Name	Mode	Description	Default
15	1000BASE-T descrambler	RO	1 = Descrambler locked.	0
14	1000BASE-T lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0
13	1000BASE-T disconnect state	RO	This is a self-clearing bit. 1 = PHY 1000BASE-T link disconnect detected.	0
12	1000BASE-T current link status	RO	1 = PHY 1000BASE-T link active.	0
11	1000BASE-T receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	1000BASE-T transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0
9	1000BASE-T SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	1000BASE-T ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7	1000BASE-T carrier extension error	RO	This is a self-clearing bit. 1 = Carrier extension error detected.	0
6:0	Reserved	RO		

4.2.15 Bypass Control

The bits in the Bypass Control register in the VSC8538 device control aspects of functionality in effect when the device is disabled so that traffic can bypass it in your design. The following table shows the settings available.

Table 24. Bypass Control, Address 18 (0x12)

Bit	Name	Mode	Description	Default
15	Transmit disable	R/W	1 = PHY transmitter disabled.	0
14:9	Reserved	RO		
8	1000BASE-T transmitter test clock	R/W	1 = Enabled.	0
7	Auto MDI-X at forced 10/100	R/W	This is a sticky bit. 1 = Disable Auto MDI-X at forced 10/100 speeds.	1
6	Reserved	RO		
5	Disable pair swap correction	R/W	This is a sticky bit. 1 = Disable the automatic pair swap correction.	0
4	Disable polarity correction	R/W	This is a sticky bit. 1 = Disable polarity inversion correction on each subchannel.	0
3	Parallel detect control	R/W	This is a sticky bit. 1 = Do not ignore advertised ability. 0 = Ignore advertised ability.	1
2	Reserved	RO		
1	Disable automatic 1000BASE-T next page exchange	R/W	This is a sticky bit. 1 = Disable automatic 1000BASE-T next page exchanges.	0
0	CLKOUT output enable	R/W	This is a sticky bit. 1 = Enable clock output pin.	CMODE

Note If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

4.2.16 Reserved Address Space

The bits in register 19, register 20, and register 21 (0x12, 0x14, and 0x15, respectively) are reserved.

4.2.17 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 25. Extended Control and Status, Address 22 (0x16)

Bit	Name	Mode	Description	Default
15	Force 10BASE-T link high	R/W	This is a sticky bit. 1 = Bypass link integrity test. 0 = Enable link integrity test.	0
14	Jabber detect disable	R/W	This is a sticky bit. 1 = Disable jabber detect.	0
13	Disable 10BASE-T echo	R/W	This is a sticky bit. 1 = Disable 10BASE-T echo.	1
12	Reserved	RO		
11:10	10BASE-T squelch control	R/W	This is a sticky bit. 00 = Normal squelch. 01 = Low squelch. 10 = High squelch. 11 = Reserved.	00
9	Sticky reset enable	R/W	This is a super-sticky bit. 1 = Enabled.	1
8	EOF Error	RO	This bit is self-clearing. 1 = EOF error detected.	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1 = 10BASE-T link disconnect detected.	0
6	10BASE-T link status	RO	1 = 10BASE-T link active.	0
5:1	Reserved	RO		
0	SMI broadcast write	R/W	This is a sticky bit. 1 = Enabled.	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:0 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which may improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and may improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0 through 31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY_0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

4.2.18 Extended PHY Control Set 1

The bits in the extended control set control the MAC auto-negotiation functioning, SGMII alignment errors, and EEPROM status. The following table shows the settings available.

Table 26. Extended PHY Control 1, Address 23 (0x17)

Bit	Name	Mode	Description	Default
15:14	Reserved	RO		
13	MAC interface auto-negotiation	R/W	This is a super-sticky bit. 1 = Enabled.	CMODE
12	MAC interface mode	R/W	This is a super-sticky bit. 1 = 1000BASE-X. 0 = SGMII.	0
11:4	Reserved	RO		
3	Far-end loopback mode	R/W	1 = Enabled.	0
2	Reserved	RO		
1	SGMII alignment error status	RO	This is a self-clearing bit. 1 = Alignment error detected since last read.	0
0	EEPROM status	RO	1 = EEPROM present on EECLK and EEDAT pins.	0

Note After configuring bits 13:8 of the extended PHY control register set 1, a software reset (Register 0, bit 15) must be written to change the device operating mode.

4.2.19 Extended PHY Control Set 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 27. Extended PHY Control 2, Address 24 (0x18)

Bit	Name	Mode	Description	Default
15:13	100BASE-TX edge rate control	R/W	This is a sticky bit. 011 = +5 Edge rate (slowest). 010 = +4 Edge rate. 001 = +3 Edge rate. 000 = +2 Edge rate. 111 = +1 Edge rate. 110 = Default edge rate. 101 = –1 Edge rate. 100 = –2 Edge rate (fastest).	110
12	PICMG 2.16 reduced power mode	R/W	This is a sticky bit. 1 = Enabled.	0
11:9	Reserved	RO		
8:7	SGMII input preamble	R/W	This is a sticky bit. 00 = No SGMII preamble required. 01 = 1-Byte SGMII preamble required. 10 = 2-Byte SGMII preamble required. 11 = Reserved.	00

Table 27. Extended PHY Control 2, Address 24 (0x18) *(continued)*

Bit	Name	Mode	Description	Default
6	SGMII output preamble	R/W	This is a sticky bit. 0 = No SGMII preamble. 1 = Two-byte SGMII preamble.	0
5:4	Jumbo packet mode	R/W	This is a sticky bit. 00 = Normal IEEE 1.5 KB packet length. 01 = 9-KB Jumbo packet length (12 KB with 60 ppm or better reference clock). 10 = 12-KB Jumbo packet length (16 KB with 70 ppm or better reference clock). 11 = Reserved.	00
3:1	100BASE-TX transmitter amplitude control	R/W	011 = +3 Amplitude setting (largest). 010 = +2 Amplitude setting. 001 = +1 Amplitude setting. 000 = Default amplitude. 111 = –1 Amplitude setting. 110 = –2 Amplitude setting. 101 = –3 Amplitude setting. 100 = –4 Amplitude setting (smallest).	000
0	1000BASE-T connector loopback	R/W	1 = Enabled.	0

Note When bits 5:4 are set to Jumbo Packet Mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher Jumbo packet length.

4.2.20 Interrupt Mask

The bits in register 25 control the device interrupt mask. The following table shows the settings available.

Table 28. Interrupt Mask, Address 25 (0x19)

Bit	Name	Mode	Description	Default
15	MDINT interrupt status enable	R/W	This is a sticky bit. 1 = Enabled.	0
14	Speed state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
13	Link state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
12	FDX state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
11	Auto-Negotiation error mask	R/W	1 = Enabled.	0
10	Auto-Negotiation complete mask	R/W	This is a sticky bit. 1 = Enabled.	0
9	In-line powered device (PoE) detect mask	R/W	This is a sticky bit. 1 = Enabled.	0
8:3	Reserved	RO		
2	Link speed downshift detect mask	R/W	This is a sticky bit. 1 = Enabled.	0

Table 28. Interrupt Mask, Address 25 (0x19) *(continued)*

Bit	Name	Mode	Description	Default
1	Master/Slave resolution error mask	R/W	This is a sticky bit. 1 = Enabled.	0
0	Reserved	RO		

Note When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted.

4.2.21 Interrupt Status

The status of interrupts already written to the device are available for reading from register 26 in the main registers space. The following table shows the readouts you can expect.

Table 29. Interrupt Status, Address 26 (0x1A)

Bit	Name	Mode	Description	Default
15	Interrupt status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
14	Speed state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
13	Link state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
12	FDX state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
11	Auto-Negotiation error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	
10	Auto-Negotiation complete status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
9	In-line powered device detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
8:3	Reserved	RO		
2	Link speed downshift detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
1	Master/Slave resolution error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
0	Reserved	RO		

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.

4.2.22 MAC Interface Auto-Negotiation Control and Status

Device auto-negotiation for the MAC interface is controlled in register 27. The same register is used to check the status of those parameters. The following table shows the settings available.

Table 30. MAC Auto-Negotiation Control and Status, Address 27 (0x1B)

Bit	Name	Mode	Description	Default
15	MAC or media interlock	R/W	This is a sticky bit. 1 = MAC interface disabled when media link down. 0 = MAC interface not suppressed by media link status.	0
14	MAC or media restart auto-negotiation interlock	R/W	This is a sticky bit. 1 = MAC interface restarts its auto-negotiation if the media link changes. 0 = MAC interface does not automatically change if media link changes.	0
13	MAC interface auto-negotiation auto-sense	R/W	This is a sticky bit. 1 = If MAC auto-negotiation is enabled, this allows the MAC interface to be able to link to MACs with auto-negotiation enabled and disabled. 0 = Normal MAC auto-negotiation behavior.	0
12	MAC interface auto-negotiation restart	R/W	This is a self-clearing bit. 1 = Restart auto-negotiation.	0
11:10	Reserved	RO		
9:8	Remote fault detected from MAC	RO	Corresponds to the remote fault bits sent by the MAC during auto-negotiation.	00
7	Asymmetric pause advertised by the MAC	RO	Corresponds to the asymmetric pause bit sent by the MAC during auto-negotiation.	0
6	Symmetric pause advertised by the MAC	RO	Corresponds to the symmetric pause bit sent by the MAC during auto-negotiation.	0
5	Full-duplex advertised by the MAC	RO	Corresponds to the full-duplex bit sent by the MAC during auto-negotiation.	0
4	Half-duplex advertised by the MAC	RO	Corresponds to the half-duplex bit sent by the MAC during auto-negotiation.	0
3	MAC auto-negotiation capable	RO	1 = MAC is auto-negotiation capable.	0
2	MAC interface link status	RO	1 = The MAC interface is actively linked.	0
1	MAC interface auto-negotiation complete	RO	1 = The MAC interface auto-negotiation is complete.	0
0	Reserved	RO		

4.2.23 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the readouts you can expect.

Table 31. Auxiliary Control and Status, Address 28 (0x1C)

Bit	Name	Mode	Description	Default
15	Auto-Negotiation complete	RO	Duplicate of bit 1.5.	0
14	Auto-Negotiation disabled	RO	Inverted duplicate of bit 0.12.	0
13	MDI/MDI-X crossover indication	RO	1 = MDI/MDI-X crossover performed internally.	0
12	CD pair swap	RO	1 = CD pairs are swapped.	0
11	A polarity inversion	RO	1 = Polarity swap on pair A.	0
10	B polarity inversion	RO	1 = Polarity swap on pair B.	0
9	C polarity inversion	RO	1 = Polarity swap on pair C.	0
8	D polarity inversion	RO	1 = Polarity swap on pair D.	0
7	ActiPHY link status time-out control [1]	R/W	This is a sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00 = 1 second. 01 = 2 seconds. 10 = 3 seconds. 11 = 4 seconds.	CMODE
6	ActiPHY mode enable	R/W	This is a sticky bit. 1 = Enabled.	0
5	FDX status	RO	1 = Full-duplex. 0 = Half-duplex.	00
4:3	Speed status	RO	00 = Speed is 10BASE-T. 01 = Speed is 100BASE-TX. 10 = Speed is 1000BASE-T. 11 = Reserved.	0
2	ActiPHY link status time-out control [0]	R/W	This is a sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00 = 1 second. 01 = 2 seconds. 10 = 3 seconds. 11 = 4 seconds.	0
1:0	Reserved	RO		

4.2.24 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information you need to access the functionality of

each of the outputs. For information about the LED modes referenced in the table, see Table 33, page 57.

Table 32. LED Mode Select, Address 29 (0x1D)

Bit	Name	Mode	Description	Default
15:12	LED3 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
11:8	LED2 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
7:4	LED1 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
3:0	LED0 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE

The following table shows the LED functional modes that can be programmed into any of the device's LED outputs. For more information about accessing or reading the status of the outputs, see Table 32, page 57.

Table 33. Available LED Mode Settings

Bit Setting	LED Indicates
0000	Link/activity, Mode 0
0001	Link1000/activity, Mode 1
0010	Link100/activity, Mode 2
0011	Link10/activity, Mode 3
0100	Link100/1000/activity, Mode 4
0101	Link10/1000/activity, Mode 5
0110	Link10/100/activity, Mode 6
0111	Reserved, Mode 7
1000	Duplex/collision, Mode 8
1001	Collision, Mode 9
1010	Activity, Mode 10
1011	Reserved, Mode 11
1100	Autoneg_Fault, Mode 12
1101	Serial mode (on LED0 and LED1 on PHY0 only), Mode 13
1110	Force LED off, Mode 14
1111	Force LED on, Mode 15

4.2.25 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 34. LED Behavior, Address 30 (0x1E)

Bit	Name	Mode	Description	Default
15:13	Reserved	RO		

Table 34. LED Behavior, Address 30 (0x1E) *(continued)*

Bit	Name	Mode	Description	Default
12	LED pulsing enable	R/W	This is a sticky bit. 0 = Normal operation. 1 = LEDs pulse with a 5-kHz, 20% duty cycle when active.	0
11:10	LED blink/ pulse-stretch rate	R/W	This is a sticky bit. 00 = 2.5-Hz blink rate / 400 ms pulse-stretch. 01 = 5-Hz blink rate / 200 ms pulse-stretch. 10 = 10-Hz blink rate / 100 ms pulse-stretch. 11 = 20-Hz blink rate / 50 ms pulse-stretch.	CMODE
9	Reserved	RO		
8	LED3 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
7	LED2 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
6	LED1 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
5	LED0 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
4	Reserved	RO		
3	LED3 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/ activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE
2	LED2 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/ activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE
1	LED1 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/ activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE
0	LED0 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/ activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE

Note Bits 29.11:10 are controlled only by port 0 and affect the behavior of all ports.

4.3 Extended Page Registers

To provide functionality beyond the IEEE802.3-specified 32 registers and main device registers, the VSC8538 device includes an extended set of registers that provide an additional 15 register spaces.

To access the extended page registers (16E through 30E), enable extended register access by writing 0x0001 to register 31. For more information, see Table 36, page 60.

When extended page register access is enabled, reads and writes to registers 16 through 30 affect the extended registers 16E through 30E instead of those same registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page space. These registers are accessible only when the device register 31 is set to 0x0001.

Table 35. Extended Registers Page Space

Register Address	Register Name
16E	Reserved
17E	SerDes MAC control
18E	CRC good counter
19E	Reserved
20E	Extended PHY control 3
21E	EEPROM interface status and control
22E	EEPROM data read or write
23E	Extended PHY control 4
24E	VeriPHY 1
25E	VeriPHY 2
26E	VeriPHY 3
27E	Reserved
28E	Reserved
29E	Ethernet packet generator (EPG) 1
30E	EPG 2

4.3.1 Extended Page Access

The register at address 31 controls the access to both the extended and GPIO registers for the VSC8538 device. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 36. Extended Page Access, Address 31 (0x1F)

Bit	Name	Mode	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000 = Register 16 through 30 accesses main register space 0x0001 = Register 16 through 30 accesses extended register space 0x0010 = Register 0 through 30 accesses GPIO register space	0x0000

4.3.2 Reserved Address Space

The bits of the extended register 16E (0x010) are reserved.

4.3.3 SerDes MAC Control

Register 17E, which is accessible only when extended register access has been enabled, controls the output swing of the VSC8538 device SerDes MAC. The following table shows the settings available.

Table 37. SerDes MAC Control, Address 17E (0x11)

Bit	Name	Mode	Description	Default
15:5	Reserved	RO		
4:2	SerDes MAC output swing control	R/W	This is a sticky bit. 000 = 400 mV (peak-to-peak). 001 = 600 mV (peak-to-peak). 010 = 800 mV (peak-to-peak). 011 = 1000 mV (peak-to-peak). 100 = 1200 mV (peak-to-peak). 101 = 1400 mV (peak-to-peak). 110 and 111 = Reserved.	100
1:0	Reserved	RO		

4.3.4 CRC Good Counter

Register 18E makes it possible to read the contents of the CRC good counter; the number of CRC routines that have executed successfully. The following table shows the readouts you can expect.

Table 38. CRC Good Counter, Address 18E (0x12)

Bit	Name	Mode	Description	Default
15	Packet since last read	RO	This is a self-clearing bit. 1 = Packet received since last read.	0

Table 38. CRC Good Counter, Address 18E (0x12) *(continued)*

Bit	Name	Mode	Description	Default
14	Reserved	RO		
13:0	CRC good counter contents	RO	This is a self-clearing bit. Counter containing the number of packets with valid CRCs; this counter does not saturate and will roll over.	0x000

4.3.5 Reserved Address Space

The bits of the extended register 19E (0x013) are reserved.

4.3.6 Extended PHY Control

Register 20E controls the device ActiPHY sleep timer, its wake-up timer, the frequency of the CLKOUT signal, and its link speed downshifting feature. The following table shows the settings available.

Table 39. ActiPHY Control, Address 20E (0x14)

Bit	Name	Mode	Description	Default
15	Disable carrier extension	R/W	1 = Disable.	0
14:13	ActiPHY sleep timer	R/W	This is a sticky bit. 00 = 1 second. 01 = 2 seconds. 10 = 3 seconds. 11 = 4 seconds.	01
12:11	ActiPHY wake-up timer (1)	R/W	This is a sticky bit. 00 = 160 ms. 01 = 400 ms. 10 = 800 ms. 11 = 2 seconds.	00
10:9	Reserved	RO		
8	CLKOUT Frequency (2)	R/W	This is a sticky bit. 1 = 156.25 MHz. 0 = 125 MHz.	CMODE
7:6	Reserved	RO		
5	Reserved	RO		
4	Enable link speed auto-downshift feature	R/W	This is a sticky bit. 1 = Enable auto link speed downshift from 1000BASE-T.	CMODE
3:2	Link speed auto-downshift control	R/W	This is a sticky bit. 00 = Downshift after 2 failed 1000BASE-T auto-negotiation attempts. 01 = Downshift after 3 failed 1000BASE-T auto-negotiation attempts. 10 = Downshift after 4 failed 1000BASE-T auto-negotiation attempts. 11 = Downshift after 5 failed 1000BASE-T auto-negotiation attempts.	01

Table 39. ActiPHY Control, Address 20E (0x14) *(continued)*

Bit	Name	Mode	Description	Default
1	Link speed auto-downshift status	RO	0 = No downshift. 1 = Downshift is required or has occurred.	0
0	Reserved	RO		

1. There is a design consideration related to this feature. For more information, see "ActiPHY Wake Timer Needs to be Set to '11'," page 99.
2. Bit 8 is valid only on PHY_0.

4.3.7 EEPROM Interface Status and Control

Register 21E is used to affect control over device function when you have incorporated a startup EEPROM into your design.

Table 40. EEPROM Interface Status and Control, Address 21E (0x15)

Bit	Name	Mode	Description	Default
15	Reserved	RO		
14	Re-read EEPROM after software reset	R/W	This is a super-sticky bit. 1 = Contents of EEPROM to be re-read after software reset.	0
13	Enable EEPROM access	R/W	This is a self-clearing bit. 1 = Execute read or write EEPROM based on the settings of register bit 21E.12.	0
12	EEPROM read or write	R/W	1 = Read from EEPROM. 0 = Write to EEPROM.	1
11	EEPROM ready	RO	1 = EEPROM is ready for read or write.	1
10:0	EEPROM address	R/W	Sets the address of the EEPROM to which the read or write is to be directed.	00000000000

4.3.8 EEPROM Data Read/Write

Register 22E in the extended register space enables access to the contents of the external EEPROM in your design. The following table shows the writes needed to obtain the data from the external device.

Table 41. EEPROM Read or Write, Address 22E (0x16)

Bit	Name	Mode	Description	Default
15:8	EEPROM read data	RO	Eight-bit data read from EEPROM; requires setting register 21E, bit 13.	0x00
7:0	EEPROM write data	R/W	Eight-bit data to be written to EEPROM.	0x00

4.3.9 PoE and Miscellaneous Functionality

The register at address 23E consists of the fourth set bits that control various aspects of inline powering and the CRC error counter in the VSC8538.

Table 42. Extended PHY Control 4, Address 23E (0x17)

Bit	Name	Mode	Description	Default
15:11	PHY address	RO	PHY address; latched on reset.	CMODE
10	In-Line powered device detection	R/W	This is a sticky bit. 1 = Enabled.	0
9:8	In-line powered device detection status	RO	00 = Searching for devices. 01 = Device found; requires inline power. 10 = Device found; does not require inline power. 11 = Reserved.	00
7:0	CRC error counter	RO	This is a self-clearing bit. CRC error counter for the Ethernet packet generator. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

Note Bits 9:8 are only valid if bit 10 is set.

4.3.10 VeriPHY Control 1

Register 24E in the extended register space provides control over the device VeriPHY diagnostics features. There are three separate VeriPHY control registers. The following table shows the settings available and describes the readouts you can expect.

Table 43. VeriPHY Control Register 1, Address 24E (0x18)

Bit	Name	Mode	Description	Default
15	VeriPHY trigger	R/W	This is a self-clearing bit. 1 = Triggers the VeriPHY algorithm; clears when VeriPHY has completed; settings in registers 24E through 26E become valid after this bit clears.	0
14	VeriPHY valid	RO	1 = VeriPHY results in registers 24E through 26E are valid.	0
13:8	Pair A (1-2) distance	RO	Loop length or distance to anomaly for pair A (1-2).	0x00
7:6	Reserved	RO		
5:0	Pair B (3-6) distance	RO	Loop length or distance to anomaly for pair B (3-6).	0x00

Note The resolution of the 6-bit length field is 3 meters.

4.3.11 VeriPHY Control 2

The register at address 25E consists of the second of the three device registers that provide control over VeriPHY diagnostics features. The following table shows the readouts you can expect.

Table 44. VeriPHY Control Register 2, Address 25E (0x19)

Bit	Name	Mode	Description	Default
15:14	Reserved	RO		
13:8	Pair C (4-5) distance	RO	Loop length or distance to anomaly for pair C (4 and 5)	0x00
7:6	Reserved	RO		
5:0	Pair D (7-8) distance	RO	Loop length or distance to anomaly for pair D (7 and 8)	0x00

Note The resolution of the 6-bit length field is 3 meters.

4.3.12 VeriPHY Control 3

The register at address 26E consists of the third of the three device registers that provide control over VeriPHY diagnostics features. Specifically, this register provides information about the termination status (fault condition) for all four link partner pairs. The following table shows the readouts you can expect.

Table 45. VeriPHY Control Register 3, Address 26E (0x1A)

Bit	Name	Mode	Description	Default
15:12	Pair A (1 and 2) termination status	RO	Termination fault for pair A (1 and 2)	0x00
11:8	Pair B (3 and 6) termination status	RO	Termination fault for pair B (3 and 4)	0x00
7:4	Pair C (4 and 5) termination status	RO	Termination fault for pair C (4 and 5)	0x00
3:0	Pair D (7 and 8) termination status	RO	Termination fault for pair D (7 and 8)	0x00

The following table shows the meanings for the various fault codes.

Table 46. VeriPHY Control Register 3 Fault Codes

Code	Denotes
0000	Correctly terminated pair
0001	Open pair
0010	Shorted pair
0100	Abnormal termination
1000	Cross-pair short to pair A
1001	Cross-pair short to pair B
1010	Cross-pair short to pair C
1011	Cross-pair short to pair D

Table 46. VeriPHY Control Register 3 Fault Codes *(continued)*

Code	Denotes
1100	Abnormal cross-pair coupling with pair A
1101	Abnormal cross-pair coupling with pair B
1110	Abnormal cross-pair coupling with pair C
1111	Abnormal cross-pair coupling with pair D

4.3.13 Reserved Extended Registers

The bits in the extended register page space at addresses 27E and 28E (0x1B and 0x1C, respectively) are reserved.

4.3.14 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two, separate EPG control registers. The following table shows the setting available in the first register.

Table 47. EPG Control Register 1, Address 29E (0x1D)

Bit	Name	Mode	Description	Default
15	EPG enable	R/W	1 = Enable EPG	0
14	EPG run or stop	R/W	1 = Run EPG	0
13	Transmission duration	R/W	1 = Continuous (sends in 10,000-packet increments) 0 = Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (Jumbo packet)	0
10	Inter-packet gap	R/W	1 = 8,192 ns 0 = 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte destination address	0000
1	Payload type	R/W	1 = Randomly generated payload pattern 0 = Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8538 device is connected to a live network.
- Bit 29E.13 (Continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.

- The six-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The six-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.15 Ethernet Packet Generator Control 2

The register at address 30E consists of the second of bits that provide access to and control over various aspects of the EPG testing feature. For information about the first set of EPG control bits, see Table 47, page 65. The following table shows the settings available.

Table 48. EPG Control Register 2, Address 30E (0x1E)

Bit	Name	Mode	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E is set to 1), that bit (29E.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 General-Purpose I/O Registers

Accessing the GPIO page register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the GPIO page register space.

To restore main register page access, write 0x0000 to register 31.

The following table lists the addresses and register names in the GPIO register page space. These registers are accessible only when the device register 31 is set to 0x0010.

Table 49. General-Purpose Registers Page Space

Register Address	Register Name
0G through 12G	Reserved
13G	Reserved
14G	Reserved
15G	GPIO input
16G	GPIO output
17G	GPIO output enable
18G	100BASE-FX control
19G through 30G	Reserved

4.4.1 Reserved GPIO Registers

The bits in registers 0G to 14G of the GPIO register page space are reserved.

4.4.2 GPIO Input Register

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

Table 50. GPIO Input, Address 15G (0x0F)

Bit	Name	Mode	Description	Default
15:0	GPIO [15:0] input	RO	Data read from the GPIO pins	0x00

4.4.3 GPIO Output Register

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

Table 51. GPIO Output, Address 16G (0x10)

Bit	Name	Mode	Description	Default
15:0	GPIO [15:0] output	R/W	Data written out on the GPIO pins	0x00

4.4.4 GPIO Pin Configuration

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

Table 52. GPIO Input/Output Configuration, Address 17G (0x11)

Bit	Name	Mode	Description	Default
15:0	GPIO [15:0] input or output enable	R/W	1 = Pin is configured as an output. 0 = Pin is configured as an input.	0x00

4.4.5 100BASE-FX Control Register

The 100BASE-FX control register can configure each PHY within the device to be in 100BASE-FX mode. The following table shows the values that can be written.

Table 53. 100BASE-FX Control, Address 18G (0x12)

Bit	Name	Mode	Description	Default
15	Activate 100BASE-FX	R/W	0 = No action 1 = Activate 100BASE-FX based on bits 11:0	0
14:12	Reserved	RO		000

Table 53. 100BASE-FX Control, Address 18G (0x12) *(continued)*

Bit	Name	Mode	Description	Default
11	100BASE-FX on all PHYs	R/W	0 = No 100BASE-FX on all PHYs 1 = Configure 100BASE-FX on all PHYs	0
10:8	Individual 100BASE-FX setting	R/W	PHY number to be configured for 100BASE-FX mode	000
7:0	100BASE-FX mode	R/W	0x00 = No 100BASE-FX 0x01 = 100BASE-FX mode 0x02 to 0xFF = Reserved	0x00

Example 1 To configure all PHYs to 100BASE-FX mode, first ensure bit 15 = 0, then set bit 11 = 1 and bits 7:0 = 0x01, and then reset bit 15 = 1.

Example 2 To configure an individual PHY to 100BASE-FX mode, first ensure bit 15 = 0, then set bits 10:8 to the correct PHY number to be configured for 100BASE-FX, then set bits 7:0 = 0x01, and then reset bit 15 = 1. Repeat these steps for each individual PHY.

4.5 CMODE

The information in this section consists of a detailed description of the methods you can use to configure the VSC8538 device using its CMODE pins. It includes descriptions of the registers that work together with the CMODE pins to control the device function.

There are eight configuration mode (CMODE) pins on the VSC8538 device. For more information about the physical location of the CMODE pins, see "Pin Descriptions," page 86. Each of the CMODE pins maps to four configuration bits, which means that each pin controls 16 possible settings for the device.

4.5.1 CMODE Pins and Related Functions

The following table lists the pin numbers and device functionality that is controlled by each configuration bit.

Table 54. CMODE Configuration Pins and Device Functions

CMODE Pin	Bit 3 (MSB) Control	Bit 2 Controls	Bit 1 Controls	Bit 0 (LSB) Controls
7	Reserved Always set to logic 0	Link speed downshift	Speed and duplex [1]	Speed and duplex [0]
6	MAC auto-negotiation	ActiPHY	Advertise asymmetric pause	Advertise symmetric pause
5	Reserved Always set to logic 0	Reserved Always set to logic 0	Clock speed 125 MHz or 156 MHz selection	CLKOUT enable
4	Reserved Always set to logic 0	Reserved Always set to logic 0	LED blink or pulse stretch [1]	LED blink or pulse stretch [0]
3	Reserved Always set to logic 0	LED3 combine or separate	LED3 [1]	LED3 [0]

Table 54. CMODE Configuration Pins and Device Functions *(continued)*

CMODE Pin	Bit 3 (MSB) Control	Bit 2 Controls	Bit 1 Controls	Bit 0 (LSB) Controls
2	PHY address reversal	LED2 combine or separate	LED2 [1]	LED2 [0]
1	PHY address [4]	LED1 combine or separate	LED1 [1]	LED1 [0]
0	PHY address [3]	LED0 combine or separate	LED0 [1]	LED0 [0]

4.5.2 Functions and Related CMODE Pins

The following table lists the pin and bit settings according to the device function and CMODE pin used to configure it.

Table 55. Device Functions and Associated CMODE Pins

Function	Sets MII Register	CMODE Pin	Bit	Description
Link speed downshift	Register 20E, bit 4	7	2	0 = Link only according to the auto-negotiation resolution. 1 = Enable link speed downshift feature.
Speed and duplex	Register 4, bits 8:5 and Register 9, bits 9:8	7	1 and 0	00 = 10/100/1000BASE-T FDX/HDX. 01 = 10/100/1000BASE-T FDX; 10/100BASE-T HDX. 10 = 1000BASE-T FDX only. 11 = 10/100BASE-T FDX/HDX.
MAC auto-negotiation	Register 23, bit 13	6	3	0 = Disabled. 1 = Enabled.
ActiPHY	Register 28, bit 6	6	2	0 = Disabled. 1 = Enabled.
Advertise asymmetric pause	Register 4, bit 11	6	1	0 = Not advertised. 1 = Advertised.
Advertise symmetric pause	Register 4, bit 10	6	0	0 = Not advertised. 1 = Advertised.
Clock speed	Register 20E, bit 8	5	1	0 = 125 MHz. 1 = 156.2 MHz.
CLKOUT enable	Register 18, bit 0	5	0	0 = Disabled. 1 = Enabled.
LED blink/pulse stretch rate	Register 30, bits 11:10	4	1 and 0	00 = 2.5 Hz blink rate, 400 ms pulse stretch. 01 = 5.0 Hz blink rate, 200 ms pulse stretch. 10 = 10.0 Hz blink rate, 100 ms pulse stretch. 11 = 20.0 Hz blink rate, 50 ms pulse stretch.
LED_3, LED_2, LED_1, and LED_0 combine or separate	Register 30, bits 3:0	3, 2, 1, and 0	2	0 = Link, Link10, Link100, Link1000, Link10/100, Link10/1000, Link100/1000. LEDs blink or flash when activity is present. Also, duplex LED blinks or flashes when collision is present. 1 = Link, Link10, Link100, Link1000, Link10/100, Link10/1000, Link100/1000. LEDs indicate status only. Also, duplex LED indicates duplex status only.

Table 55. Device Functions and Associated CMODE Pins *(continued)*

Function	Sets MII Register	CMODE Pin	Bit	Description
LED_3 indication function	Register 29, bits 15:12	3	1 and 0	00 = Duplex or collision. 01 = Link100 or activity. 10 = Activity. 11 = Reserved.
Address reversal		2	3	0 = Normal functioning. PHY address 0:7 = Port 0:7. 1 = Reversed functioning. PHY address 7:0 = Port 0:7.
LED_2 indication function	Register 29, bits 11:8	2	1 and 0	00 = Link or activity. 01 = Duplex or collision. 10 = Reserved. 11 = Link10 or activity.
PHY address [4:3]		1 and 0	3	Sets the two MSBs of the PHY address.
LED_1 indication function	Register 29, bits 7:4	1	1 and 0	00 = Link100 or activity. 01 = Link100/1000 or activity. 10 = Link 10/100 or activity. 11 = Reserved.
LED_0 indication function	Register 29, bits 3:0	0	1 and 0	00 = Link1000 or activity. 01 = Link100/1000 or activity. 10 = Activity. 11 = Link or activity.

Note The MAC auto-negotiation, LED_0, LED_1, LED_2, and LED_3 settings available using the CMODE pins and configuration bits is limited. For full functionality, use the registers. For more information about using the registers for these and other functions, see "Registers," page 39.

4.5.3 CMODE Resistor Values

To affect an aspect of the VSC8538 device configuration, find the parameter in Table 54, page 68 or in Table 55, page 69, and connect the associated pin to the resistor specified in the following table. This sets the bits as shown.

Table 56. CMODE Resistor Values and Resultant Bit Settings

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VSS	0	0	0	0	0
VSS	2.26 kΩ	0	0	0	1
VSS	4.02 kΩ	0	0	1	0
VSS	5.90 kΩ	0	0	1	1
VSS	8.25 kΩ	0	1	0	0
VSS	12.1 kΩ	0	1	0	1
VSS	16.9 kΩ	0	1	1	0
VSS	22.6 kΩ	0	1	1	1
VDD33	0	1	0	0	0

Table 56. CMODE Resistor Values and Resultant Bit Settings *(continued)*

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VDD33	2.26 kΩ	1	0	0	1
VDD33	4.02 kΩ	1	0	1	0
VDD33	5.90 kΩ	1	0	1	1
VDD33	8.25 kΩ	1	1	0	0
VDD33	12.1 kΩ	1	1	0	1
VDD33	16.9 kΩ	1	1	1	0
VDD33	22.6 kΩ	1	1	1	1

Using resistors with the CMODE pins can be optional in designs that access the device's MDC/MDIO pins. In designs that do this, all configurations otherwise affected on the device by using the CMODE pins can be changed using the regular device register settings, and all the CMODE pins can be pulled to VSS (ground). However, in this case, the PHYADDR [4:3] and the PHYADD_REVERSAL settings still require CMODE configuration. This configuration can be set by connecting these pins to either the VDD33 or VSS pins.

4.6 EEPROM

The VSC8538 device EEPROM interface makes it possible for you to set up the device to self-configure its internal registers based on the information programmed into and stored in an external device. To accomplish this, the EEPROM is read on power-up or de-assertion of the NRESET bit. For field configurability, the EEPROM can also be accessed using VSC8538 device registers 21E and 22E.

The EEPROM you use to interface to the VSC8538 device must have a two-wire interface. A device such as the Atmel part AT24CXXX is suggested.

As defined by the interface, data is clocked from the VSC8538 device on the falling edge of EECLK. The device determines that an external EEPROM is present if EEDAT is connected to a 4.7-kΩ external pull-up resistor. The EEDAT pin can be left floating or grounded to indicate that no EEPROM is present.

4.6.1 EEPROM Contents Description

When an EEPROM is present, the VSC8538 device looks for the command header, 0xBDBD at address 0 and 1 of the EEPROM. The address is incremented by 256 until the header is found. If the header is not found or no EEPROM is connected, the VSC8538 device bypasses the EEPROM read step.

When an EEPROM is present, the VSC8538 device waits for an acknowledgement for approximately three seconds (in accordance with the ATMEL EEPROM protocol). If there is no acknowledgement for three seconds, the VSC8538 device aborts its attempt to connect to the EEPROM and reverts to its otherwise normal operating mode.

After the header value is found, the two-byte address value shown in the following table indicates the EEPROM word address where the configuration contents for the device are located. At the base address location, the next set of bytes indicates where the

configuration data contents to be programmed into the VSC8538 device are located. The first address points to the data common to all PHYs. Each subsequent address location points to each individual PHY's configuration contents. At each programming location, the two bytes represent the total number of bytes (11 bits long, with MSB first) where the Total_Number_Bytes[10:0] is equal to the number of SMI writes multiplied by 3 (one byte for SMI port and register address and two bytes for data). Data is read from the EEPROM sequentially until all SMI write commands are completed.

Table 57. EEPROM Configuration Contents

10-bit Address	Content (Bits 7:0)
0	0xBD
1	0xBD
2	PHY_ADDR[4:2], 00, Base_Address_Location[10:8]
3	Base_Address_Location[7:0] (K)
	Address length not specified
K	00000, Common_Config_Base_Address[10:8]
K+1	Common_Config_Base_Address[7:0] (X)
K+2	00000, PHY0_Specific_Config_Base_Address[10:8]
K+3	PHY0_Specific_Config_Base_Address[7:0] (Y)
K+4	00000, PHY1_Specific_Config_Base_Address[10:8]
K+5	PHY1_Specific_Config_Base_Address[7:0]
K+6	00000, PHY2_Specific_Config_Base_Address[10:8]
K+7	PHY2_Specific_Config_Base_Address[7:0]
	Address length not specified
K+16	00000, PHY7_Specific_Config_Base_Address[10:8]
K+17	PHY7_Specific_Config_Base_Address[7:0]
	Address length not specified
X	00000, Total_Number_Bytes[10:8]
X+1	Total_Number_Bytes [7:0] (M)
X+2	Register Address a
X+3	Data[15:8] to be written to Register Address a
X+4	Data[7:0] to be written to Register Address a
X+5	Register Address b
X+6	Data[15:8] to be written to Register Address b
X+7	Data[7:0] to be written to Register Address b
	Address length not specified
X+(M-2)	Register Address x
X+(M-1)	Data[15:8] to be written to Register Address x
X+M	Data[7:0] to be written to Register Address x
	Address length not specified
Y	00000, Total_Number_Bytes[10:8]
Y+1	Total_Number_Bytes [7:0] (N)
Y+2	Register Address a
Y+3	Data[15:8] to be written to Register Address a

Table 57. EEPROM Configuration Contents *(continued)*

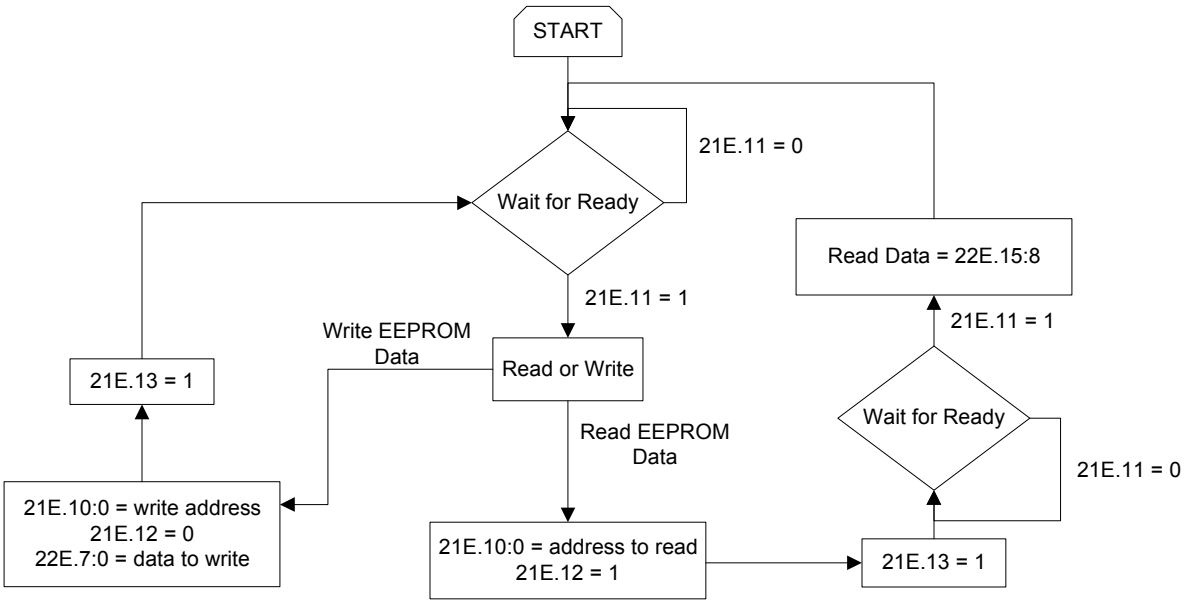
10-bit Address	Content (Bits 7:0)
Y+4	Data[7:0] to be written to Register Address a
	Address length not specified
Y+(N-2)	Register Address x
Y+(N-1)	Data[15:8] to be written to Register Address x
Y+N	Data[7:0] to be written to Register Address x
	Address length not specified
Max Address	

4.6.2 Read/Write Access to the EEPROM

The VSC8538 device also has the ability to read from and write to an EEPROM such as an ATMEL AT24CXXX that is directly connected to its EECLK and EEDAT pins. If it is required to be able to write to the EEPROM, refer to the EEPROM's specific datasheet to ensure that write protection on the EEPROM is not set.

The following illustration shows the interaction of the VSC8538 device and the EEPROM.

Figure 17. EEPROM Read and Write Register Flow



To read a value from a specific address of the EEPROM:

1. Read the VSC8538 device register bit 21E.11 and ensure that it is set.
2. Write the EEPROM address to be read to register bits 21E.10:0.
3. Set both register bits 21E.12 and 21E.13 both to 1.
4. When register bit 21E.11 changes to 1, read the 8-bit data value found at register bits 22E.15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the EEPROM:

1. Read the VSC8538 device register bit 21E.11 and ensure that it is set.
2. Write the address to be written to register bits 21E.10:0.
3. Set register bit 21E.12 to 0.
4. Set register bits 22E.7:0 with the 8-bit value to be written to the EEPROM.
5. Set register bit 21E.13 to 1.

To avoid collisions during read and write transactions, always wait until register bit 21E.11 changes to 1 before performing another EEPROM read or write operation.

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8538 device. It includes information on the various timing functions of the device.

5.1 DC Characteristics

In addition to any parameter-specific conditions, the specifications listed in the following tables may be considered valid only in the environment characterized by the specifications listed as recommended operating conditions for the VSC8538 device. For more information about the recommended operating conditions, see "Operating Conditions," page 85.

5.1.1 VDDIO at 3.3 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 3.3 V
- VDD33 is 3.3 V
- VDD12 is 1.2 V
- VDD12A is 1.2 V

Table 58. DC Characteristics for Pins Referenced to VDDIO at 3.3 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4 mA
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.1.2 VDDIO at 2.5 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 2.5 V
- VDD33 is 3.3 V
- VDD12 is 1.2 V
- VDD12A is 1.2 V

Table 59. DC Characteristics for Pins Referenced to VDDIO at 2.5 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0	2.8	V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	1.7	3.0	V	
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current	I_{ILEAK}	–32	32	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–32	32	µA	Internal resistor included
Output low current drive strength	I_{OL}		6	mA	
Output high current drive strength	I_{OH}	–6		mA	

5.1.3 VDDIO at 1.8 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 1.8 V
- VDD33 is 3.3 V
- VDD12 is 1.2 V
- VDD12A is 1.2 V

Table 60. DC Characteristics for Pins Referenced to VDDIO at 1.8 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	1.4	2.1	V	I_{OH} = –0.5 mA
Output low voltage	V_{OL}	0	0.3	V	I_{OL} = 0.5 mA
Input high voltage	V_{IH}	1.2	2.1	V	
Input low voltage	V_{IL}	0	0.6	V	
Input leakage current	I_{ILEAK}	–23	23	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–23	23	µA	Internal resistor included

Table 60. DC Characteristics for Pins Referenced to VDDIO at 1.8 V *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output low current drive strength	I_{OL}		4.0	mA	
Output high current drive strength	I_{OH}	–4.0		mA	

5.1.4 VDD at 3.3 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 3.3 V
- VDD33 is 3.3 V
- VDD12 is 1.2 V
- VDD12A is 1.2 V

Table 61. DC Characteristics for Pins Referenced to VDD33 at 3.30 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4 mA
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.1.5 MAC Outputs

For more information about the number and physical location of the MAC output pins on the VSC8538 device, see "Pin Descriptions," page 86.

Table 62. DC Characteristics for MAC_RDP/N_*n* Pins

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Frequency lock time	T_{LOCK}		500		µs	
Output differential voltage, peak-to-peak	V_{ODIFF}	700	1000	1200	mV	Based on 100 Ω differential load.
Output common mode voltage	V_{OCM}	480	540	610	mV	VDD12A = 1.20 V.

Table 62. DC Characteristics for MAC_RDP/N_*n* Pins *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Output rise time and fall time (20% to 80%)	t_r , t_f		120	200	ps	
Total jitter, peak-to-peak	T_J		165	220	ps	Uses K28.5 test pattern. Bit error rate (BER) = 10^{-12}.
Total receive jitter tolerance, peak-to-peak	$J_{RXTOTAL}$	420	510		ps	Uses K28.5 test pattern.
Output low current drive strength	I_{OL}			8	mA	
Output high current drive strength	I_{OH}	–8			mA	
Output driver impedance per pin	Z_O		50		Ω	

5.1.6 MAC Inputs

For more information about the number and physical location of the MAC input pins on the VSC8538 device, see "Pin Descriptions," page 86.

Table 63. DC Characteristics for MAC_TDP/N_*n* Pins

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Peak-to-peak input differential voltage	V_{IDIFF}	120	1400	mV	Based on 100 Ω differential load
Input common mode voltage	V_{ICM}	0.4	1.3	V	VDD12A = 1.20 V

5.1.7 LED Pins

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 3.30 V
- VDD33 is 3.30 V
- VDD12 is 1.20 V
- VDD12A is 1.20 V

Table 64. DC Characteristics for LED[3:0]_*n* Pins

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4.0 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4.0 mA
Output leakage current	I_{OLEAK}	–10	10	µA	

Table 64. DC Characteristics for LED[3:0]_*n* Pins *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output low current drive strength	I_{OL}		8.0	mA	
Output high current drive strength	I_{OH}	–8.0		mA	

5.1.8 JTAG Pins

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- VDDIO is 3.30 V
- VDD33 is 3.30 V
- VDD12 is 1.20 V
- VDD12A is 1.20 V

Table 65. DC Characteristics for JTAG Pins

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –1.5 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 1.5 mA
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.2 Current Consumption

The typical current consumption values are based on nominal voltages with all ports operating at 1000BASE-T speeds with full-duplex enabled and a 64-byte random data pattern at 100% utilization.

Table 66. Typical Current Consumption

Parameter	Symbol	Typical	Maximum	Unit
Power consumption under full traffic conditions	P_D		5.91	W
Current with VDDIO at 1.8 V	I_{VDDIO}	1		mA
Current with VDDIO at 2.5 V	I_{VDDIO}	1		mA
Current with VDDIO at 3.3 V	I_{VDDIO}	1		mA
Current with VDD33A at 3.3 V	I_{VDD33A}	852		mA
Current with VDDIG at 1.2 V	I_{VDD12}	1488		mA

Table 66. Typical Current Consumption *(continued)*

Parameter	Symbol	Typical	Maximum	Unit
Current with VDD12A at 1.2 V	I_{VDD12A}	490		mA

5.3 AC Characteristics

The AC specifications are grouped according to specific device pins and associated timing characteristics.

5.3.1 Reference Clock Input

The following table shows the specifications for the reference clock input frequency including various frequencies, duty cycle, and accuracy.

Table 67. AC Characteristics for REFCLK Input

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Frequency with 25 MHz input	f_{CLK25}		25		MHz
Frequency with 125 MHz input	f_{CLK125}		125		MHz
Frequency accuracy	f_{TOL}			100	ppm
Duty cycle	$\%_{DUTY}$	40		60	%
Rise time with 25 MHz input (20% to 80%)	t_{R25}			4	ns
Rise time with 125 MHz input (20% to 80%)	t_{R125}			1	ns
Fall time with 25 MHz input (20% to 80%)	t_{R25}			4	ns
Fall time with 125 MHz input (20% to 80%)	t_{F125}			1	ns

If using the 25 MHz crystal clock input option, the additional specifications in the following table are required.

Table 68. AC Characteristics for REFCLK Input with 25 MHz Clock Input

Parameter	Minimum	Typical	Maximum	Unit
Crystal parallel load capacitance	18		20	pF
Crystal equivalent series resistance		10	30	Ω
Crystal accuracy			50	ppm

5.3.2 Clock Output

The specifications in the following table show the AC characteristics for the clock output of the VSC8538 device when used in your design.

Table 69. AC Characteristics for the CLKOUT Pin

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
CLKOUT frequency	f_{CLK125}		125.00 156.25		MHz	125 MHz output clock 156.25 MHz output clock
CLKOUT cycle time	t_{CYC}		8.0 6.4		ns	125 MHz output clock 156.25 MHz output clock
Frequency stability	$f_{STABILITY}$			100	ppm	
Duty cycle	$\%_{DUTY}$	40	50	60	%	
Clock rise and fall times (20% to 80%)	t_R and t_F			1	ns	
Total jitter(1)	J_{CLK}		217	491	ps	Measured peak-to-peak

1. These values were tested with a low ppm oscillator and linear power supplies. The quality of the clock and power supply affects these values.

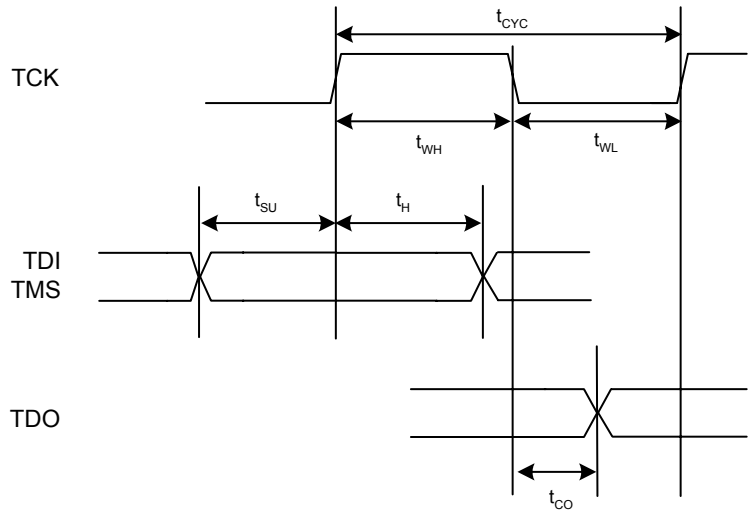
5.3.3 JTAG Interface

The following table lists the characteristics for the JTAG testing feature. The illustration provides a diagram of the timing.

Table 70. AC Characteristics for the JTAG Interface

Parameter	Symbol	Minimum	Maximum	Unit
TCK frequency	f_{CLK}		10	MHz
TCK cycle time	t_{CYC}	100		ns
TCK time high	t_{WH}	45		ns
TCK time low	t_{WL}	45		ns
Setup to TCLK rising	t_{SU}	10		ns
Hold from TCLK rising	t_H	10		ns
TCK to TDO valid	t_{CO}		15	ns

Figure 18. JTAG Interface Timing



5.3.4 SMI Interface

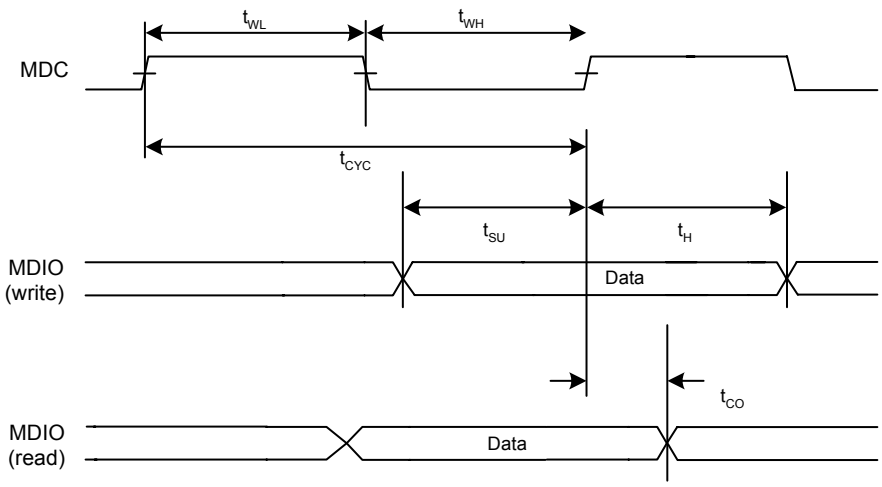
Use the information in the following table when incorporating the VSC8538 device SMI interface into your own design. The illustration provides information about SMI interface timing.

Table 71. AC Characteristics for the SMI Interface

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}		2.5	12.5	MHz	
MDC cycle time	t_{CYC}	80	400		ns	
MDC time high	t_{WH}	20	50		ns	
MDC time low	t_{WL}	20	50		ns	
Setup to MDC rising	t_{SU}	10			ns	
Hold from MDC rising	t_H	10			ns	
MDC rise time	t_R	100 t_{CYC} × 10%(1)			ns	For MDC = 0 – 1 MHz For MDC = 1 MHz – f_{CLK}(MAX)
MDC fall time	t_F	100 t_{CYC} × 10%(1)				
MDC to MDIO valid	t_{CO}		10	300	ns	Time dependant on value of external pull-up resistor on MDIO pin

1. For f_{CLK} above 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 19. SMI Interface Timing



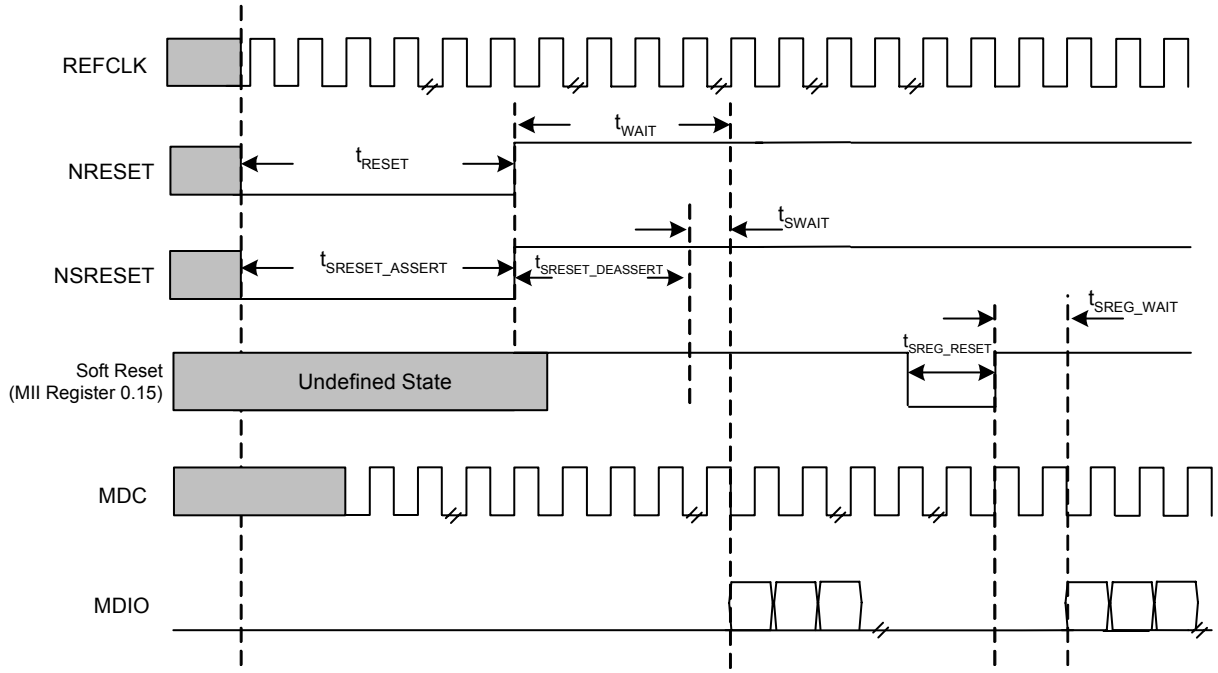
5.3.5 Device Reset

The following specifications apply to the device reset functionality. The illustration shows the reset timing.

Table 72. AC Characteristics for Device Reset

Parameter	Symbol	Minimum	Maximum	Unit	Condition
NRESET assertion time	t_{RESET}	100		ns	
Wait time between NRESET deassert and access of the SMI interface	t_{WAIT}	20 220		ms ms	Register 21E.14 = 0 Register 21E.14 = 1
Soft reset (pin) assertion	t_{SRESET_ASSERT}	4		ms	
Soft reset (pin) deassertion	$t_{SRESET\_DEASSERT}$	4		ms	
Wait time between soft reset pin deassert and access of the SMI interface	t_{SWAIT}	4 300 200 200		µs µs ms ms	Registers 22.9 = 1, 21E.14 = 0 Registers 22.9 = 0, 21E.14 = 0 Registers 22.9 = 0, 21E.14 = 1 Registers 22.9 = 1, 21E.14 = 1
Soft reset MII register 0.15 assertion	t_{SREG_RESET}	100		ns	
Wait time between Soft Reset (MII Register 0.15) deassert and access to the SMI interface	t_{SREG_WAIT}	4 300 200 200		µs µs ms ms	Registers 22.9 = 1, 21E.14 = 0 Registers 22.9 = 0, 21E.14 = 0 Registers 22.9 = 0, 21E.14 = 1 Registers 22.9 = 1, 21E.14 = 1

Figure 20. Reset Timing



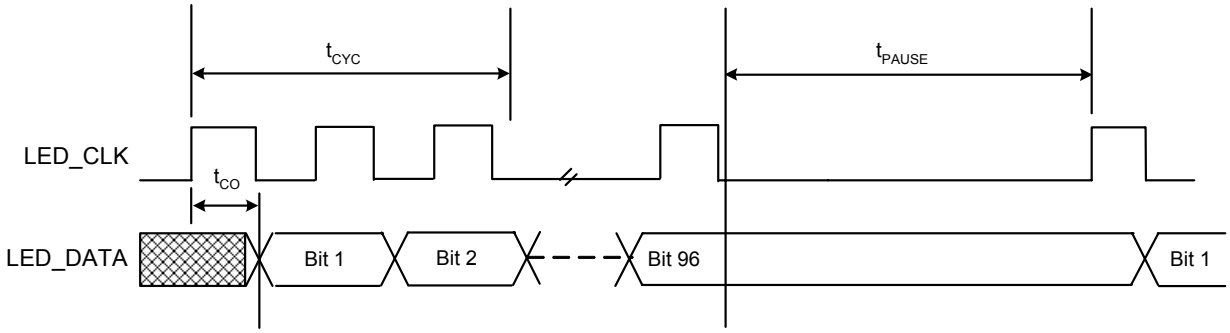
5.3.6 Serial LEDs

The following table provides specifications for the device serial LEDs. The illustration shows the LED timing.

Table 73. AC Characteristics for Serial LEDs

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	1		µs
Pause between LED bit sequences	t_{PAUSE}	25		ms
LED_CLK to LED_DATA	t_{CO}		1	ns

Figure 21. Serial LED Timing



5.4 Operating Conditions

The following table shows the recommended operating conditions for the VSC8538 device.

Table 74. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for VDDIO at 1.8 V	V_{DDIO}	1.70	1.80	1.90	V
Power supply voltage for VDDIO at 2.5 V	V_{DDIO}	2.37	2.50	2.63	V
Power supply voltage for VDDIO at 3.3 V	V_{DDIO}	3.13	3.30	3.47	V
Power supply voltage for VDD33A	V_{DD33A}	3.13	3.30	3.47	V
Power supply voltage for VDDIG	V_{DDIG}	1.14	1.20	1.26	V
Power supply voltage for VDD12A	V_{DD12A}	1.14	1.20	1.26	V
Operating temperature(1)	T	0		90	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

5.5 Stress Ratings

This section contains the stress ratings for the VSC8538 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 75. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
DC input voltage on VDDIO supply pin	V_{DDIO}	–0.5	4.0	V
DC input voltage on VDD33 supply pin	V_{DD33}	–0.5	4.0	V
DC input voltage on VDD12 supply pin	V_{DD12}	–0.5	1.4	V
DC input voltage on VDD12A supply pin	V_{DD12A}	–0.5	1.4	V
DC input voltage on JTAG 5 V-tolerant pins	V_{DD}(5 V)	–0.5	5.5	V
DC input voltage on any non-supply pin	V_{DD}(PIN)	–0.5	VDD + 0.5	V
Storage temperature	T_S	–65	150	°C
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8538 device has 444 pins, which are described in this section.

6.1 Pin Diagram

The following illustrations show the physical location of the pins on the VSC8538 device. For clarity, the device is shown in two halves; first, the left half, with the viewer oriented looking downward at the device; and second, the right half, again with the viewer looking down at the device.

Figure 22. Pin Diagram, Left Side, Top

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		VSS	TXVPB_6	TXVPC_6	TXVPD_6	TXVPA_5	TXVPB_5	TXVPC_5	TXVPD_5	TXVPA_4	TXVPB_4	TXVPC_4	TXVPD_4
B	VSS	VSS	TXVNB_6	TXVNC_6	TXVND_6	TXVNA_5	TXVNB_5	TXVNC_5	TXVND_5	TXVNA_4	TXVNB_4	TXVNC_4	TXVND_4
C	TXVPA_6	TXVNA_6	VDD33	VDD33	VSS	NC	VDD12A	VSS	VSS	VDD33	VDD33	VDD33	VDD12A
D	TXVPD_7	TXVND_7	VDD33	VDD33	VSS	VDD12A	VDD12A	VSS	VSS	VDD33	VDD33	VDD33	VDD12A
E	TXVPC_7	TXVNC_7	VDD12A	VDD12A									
F	TXVPB_7	TXVNB_7	VSS	REF_REXT_B									
G	TXVPA_7	TXVNA_7	NC	REF_FILT_B									
H	VSS	VSS	VSS	VSS									
J	XTAL1/REFCLK	XTAL2	LED3_7	LED2_7									
K	VSS	VSS	LED1_7	LED0_7				VDD12	VSS	VSS	VSS	VSS	VSS
L	LED3_6	LED2_6	LED3_5	LED2_5				VDD12	VSS	VSS	VSS	VSS	VSS
M	LED1_6	LED0_6	LED1_5	LED0_5				VDD12	VSS	VSS	VSS	VSS	VSS
N	VDD33	VDD33	VDD33	VDD33				VDD12	VSS	VSS	VSS	VSS	VSS
P	EECLK	EEDAT	LED3_4	LED2_4				VDD12	VSS	VSS	VSS	VSS	VSS
R	PLLMODE	OSCEN	LED1_4	LED0_4				VDD12	VSS	VSS	VSS	VSS	VSS
T	TMS	TCK	NTRST	TDO				VDD12	VSS	VSS	VSS	VSS	VSS
U	TDI	VDDIO	MDC	VDD33				VDD12	VDD12	VDD12	VDD12	VDD12	VDD12
V	CLKOUT	VDDIO	MDIO	VSS									
W	MDINT_0	MDINT_1	MDINT_2	MDINT_3									
Y	MDINT_4	MDINT_5	MDINT_6	MDINT_7									
AA	NC	NC	NRESET	VSS									
AB	NC	NC	VSS	VDDIO									
AC	MAC_RDN_7	MAC_RDP_7	VSS	VDD12A	VDD12A	VSS	VDD12A	VDD12A	VSS	VSS	VDD12A	VDD12A	VDD12A
AD	MAC_TDN_7	MAC_TDP_7	VDD33	VSS	VDD33	VSS	VDD33	VDD12A	VSS	VSS	VDD33	VDD33	VSS
AE	VSS	NC	NC	MAC_RDP_6	MAC_TDP_6	NC	NC	MAC_RDP_5	MAC_TDP_5	NC	NC	MAC_RDP_4	MAC_TDP_4
AF		NC	NC	MAC_RDN_6	MAC_TDN_6	NC	NC	MAC_RDN_5	MAC_TDN_5	NC	NC	MAC_RDN_4	MAC_TDN_4
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 23. Pin Diagram, Right Side, Top

14	15	16	17	18	19	20	21	22	23	24	25	26	
TXVPA_3	TXVPB_3	TXVPC_3	TXVPD_3	TXVPA_2	TXVPB_2	TXVPC_2	TXVPD_2	TXVPA_1	TXVPB_1	TXVPC_1	TXVPD_1		A
TXVNA_3	TXVNB_3	TXVNC_3	TXVND_3	TXVNA_2	TXVNB_2	TXVNC_2	TXVND_2	TXVNA_1	TXVNB_1	TXVNC_1	TXVND_1	VSS	B
VSS	VSS	VDD33	VDD33	VSS	VDD12A	VDD12A	VDD33	NC	VDD33	VSS	VDD33	VSS	C
VSS	VSS	VDD33	VDD33	VSS	VDD12A	VDD12A	VDD33	VDD33	VDD12A	VSS	TXVNA_0	TXVPA_0	D
									REF_FILT_A	VDD12A	TXVNB_0	TXVPB_0	E
									REF_REXT_A	VDD33	TXVNC_0	TXVPC_0	F
									VDD33	NC	TXVND_0	TXVPD_0	G
									VDD33	VDD33	CMODE7	VSS	H
									VDD33	CMODE6	CMODE5	CMODE4	J
VSS	VSS	VSS	VSS	VSS	VDD12				VSS	CMODE3	CMODE2	CMODE1	K
VSS	VSS	VSS	VSS	VSS	VDD12				VSS	CMODE0	LED1_0	LED0_0	L
VSS	VSS	VSS	VSS	VSS	VDD12				VDD33	VDD33	LED3_0	LED2_0	M
VSS	VSS	VSS	VSS	VSS	VDD12				LED1_2	LED0_2	LED1_1	LED0_1	N
VSS	VSS	VSS	VSS	VSS	VDD12				LED3_2	LED2_2	LED3_1	LED2_1	P
VSS	VSS	VSS	VSS	VSS	VDD12				LED1_3	LED0_3	VDD33	VDD33	R
VSS	VSS	VSS	VSS	VSS	VDD12				LED3_3	LED2_3	GPIO14	GPIO15	T
VDD12	VDD12	VDD12	VDD12	VDD12	VDD12				GPIO10	GPIO11	GPIO12	GPIO13	U
									GPIO6 / SIGDET_6	GPIO7 / SIGDET_7	GPIO8	GPIO9	V
									GPIO2 / SIGDET_2	GPIO3 / SIGDET_3	GPIO4 / SIGDET_4	GPIO5 / SIGDET_5	W
									GPIO0 / SIGDET_0	GPIO1 / SIGDET_1	VSS	VSS	Y
									VDD33	VSS	MAC_TDP_0	MAC_TDN_0	AA
									VDD33	VDD12A	MAC_RDP_0	MAC_RDN_0	AB
VSS	VDD12A	VDD12A	VSS	VDD12A	VDD12A	VDD12A	VSS	VSS	VSS	VDD12A	NC	NC	AC
VDD33	VSS	VSS	VDD33	VSS	VDD12A	VDD33	VDD33	VSS	VSS	VSS	NC	NC	AD
NC	NC	MAC_RDP_3	MAC_TDP_3	NC	NC	MAC_RDP_2	MAC_TDP_2	NC	NC	MAC_RDP_1	MAC_TDP_1	VSS	AE
NC	NC	MAC_RDN_3	MAC_TDN_3	NC	NC	MAC_RDN_2	MAC_TDN_2	NC	NC	MAC_RDN_1	MAC_TDN_1		AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

6.2 Pin Identifications

This section provides a series of tables that list the pin descriptions for the VSC8538 device, sorted according to their function.

6.2.1 SerDes MAC Interface

The following table shows the pins associated with the device SerDes MAC interface.

Table 76. SerDes MAC Interface Pins

Pin	Name	Type	Description
AD2	MAC_TDP_7	I_{DIFF}	SerDes MAC transmitter input pair.
AE5	MAC_TDP_6		
AE9	MAC_TDP_5		
AE13	MAC_TDP_4		
AE17	MAC_TDP_3		
AE21	MAC_TDP_2		
AE25	MAC_TDP_1		
AA25	MAC_TDP_0		
AD1	MAC_TDN_7		
AF5	MAC_TDN_6		
AF9	MAC_TDN_5		
AF13	MAC_TDN_4		
AF17	MAC_TDN_3		
AF21	MAC_TDN_2		
AF25	MAC_TDN_1		
AA26	MAC_TDN_0		
AC2	MAC_RDP_7	O_{DIFF}	SerDes MAC receiver output pair.
AE4	MAC_RDP_6		
AE8	MAC_RDP_5		
AE12	MAC_RDP_4		
AE16	MAC_RDP_3		
AE20	MAC_RDP_2		
AE24	MAC_RDP_1		
AB25	MAC_RDP_0		
AC1	MAC_RDN_7		
AF4	MAC_RDN_6		
AF8	MAC_RDN_5		
AF12	MAC_RDN_4		
AF16	MAC_RDN_3		
AF20	MAC_RDN_2		
AF24	MAC_RDN_1		
AB26	MAC_RDN_0		

6.2.2 GPIO

The following table shows the pins associated with the device GPIO.

Table 77. GPIO Pins

Pin	Name	Type	Description
T26	GPIO15	I_{PD}/O	General purpose input/output (GPIO). 16 dedicated GPIO pins are provided.
T25	GPIO14		
U26	GPIO13		
U25	GPIO12		
U24	GPIO11		
U23	GPIO10		
V26	GPIO9		
V25	GPIO8		
V24	GPIO7		
V23	GPIO6		
W26	GPIO5		
W25	GPIO4		
W24	GPIO3		
W23	GPIO2		
Y24	GPIO1		
Y23	GPIO0		

6.2.3 Twisted Pair Interface

The following table lists the device pins associated with the device two-wire, twisted pair interface.

Table 78. Twisted Pair Interface Pins

Pin	Name	Type	Description
G1	TXVPA_7	A_{DIFF}	TX/RX channel A positive signal
C1	TXVPA_6		
A6	TXVPA_5		
A10	TXVPA_4		
A14	TXVPA_3		
A18	TXVPA_2		
A22	TXVPA_1		
D26	TXVPA_0		
G2	TXVNA_7	A_{DIFF}	TX/RX channel A negative signal
C2	TXVNA_6		
B6	TXVNA_5		
B10	TXVNA_4		
B14	TXVNA_3		
B18	TXVNA_2		
B22	TXVNA_1		
D25	TXVNA_0		
F1	TXVPB_7	A_{DIFF}	TX/RX channel B positive signal
A3	TXVPB_6		
A7	TXVPB_5		
A11	TXVPB_4		
A15	TXVPB_3		
A19	TXVPB_2		
A23	TXVPB_1		
E26	TXVPB_0		

Table 78. Twisted Pair Interface Pins *(continued)*

Pin	Name	Type	Description
F2	TXVNB_7	A_{DIFF}	TX/RX channel B negative signal
B3	TXVNB_6		
B7	TXVNB_5		
B11	TXVNB_4		
B15	TXVNB_3		
B19	TXVNB_2		
B23	TXVNB_1		
E25	TXVNB_0		
E1	TXVPC_7	A_{DIFF}	TX/RX channel C positive signal
A4	TXVPC_6		
A8	TXVPC_5		
A12	TXVPC_4		
A16	TXVPC_3		
A20	TXVPC_2		
A24	TXVPC_1		
F26	TXVPC_0		
E2	TXVNC_7	A_{DIFF}	TX/RX channel C negative signal
B4	TXVNC_6		
B8	TXVNC_5		
B12	TXVNC_4		
B16	TXVNC_3		
B20	TXVNC_2		
B24	TXVNC_1		
F25	TXVNC_0		
D1	TXVPD_7	A_{DIFF}	TX/RX channel D positive signal
A5	TXVPD_6		
A9	TXVPD_5		
A13	TXVPD_4		
A17	TXVPD_3		
A21	TXVPD_2		
A25	TXVPD_1		
G26	TXVPD_0		
D2	TXVND_7	A_{DIFF}	TX/RX channel D negative signal
B5	TXVND_6		
B9	TXVND_5		
B13	TXVND_4		
B17	TXVND_3		
B21	TXVND_2		
B25	TXVND_1		
G25	TXVND_0		

6.2.4 Serial Management Interface

The following table lists the device pins associated with the device serial management interface (SMI). Note that the pins in this table, except for EECLK and EEDAT, are

referenced to VDDIO and can be set to a 1.8 V, 2.5 V, or 3.3 V power supply. The EECLK and EEDAT pins are instead referenced to VDD33.

Table 79. SMI Pins

Pin	Name	Type	Description
U3	MDC	I	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
V3	MDIO	OD	Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.
Y4 Y3 Y2 Y1 W4 W3 W2 W1	MDINT_7 MDINT_6 MDINT_5 MDINT_4 MDINT_3 MDINT_2 MDINT_1 MDINT_0	OS/OD	Management interrupt signal. Upon reset the device will configure these pins as active-low (open drain) or active-high (open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.
P2	EEDAT	I_{PD}/O	(Optional) EEPROM serial I/O data. Used to configure PHYs in a system without a Station Manager. Connect to the SDA pin of the ATMEL “AT24CXXX” serial EEPROM device family. The VSC8538 device determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when NRESET is de-asserted. If EEDAT has a 4.7 kΩ external pull-up resistor, the VSC8538 assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.
P1	EECLK	O	(Optional) EEPROM serial output clock. Used to configure PHYs in a system without a station manager. Connect to the SCL pin of the ATMEL “AT24CXXX” serial EEPROM device family.
AA3	NRESET	I_{PU}	Device reset. Active low input that powers down the device and sets the register bits to their default state.
V1	CLKOUT	O	Clock output can be enabled or disabled and also output a reference clock frequency of 125 MHz or 156.25 MHz using CMODE or register setting. This pin is not active when NRESET is asserted. When disabled, the pin is held low.

6.2.5 JTAG

The following table lists the pins associated with the device JTAG testing facility.

Table 80. JTAG Pins

Pin	Name	Type	Description
U1	TDI	I_{PU5V}	JTAG test serial data input.

Table 80. JTAG Pins *(continued)*

Pin	Name	Type	Description
T4	TDO	O	JTAG test serial data output.
T1	TMS	I_{PU5V}	JTAG test mode select.
T2	TCK	I_{PU5V}	JTAG test clock input.
T3	NTRST	I_{PU5V}	JTAG reset. If JTAG is not used, then tie this pin to VSS (ground) with a pull-down resistor.

6.2.6 Power Supply

The following table lists the device power supply pins.

Table 81. Power Supply Pins

Pin	Name	Type	Description
C3 C4 C10 C11 C12 C16 C17 C21 C23 C25 D3 D4 D10 D11 D12 D16 D17 D21 D22 F24 G23 H23 H24 J23 M23 M24 N1 N2 N3 N4 R25 R26 U4 AA23 AB23 AD3 AD5 AD7 AD11 AD12 AD14 AD17 AD20 AD21	VDD33	3.3 V	General 3.3 V power supply
U2 V2 AB4	VDDIO	3.3 V 2.5 V 1.8 V	I/O power supply
K8 K19 L8 L19 M8 M19 N8 N19 P8 P19 R8 R19 T8 T19 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19	VDD12	1.2 V	Internal digital core voltage
C7 C13 C19 C20 D6 D7 D13 D19 D20 D23 E3 E4 E24 AB24 AC4 AC5 AC7 AC8 AC11 AC12 AC13 AC15 AC16 AC18 AC19 AC20 AC24 AD8 AD19	VDD12A	1.2 V	1.2 V analog power requiring additional PCB power supply filtering

Table 81. Power Supply Pins *(continued)*

Pin	Name	Type	Description
A2 B1 B2 B26 C5 C8 C9 C14 C15 C18 C24 C26 D5 D8 D9 D14 D15 D18 D24 F3 H1 H2 H3 H4 H26 K1 K2 K9 K10 K11 K12 K13 K14 K15 K16 K17 K18 K23 L9 L10 L11 L12 L13 L14 L15 L16 L17 L18 L23 M9 M10 M11 M12 M13 M14 M15 M16 M17 M18 N9 N10 N11 N12 N13 N14 N15 N16 N17 N18 P9 P10 P11 P12 P13 P14 P15 P16 P17 P18 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 V4 Y25 Y26 AA4 AA24 AB3 AC3 AC6 AC9 AC10 AC14 AC17 AC21 AC22 AC23 AD4 AD6 AD9 AD10 AD13 AD15 AD16 AD18 AD22 AD23 AD24 AE1 AE26	VSS	0 V	General device ground

Although certain function pins may not be used for a specific application, all power supply pins must be connected to their respective voltage input.

Table 82. Power Supply and Associated Function Pins

Pin	Nominal Voltage	Associated Functional Pins
VDD33	3.3 V	LED[3:0]_n, GPIO[15:0], EECLK, EEDAT, JTAG (5), XTAL1, XTAL2, CMODE, TXVP_n, TXVN_n, REF_FILT, REF_REXT
VDDIO	1.8 V, 2.5 V, 3.3 V	MDC, MDIO, MDINT_n, nRESET, CLKOUT
VDD12A	1.2 V	MAC_RDP/N_n, MAC_TDP/N_n
VDD12	1.2 V	N/A (Internal Core Voltage)

6.2.7 Miscellaneous

The following table lists pins not associated with a particular interface or facility on the device.

Table 83. Miscellaneous Pins

Pin	Name	Type	Description
H25 J24 J25 J26 K24 K25 K26 L24	CMODE7 CMODE6 CMODE5 CMODE4 CMODE3 CMODE2 CMODE1 CMODE0	I_A	Configuration mode (CMODE) pins. For more information, see "CMODE," page 68.
J1	XTAL1/ REFCLK	I	Crystal oscillator input. If OSCEN=high then a 25 MHz parallel resonant crystal with +/- 50 ppm frequency tolerance should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL1 pin to ground. Reference clock input. If OSCEN=low, the clock input frequency can either be 25 MHz (PLLMODE=0) or 125 MHZ (PLLMODE is high).
J2	XTAL2	O_{CRYST}	Crystal oscillator output. The crystal should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL2 pin to ground. If not using a crystal oscillator, this output pin can be left floating if driving XTAL1/REFCLK with a reference clock.
R2	OSCEN	I_{PD}	Oscillator enable. This pin is sampled on the rising edge of NRESET. If HIGH, then the on-chip oscillator circuit is enabled. If low (or left floating), the oscillator circuit is disabled and the device must be supplied with a 25 MHz or 125 MHz reference clock to the REFCLK pin
R1	PLLMODE	I_{PD}	PLL mode input select. Sampled on power-up or reset. If PLLMODE is low, then REFCLK must be 25 MHz. If PLLMODE is high, then REFCLK must be 125 MHz.
J3 J4 K3 K4 L1 L2 M1 M2 L3 L4 M3 M4 P3 P4 R3 R4 T23 T24 R23 R24 P23 P24 N23 N24 P25 P26 N25 N26 M25 M26 L25 L26	LED[3:0]_7 LED[3:0]_6 LED[3:0]_5 LED[3:0]_4 LED[3:0]_3 LED[3:0]_2 LED[3:0]_1 LED[3:0]_0	O	LED direct-drive outputs. All LEDs pins are active-low. A serial LED stream can also be implemented. For more information about LED operation, see "LED Mode Select," page 56.
F23	REF_REXT_A	A_{BIAS}	Reference external connects to an external 2 KΩ (1%) resistor to analog ground.
E23	REF_FILT_A	A_{BIAS}	Reference filter connects to an external 1 µF capacitor to analog ground.
F4	REF_REXT_B	A_{BIAS}	Reference external connects to an external 2 KΩ (1%) resistor to analog ground.
G4	REF_FILT_B	A_{BIAS}	Reference filter connects to an external 1 µF capacitor to analog ground.

Table 83. Miscellaneous Pins *(continued)*

Pin	Name	Type	Description
G3 C6 C22 G24 AA1 AA2 AB1 AB2 AC25 AC26 AD25 AD26 AE2 AE3 AE6 AE7 AE10 AE11 AE14 AE15 AE18 AE19 AE22 AE23 AF2 AF3 AF6 AF7 AF10 AF11 AF14 AF15 AF18 AF19 AF22 AF23	NC	NC	These pins are no connects. Do not connect them together or to ground. Leave these pins unconnected (floating).

7 Package Information

The VSC8538 device is available in two package types. VSC8538HJ is a 444-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8538XHJ.

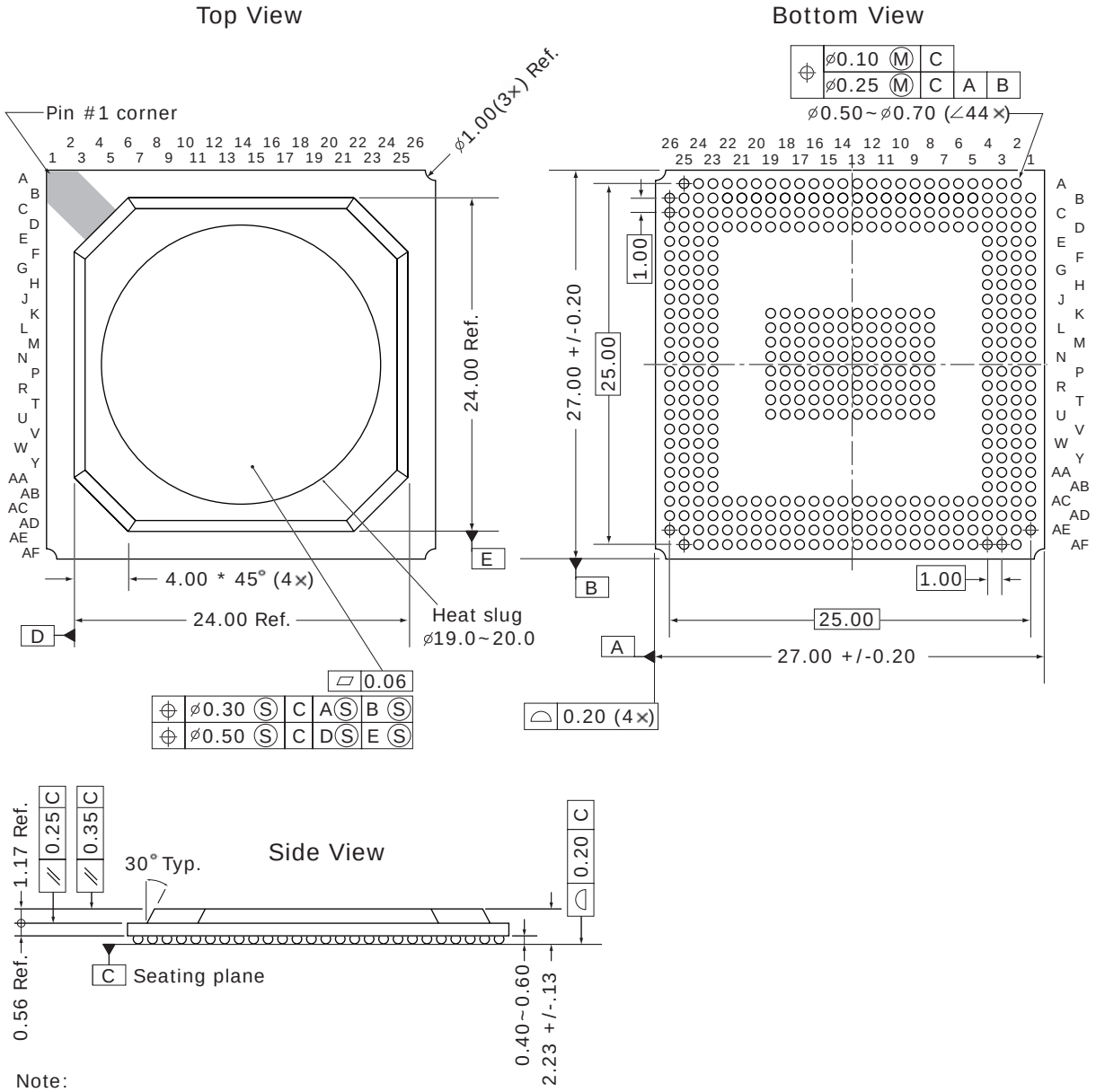
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8538 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8538 device. The drawing contains the top view, bottom view, and side view, as well as information pertaining to dimensional tolerances and other notes. The information in the inllustration applies to both the available package types.

Figure 24. Package Drawing



Note:
All dimensions are in millimeters (mm).

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 84. Thermal Resistances

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC8538HJ	4.1	7.3	13.4	13.2	13
VSC8538XHJ	4.1	7.3	13.4	13.2	13

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Consideratons

This section provides design considerations for the VSC8538 device.

8.1 Remote Fault Status

Issue: Register 1, bit 4 (remote fault) has a reporting issue. The purpose of this register bit is to latch a remote fault indication on the positive edge from the Cat5 link partner and clear the indication when register 1 is read. However, after an initial remote fault, followed by a management read of register 1, bit 4, if then a re-autoneg is attempted by the link partner, the PHY will miss this event because it only latches on the initial positive edge, thereby missing the remote fault event and not setting bit 4 = 1.

Implications: This feature will fail UNH's test suite.

Workaround: None.

8.2 ActiPHY Wake Timer Needs to be Set to '11'

Issue: The ActiPHY Wake Timer (extended register 20E, bits 12:11) does not work as stated in the datasheet. This timer must be set to a value of two seconds (register 20E.12:11 = '11') to allow the device to function properly.

Implications: When using the ActiPHY Wake Timer feature, the workaround must be implemented in order for each PHY to function properly.

Workaround: There is a software workaround. Implement the following script at PHY initialization time:

```
PhyWrite( PortNo, Register (dec), 16_bit_unsigned_data(hex) );

16_bit_unsigned_data = PhyRead( PortNo, Register (dec) );



PhyWrite( PortNo, 31, 0x0001 ); // Switch to Extended Page register

Reg20E = PhyRead( PortNo, 20 );

Reg20E = ( Reg20E | 0x1800 ); // Set Bit 12 = 1, and Bit 11 = 1

PhyWrite( PortNo, 20, Reg20E );

PhyWrite( PortNo, 31, 0x0000 ); // Go to Normal Page
```

8.3 DSP Optimization Script

Issue: In order to ensure robust cable performance, a DSP optimization script is required. This script will change the behavior of the internal DSP.

Implications: Using this optimization script will ensure robust cable performance.

Workaround: Change the DSP settings using the following script at PHY initialization time:

```
PhyWrite( PortNo, Register (dec), 16_bit_unsigned_data(hex) );

PhyWriteMsk( PortNo, Register (dec), 16_bit_unsigned_data(hex), mask );


PhyWrite( PortNo, 31, 0x52B5 );

PhyWrite( PortNo, 16, 0xAF8A );

PhyWriteMsk( PortNo, 18, 0x0000, 0x0000 );

PhyWriteMsk( PortNo, 17, 0x0008, 0x000C );

PhyWrite( PortNo, 16, 0x8F8A );

PhyWrite( PortNo, 16, 0xAF86 );

PhyWriteMsk( PortNo, 18, 0x0008, 0x000C );

PhyWriteMsk( PortNo, 17, 0x0000, 0x0000 );

PhyWrite( PortNo, 16, 0x8F86 );

PhyWrite( PortNo, 16, 0xAF82 );

PhyWriteMsk( PortNo, 18, 0x0000, 0x0000 );

PhyWriteMsk( PortNo, 17, 0x0100, 0x0180 );

PhyWrite( PortNo, 16, 0x8F82 );

PhyWrite( PortNo, 31, 0x0000 );
```

9 Ordering Information

The VSC8538 device is available in two package types. VSC8538HJ is a 444-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8538XHJ.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8538 device.

Table 85. Ordering Information

Part Order Number	Description
VSC8538HJ	444-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height
VSC8538XHJ	Lead(Pb)-free, 444-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height